



Embedded ESD Protection Proof of Concept Final Report

David Gerke
Jet Propulsion Laboratory
Pasadena, CA

Bill Herrmann
Electronic Polymer, Inc.
Round Rock, TX

Jet Propulsion Laboratory
California Institute of Technology
Pasadena, California

JPL Publication 08-25 8/08



Embedded ESD Protection Proof of Concept Final Report

NASA Electronic Parts and Packaging (NEPP) Program
Office of Safety and Mission Assurance

David Gerke
Jet Propulsion Laboratory
Pasadena, CA

Bill Herrmann
Electronic Polymer, Inc.
Round Rock, TX

NASA WBS: 939904.01.11.20
JPL Project Number: 102197
Task Number: 2.33.6

Jet Propulsion Laboratory
4800 Oak Grove Drive
Pasadena, CA 91109

<http://nepp.nasa.gov>

This research was carried out at the Jet Propulsion Laboratory, California Institute of Technology, and was sponsored by the National Aeronautics and Space Administration Electronic Parts and Packaging (NEPP) Program.

Reference herein to any specific commercial product, process, or service by trade name, trademark, manufacturer, or otherwise, does not constitute or imply its endorsement by the United States Government or the Jet Propulsion Laboratory, California Institute of Technology.

Copyright 2008. All rights reserved.

Table of Contents

Abstract..... 1

1.0 Electrostatic Discharge and ESD Standards 1

2.0 EPI-FLO™ Polymer Voltage Suppression (PVS) Devices 2

3.0 Project Overview 3

 3.1 Phase 1 3

 3.2 Phase 2 6

 3.3 Phase 3 9

 3.4 Phase 4 10

4.0 Summary 13

References..... 13

Abstract

The purpose of this project is to characterize and correlate Electrostatic Discharge (ESD) sensitivity levels of an Integrated Circuit (IC) package using Transmission Line Pulse (TLP) and Human Body Model (HBM) methods. This characterization will be used as a baseline ESD sensitivity level to demonstrate improvement to the ESD sensitivity of the IC package through the use of EPI-FLO™ Polymer Voltage Suppression (PVS) protection devices developed and manufactured by Electronic Polymers, Inc. (EPI).

1.0 Electrostatic Discharge and ESD Standards

Static electricity is defined as an electrical charge caused by an imbalance of electrons on the surface of a material, which then produces an electric field. Electrostatic Discharge (ESD) is defined as the transfer of charges between bodies at different electrical potential. ESD transient events are typically characterized by several hundreds or thousands of volts with very fast rise times, typically the transients only last for tens to hundreds of nanoseconds.

Depending on the source of ESD transients, different specifications are chosen to classify the sensitivity levels of Integrated Circuit (IC) devices against damage from ESD events. Examples of common standards are Human Body Model (HBM), Machine Model (MM), and Charged Device Model (CDM) while emerging ESD standards include Cable Discharge Event (CDE) and System Level. The differences between the standards are the characteristics of the ESD pulse, including the voltage, current, rise time, duration, shape (including reflections), and decay time. Within a given standard ESD test method, the input voltage is used to define the device ESD sensitivity level.

Transmission Line Pulse (TLP) is a test methodology utilizing high current, fast rise time, rectangular wave, and short pulse testing for ESD characterization of ICs [1]. TLP systems consist of a high voltage power supply, which charges a coaxial cable or transmission line, a switch to discharge the cable to the device under test (DUT), and an oscilloscope to measure voltage and current across the DUT. The TLP is a rectangular pulse with specified rise and fall times. Figure 1 demonstrates a 200 V, 40 ns pulse. The pulse width can be adjusted by the length of the charging cable. Typical pulse widths range between 120 ns to less than 10 ns. The TLP is also used to characterize the EPI-FLO™ PVS devices, which will be used for ESD reliability improvement.

This project utilized both HBM and TLP ESD test methods for failure voltage characterization and ESD sensitivity improvement. Table 1 depicts the Joint Electron Devices Engineering Council (JEDEC) classification for HBM sensitivity (ESD Sensitivity Testing Human Body Model [HBM] JESD22-A114E) based on applied voltage level.

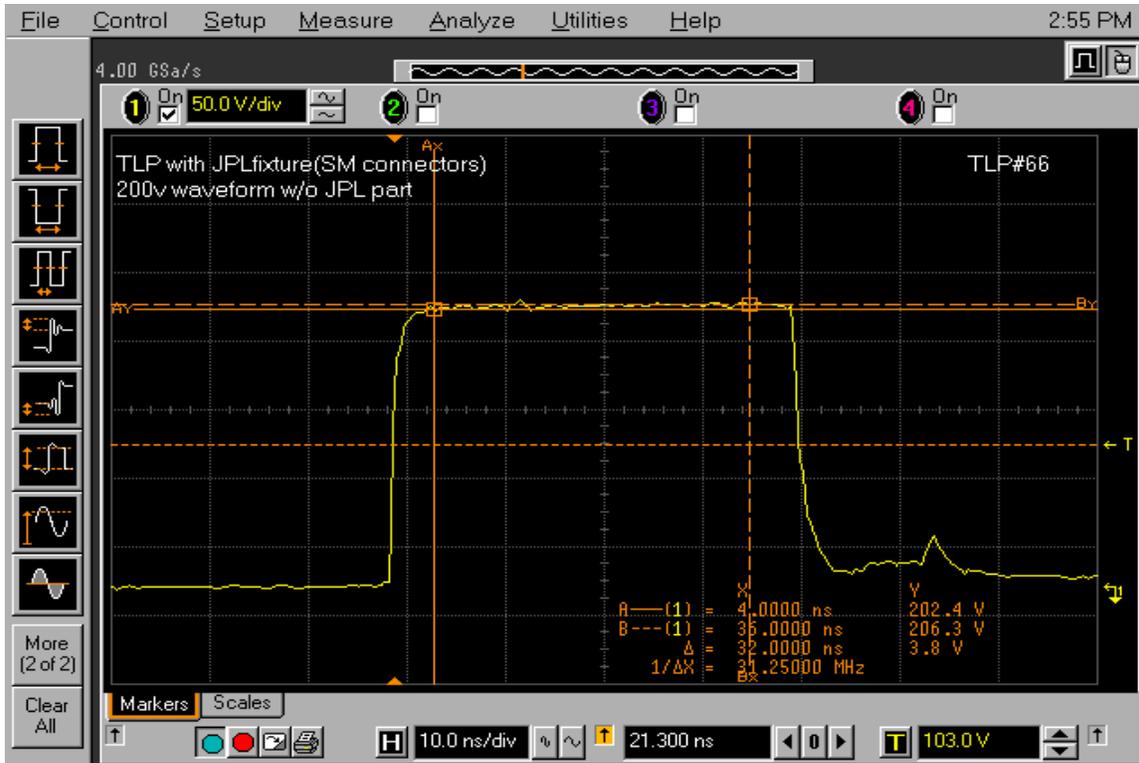


Figure 1. Waveform of 200 V, 40 ns Transmission Line Pulse (TLP), $V_{4\text{ns}} = 202.4\text{ V}$, $V_{40\text{ns}} = 206.3\text{ V}$

Table 1. JEDEC HBM ESD Sensitivity Classification Criteria

JEDEC Classification Level	Passing Voltage +/- Polarity (V)	Failure Voltage +/- Polarity (V)
Class 0	N/A	250
Class 1A	250	500
Class 1B	500	1000
Class 1C	1000	2000
Class 2	2000	4000
Class 3A	4000	8000
Class 3B	8000	N/A

2.0 EPI-FLO™ Polymer Voltage Suppression (PVS) Devices

Traditional ESD protection utilizes on-chip diodes. Today, with IC downsizing combined with faster IC speeds and higher communication bandwidths, there is an emerging need for femtofarad capacitance ESD protection. The ESD Association's ESD Technology Roadmap predicts the continuation of the current trend of circuit performance at the expense of ESD protection levels [2]. Electronic Polymers, Inc.'s (EPI's) new class of Polymer Voltage Suppression (PVS) ESD protection has demonstrated the capability to enhance ESD reliability of sensitive ICs. This is a particularly important development for high reliability environments such as command, control, and communication in military and space environments.

An EPI-FLO™ PVS device function is twofold. It is typically connected in parallel to the circuit line (to be protected) and to ground. In its passive or non-conductive state, it has very high resistance and as such is transparent to the function of the integrated circuit. In its active state, the voltage potential created from an ESD event will turn the EPI-FLO™ PVS device conductive in sub-nanoseconds and shunt the ESD event harmlessly to ground.

EPI-FLO™ PVS devices are classified by the Trigger Voltage (V_t) or the voltage at which the EPI-FLO™ PVS device begins to become conductive. Other key attributes include the residual voltage potential not shunted to ground or the clamp voltage (V_c), time to reach V_c , and capacitance.

EPI-FLO™ PVS devices can be constructed as standard surface mount devices such as 0201, 0402, or 0603 passive packages (Figure 2) and custom arrays to protect connector pins (Figures 3 and 4) [3]. A more recent application of EPI-FLO™ PVS technology is embedding the material in a Chip Scale Package (CSP) [4].

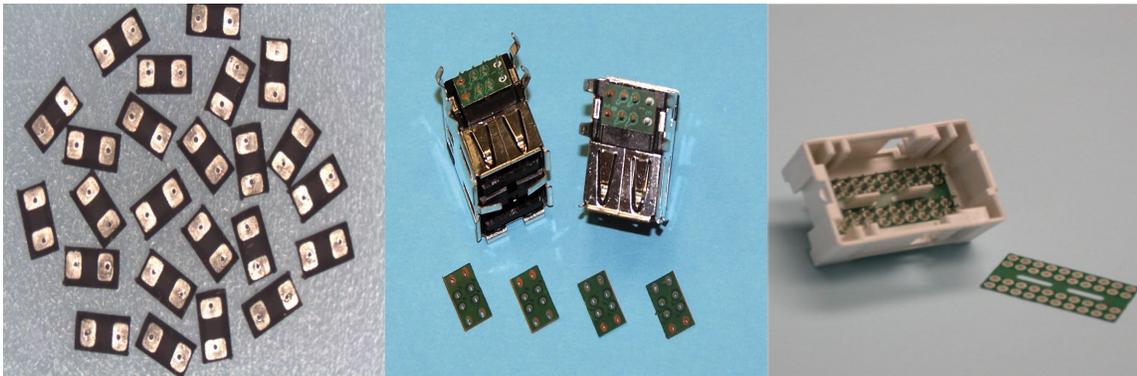


Figure 2. Surface Mount (0402)

Figure 3. Dual Port USB Connector Array

Figure 4. 40-Pin Automotive Connector Array

3.0 Project Overview

The project was comprised of four phases consisting of 1) device selection and test board design and fabrication, and test fixture build; 2) device procurement and characterization of TLP failure voltage; 3) characterization of HBM failure voltage and correlation to TLP failure voltage; and 4) selection of EPI-FLO™ PVS devices based on failure voltage characterization and demonstration of improved ESD protection.

3.1 Phase 1

Two devices were selected for evaluation as candidates based on manufacturer's supplied HBM failure test results. One device was a Silicon Germanium (SiGe) 3.5 GHz amplifier and the other was a Gallium Arsenide (GaAs) 5.0 GHz power amplifier for cell phones. Both devices were packaged in 3-mm x 3-mm, 16-pin, Plastic Quad Flatpack (PQFP). Test boards were designed and fabricated at EPI to enable soldering of the device package to the test board and to enable testing of different pin combinations via jumpers. Figure 5 shows the top layer artwork. The test board included surface mount pads so an EPI-FLO™ 0402 or 0603 could be soldered on

for Phase 4 protection. Figure 6 shows the completed test board with header pins for pin combination jumpers.

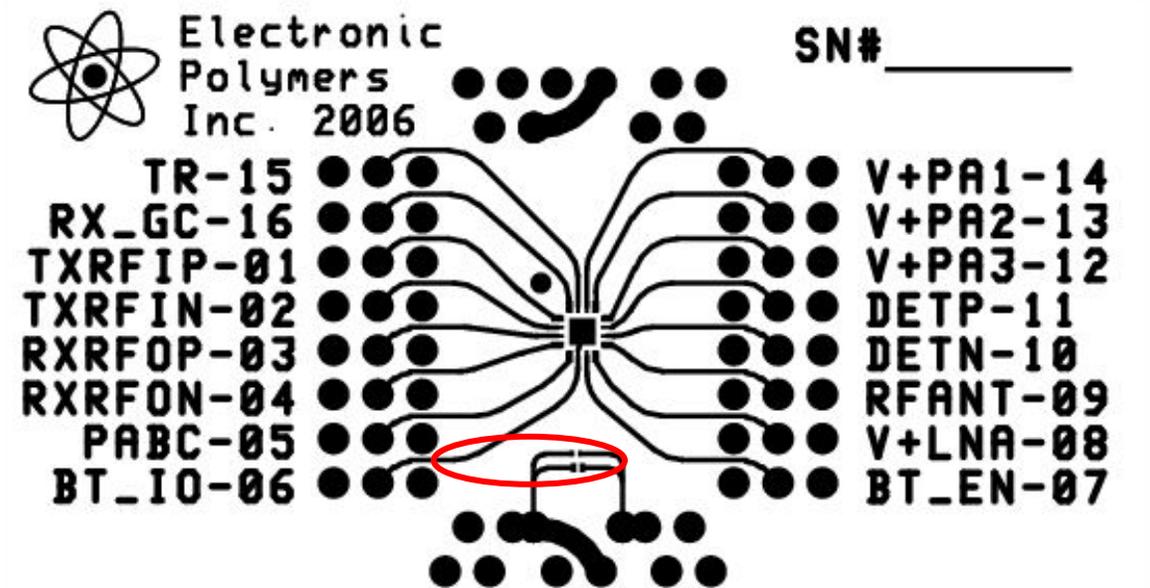


Figure 5. Test board layout for 3-mm x 3-mm, 16-pin PQFP with surface mount pads for EPI-FLO™ ESD protection in Phase 4

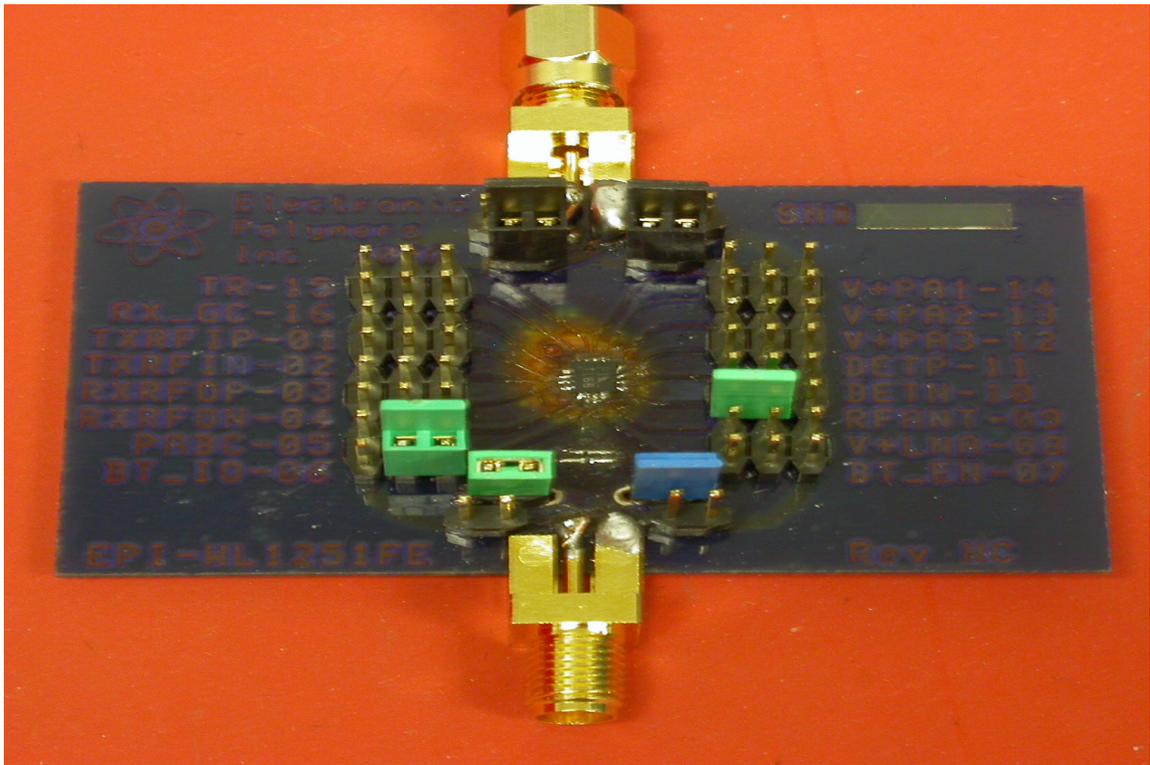


Figure 6. EPI TLP test board with SMA connectors and pin combination headers and jumpers

A test fixture was then built so the test board could be inserted into the test fixture for HBM testing. HBM direct discharge ESD testing utilized a Keytek Mini-Zap gun (Figure 7). TLP testing was accomplished using EPI's TLP model TLP-05 (Figure 8).



Figure 7. HBM ESD test gun with test board inserted in test fixture for direct discharge ESD testing

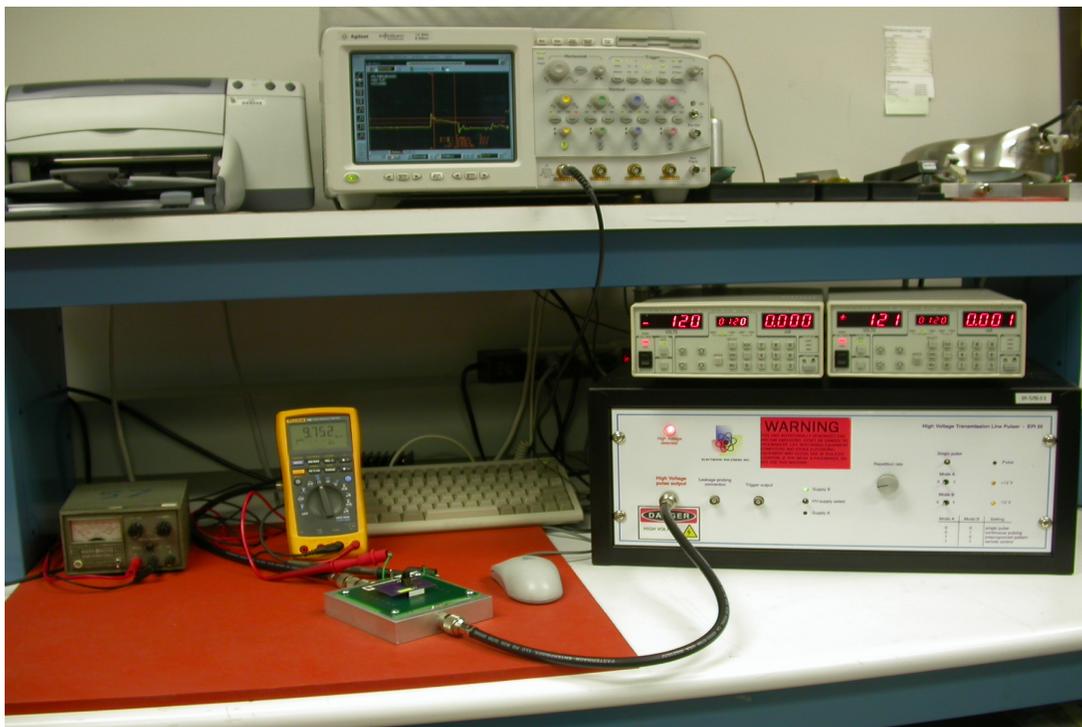


Figure 8. TLP test setup utilizing Electronic Polymers, Inc. TLP Model EPI-05

In order to determine ESD sensitivity levels, the typical EPI test protocol was used. The device was soldered to the test board and tested for shorts or opens. A pin combination was selected and the corresponding jumpers were attached across the pins. A 1.0 V dc current was applied and the leakage current was measured to obtain the pre-pulse baseline leakage current. The device was then pulsed once with either a TLP or HBM ESD pulse in positive polarity. The leakage current was then re-measured and compared with the baseline leakage current. If the leakage current changed by more than 20% from the baseline, the device was classified as ESD sensitive at that respective voltage. If the leakage current was within 20% of the baseline, the polarity was changed, the part was pulsed once, and the leakage current was re-measured. The voltage was then increased and the process was repeated, alternating polarity until the sensitivity level was obtained. As explained later, this test protocol was modified slightly to increase the pool of data for characterization, analysis, and ESD sensitivity improvement.

For TLP ESD testing scope traces are also recorded before and after ESD pulsing to enable identification of the V_t and V_c characteristics of the device.

3.2 Phase 2

A limited number of the SiGe and GaAs power amplifiers were screened for HBM and TLP failure voltages. Several pin combinations were selected for each of the devices and the initial results are summarized in Table 2.

Table 2. TLP and HBM Failure Voltage Screening Results

	HBM Failure Voltage (V)	TLP Failure Voltage (V)	HBM:TLP Failure Voltage Ratio
SiGe Device	1500–3000	50	30:1–60:1
GaAs Device	1000–1500	150–250	6:1–7:1

The SiGe device had various pin combinations failing HBM between 1500 V and 3000 V while the GaAs device had HBM failures between 1000 V and 1500 V; in both cases, this matched the manufacturers reported classifications.

Figure 9 is an example of a TLP waveform for the GaAs power amplifier at 100 V and 40 ns. After this pulse, the leakage current was measured at 1.0 V dc nominal and the part was observed to be undamaged. Figure 10 is an example of a TLP waveform for the GaAs power amplifier at 150 V and 40 ns. After this pulse, the leakage current measured greater than 20% from nominal, at 1.0 V dc; hence, the part was damaged.

In addition to the leakage current change of greater than 20%, Figure 10 also demonstrates a characteristic failure signature observed as the IC began to absorb the ESD pulse energy and break down.

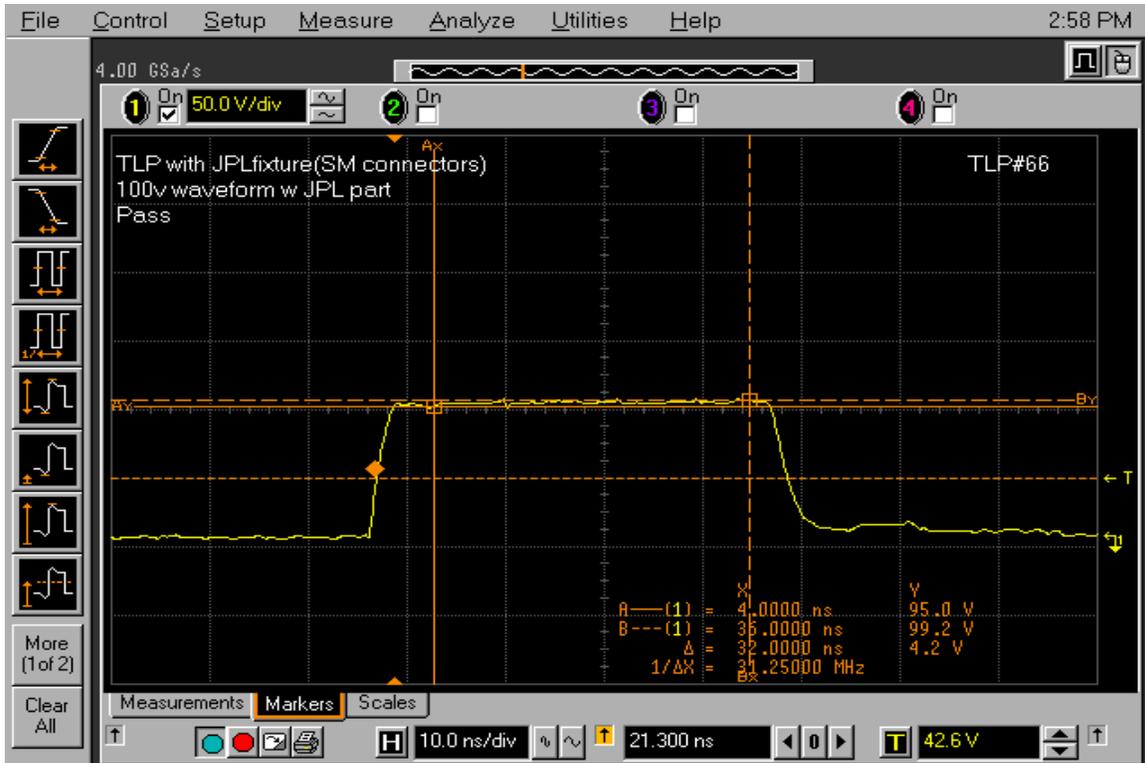


Figure 9. Waveform of 100 V, 40 ns TLP Pulse, Device Undamaged, $V_{4\text{ ns}} = 95.0\text{ V}$, $V_{40\text{ ns}} = 99.2\text{ V}$

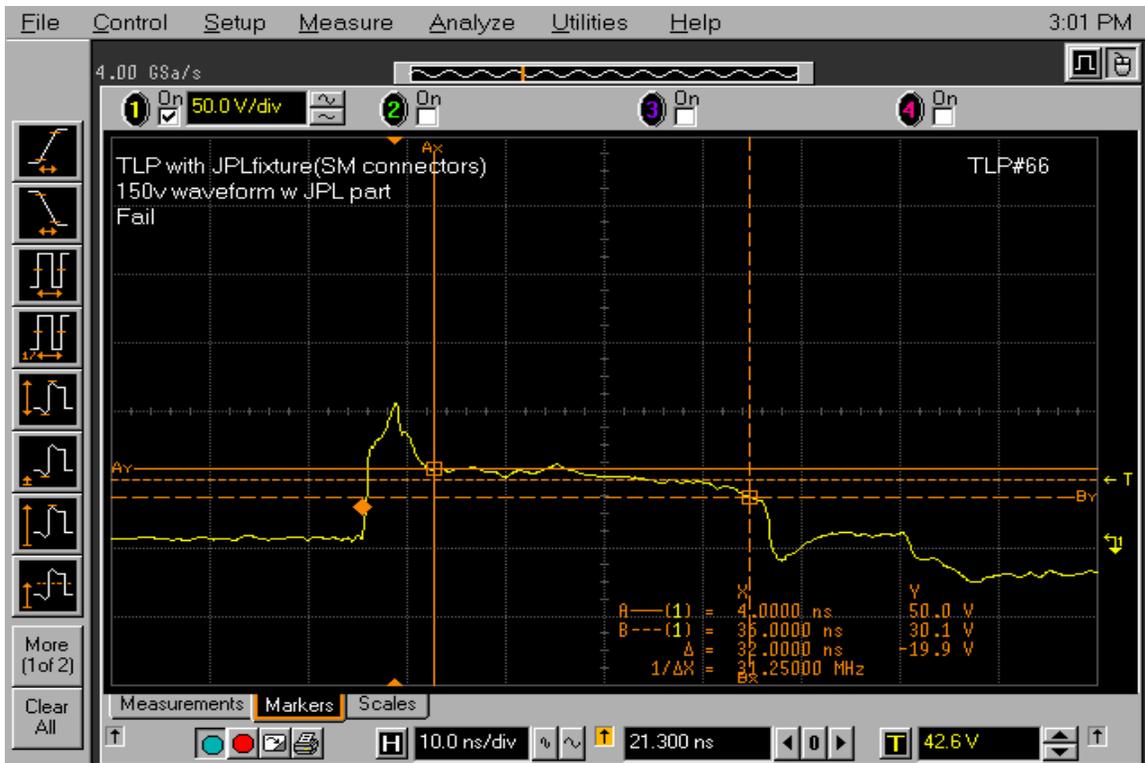


Figure 10. Waveform of 150 V, 40 ns TLP Pulse, Device Damaged, $V_{4\text{ ns}} = 50.0\text{ V}$, $V_{40\text{ ns}} = 30.1\text{ V}$

TLP testing revealed the SiGe device to be more sensitive than the GaAs device by a factor of 3–5 times. Figure 11 is a typical waveform for the SiGe device, which failed after a single 50 V pulse. This level of ESD sensitivity is likely due to smaller features inside the SiGe IC device compared to GaAs technology. Given the extreme sensitivity of the SiGe device, Phases 2, 3, and 4 were completed with the GaAs device.

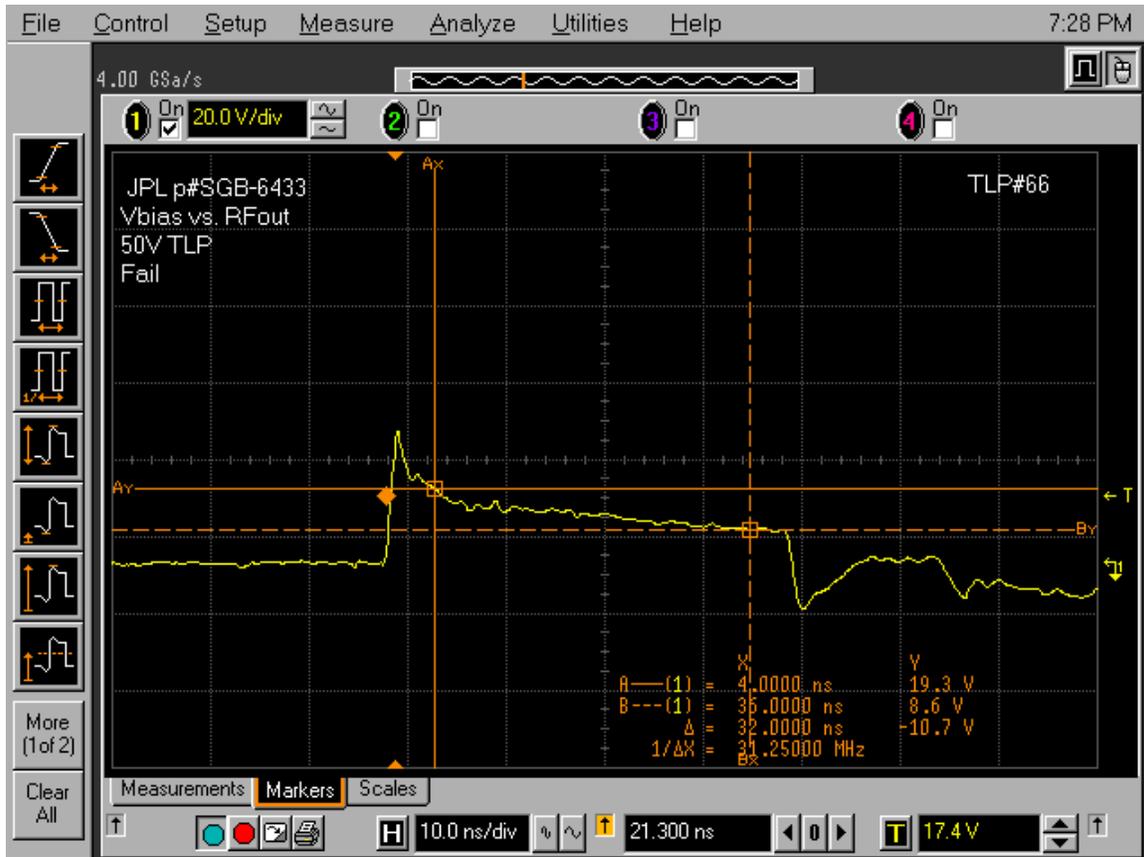


Figure 11. 50 V, 40 ns TLP Waveform on SiGe Device, $V_{4\text{ ns}} = 19.3\text{ V}$, $V_{40\text{ ns}} = 8.6\text{ V}$

TLP testing was completed on the GaAs device. The results are shown in Figure 12. It was observed that the same pin combination failed at slightly different failure voltages depending on the polarity of the pulse. Typical test protocol alternates between positive and negative polarity, but for the purposes of this study, polarity was not alternated so as to have two different sets of data on the same device.

Sample size for the baseline TLP testing was 38 devices across 15 pins, including both polarities. Typical failure voltage for TLP positive polarity was 150 V with one device failing at 200 V. Typical failure voltage for TLP negative polarity was 250 V with one device failing at 200 V and two devices failing at 150 V.

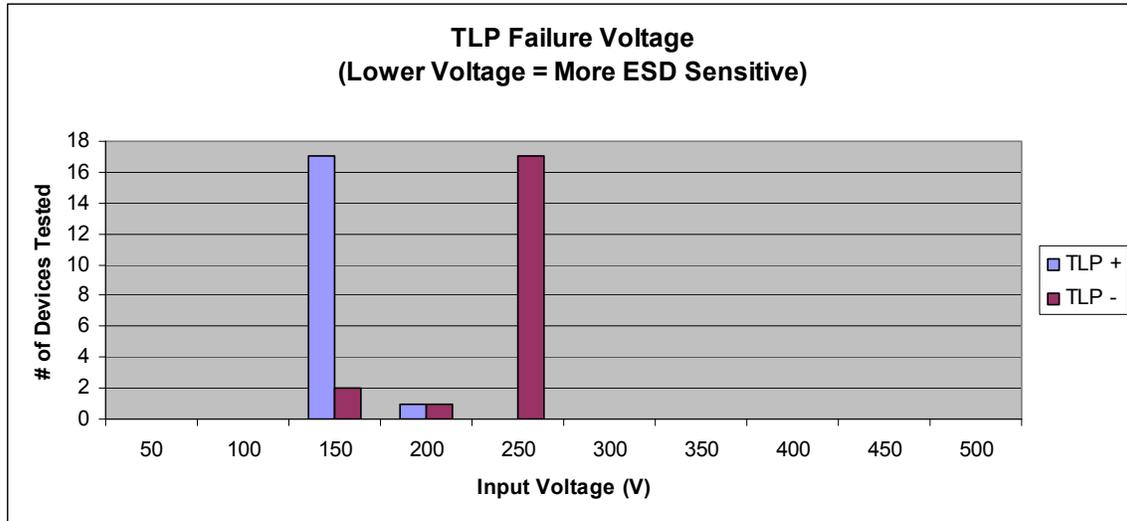


Figure 12. TLP Failure Voltages using Positive and Negative Polarity on the GaAs Device

3.3 Phase 3

HBM testing was completed on the GaAs devices. The results are shown in Figure 13. The same observation was made with HBM testing and the influence of polarity (i.e., the negative polarity failed at a higher voltage than the positive). The same rationale was used for Phase 3 as in Phase 2, testing each polarity separately so as to have two sets of data from the same device.

The pin RF Out was of interest and was tested with every other pin. The total sample size for the baseline HBM testing was 38 devices across the 15 RF Out pin combinations, including both polarities. Typical failure voltage for HBM positive polarity was 1000 V with one device failing at 500 V and three devices failing at 1500 V. Using just the positive polarity data results in a classification of the device sensitivity as HBM class between 1A and 1B.

Typical failure voltage on HBM negative polarity was 1500 V with three devices failing at 1000 V and one device failing at 2000 V. Using just the negative polarity data results in a classification of the device sensitivity as HBM Class 1B, given that 3 out of 20, or 15% of the devices failed at 1000 V.

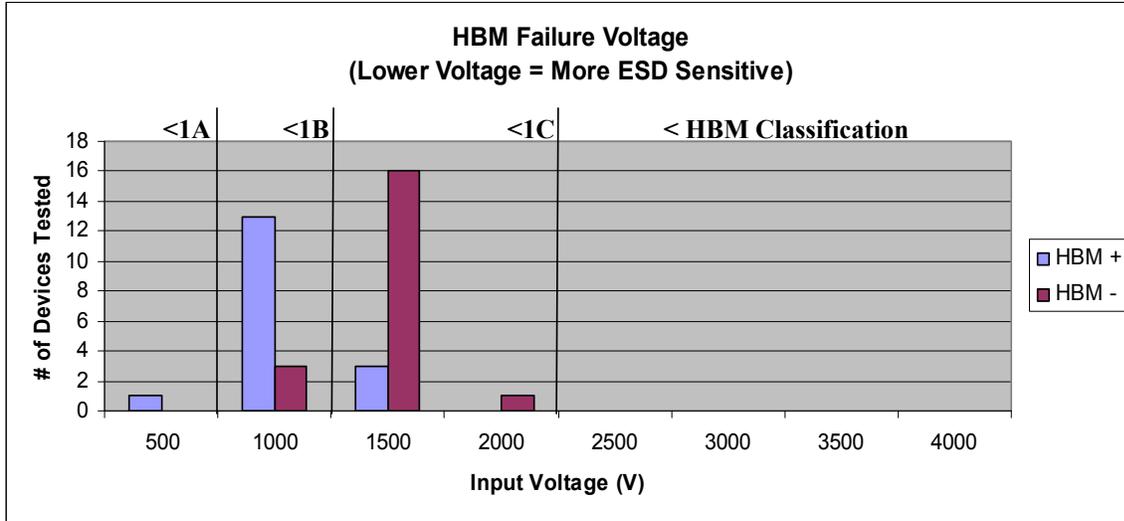


Figure 13. HBM Failure Voltages using Positive and Negative Polarity on the GaAs Device

To correlate the two test methods, the typical failure voltage found in the TLP and HBM tests was used. The results of the correlation are contained in Table 3.

Table 3. TLP and HBM Failure Voltage Screening Results

	Typical HBM Failure Voltage (V)	Typical TLP Failure Voltage (V)	HBM:TLP Failure Voltage Ratio
Positive Polarity	1000	150	6.67:1
Negative Polarity	1500	250	6.00:1

3.4 Phase 4

Phase 4 is the proof of concept milestone for the project. This phase was broken down into two rounds of protection testing. The first round protected both HBM and TLP in separate polarities to understand the characteristics required of the EPI-FLO™ PVS device to provide protection. That learning was applied to Round 2 where the HBM JEDEC protocol was introduced for final proof of concept.

Round 1

Given the TLP failure voltages found in Phase 2 where the device failed at 150 V positive polarity and 250 V negative polarity, several EPI-FLO™ PVS 0402 devices were selected for protection. In addition to selected industry-standard 0402 devices, other test vehicles were soldered to the SMT pads on the test board. These test vehicles were two metal layer, vialess, copper/ EPI-FLO™/copper laminate devices utilized by EPI to characterize the embedded CSP EPI-FLO™ PVS embodiment of the technology. This embedded technology can be utilized in the CSP for devices like the GaAs power amplifier. In both cases, protection devices were selected based on TLP-derived trigger voltages. The trigger voltages selected were between 100 V and 150 V so that the EPI device could trigger and shunt the ESD pulse to ground before device damage occurred.

Table 4 contains the results of Round 1 TLP and HBM protection improvement.

Table 4. Round 1 Protection Results

	TLP +	TLP -	HBM +	HBM -
Typical Failure Voltage Unprotected	150	250	1000	1500
Number of Protection Tests	5	11	4	2
Range of Protected Failure Voltage	200–400	200–1000	1500–3500	1000–3500
Average Protected Failure Voltage	320	377	2000	2250
Times Protection Over Typical Failure Voltage	2.1x	1.5x	2.0x	1.5x

Round 2

For Round 2 testing, the JEDEC test protocol (Table 1) was utilized with both polarities as outlined in Table 5. A baseline leakage current was taken at time zero and again after each pulse. HBM ESD pulsing continued until leakage current exceeded a 20% change over baseline levels.

Table 5. Round 2 HBM Test Protocol

Pulse Number	HBM Voltage (V) and Polarity	Pulse Number	HBM Voltage (V) and Polarity
1	500 +	2	500 -
3	1000 +	4	1000 -
5	2000 +	6	2000 -
7	4000 +	8	4000 -
9	8000 +	10	8000 -

Five additional EPI-FLO™ PVS devices were selected for HBM ESD testing and the results are contained in Table 6.

Table 6. Round 2 HBM Test Protocol

Pulse Number	HBM Voltage (V) and Polarity	HBM Class	Device Serial 101	Device Serial 102	Device Serial 103	Device Serial 104	Device Serial 105
1	500 +	1B	Pass	Pass	Pass	Pass	Pass
2	500 -	1B	Pass	Pass	Pass	Pass	Pass
3	1000 +	1C	Pass	Pass	Pass	Pass	Pass
4	1000 -	1C	Pass	Pass	Pass	Pass	Pass
5	2000 +	2	Pass	Fail	Pass	Pass	Pass
6	2000 -	2	Pass		Pass	Pass	Pass
7	4000 +	3A	Pass		Pass	Fail	Pass
8	4000 -	3A	Pass		Pass		Pass
9	8000 +	3B	Pass		Fail		Pass
10	8000 -	3B	Pass				Pass

Since HBM data collected during Phase 3 were at separate polarities and the JEDEC testing was performed with both polarities, Figure 14 depicts the positive polarity data for comparison. This is reasonable because the devices would have failed at the lower positive polarity before reaching higher damage levels in the negative polarity. ESD protection was significantly improved in four of the five cases with EPI-FLO™ PVS ESD protection devices, with three of the five passing 4000 V.

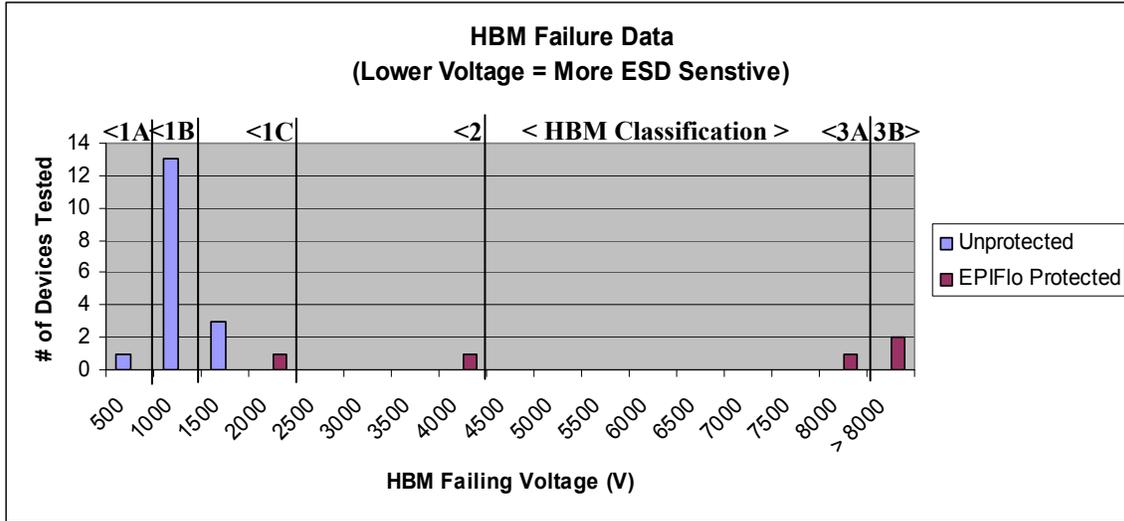


Figure 14. HBM Failure Voltage, EPI-FLO™ PVS Protected vs. Unprotected Positive Polarity

Further analysis of the EPI-FLO™ PVS devices is contained in Table 7. The devices that provided maximum protection (Serial 101 and Serial 105) had lower 4-ns and 36-ns clamping voltages than the devices that provided protection above typical failure voltages. The lower clamping voltages shunted more energy to ground, further extending improved HBM ESD protection.

Table 7. EPI-FLO™ PVS ESD Protection Device Characterization

Protection Device	Capacitance (fF)	V _t –Trigger Voltage (V)	V _{c4} –4 ns Clamp Voltage (V)	V _{c36} –36 ns Clamp Voltage (V)	HBM ESD Protection Level (V)
Serial 101	450	100	32	16	> 8000
Serial 102	550	100	48	33	1000 -
Serial 103	400	100	74	33	4000 -
Serial 104	400	100	74	33	2000 -
Serial 105	400	100	35	22	> 8000

Figure 15 contains all TLP ESD data collected for protected vs. unprotected devices for both polarities.

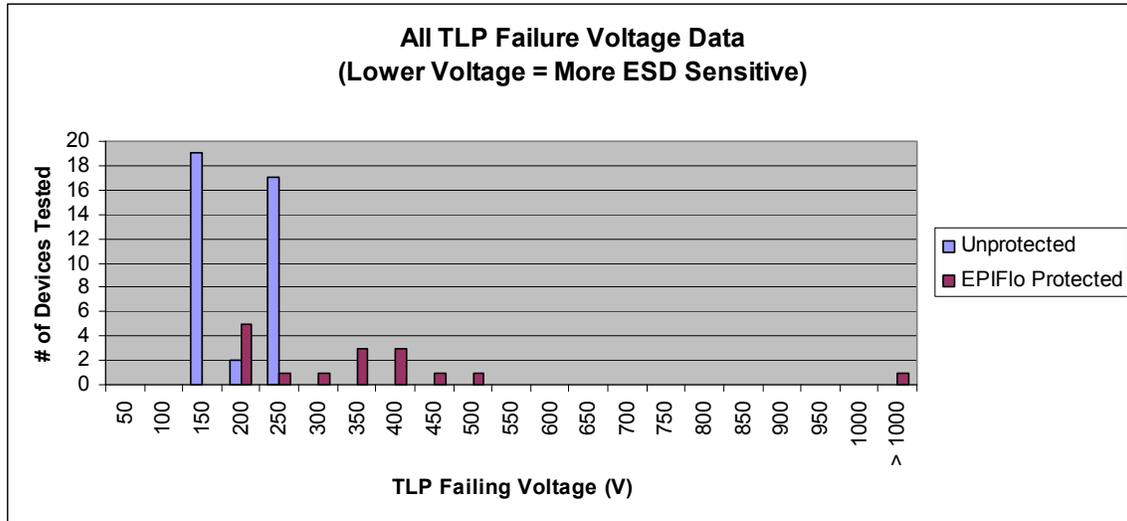


Figure 15. TLP Failure voltage, EPI-FLO™ PVS Protected vs. Unprotected (both polarities)

4.0 Summary

A GaAs power amplifier was thoroughly characterized using HBM and TLP ESD testing techniques and the HBM sensitivity level was characterized as Class 1B to 1C. Initial demonstration of proof of concept for improved ESD protection utilizing EPI-FLO™ PVS protection devices resulted in 1.5 to 2.1 times improvement.

Final demonstration of ESD protection increased a HBM Class 1B to 1C GaAs power amplifier to Class 2, 3A, and 3B. Maximum protection was achieved with 100 V trigger devices with 4-ns clamping voltages between 32 V and 35 V, and 36-ns clamping voltages between 16 V and 22 V.

Potential future work includes polymer devices with a specification for V_t of 100 V, $V_{c,4ns}$ of 20 V, and $V_{c,40ns}$ of 15 V. EPI expects this would protect most GaAs devices. Other potential work would include the embedded application of this formulation in a CSP for GaAs devices or similar devices.

References

- [1] Shrier, Karen, Tuyen Troung, and Jimmie Felps. 2004. "Transmission Line Pulse Test Methods, Test Techniques and Characterization of Low Capacitance Voltage Suppression Device for System Level Electrostatic Discharge Compliance." Proceedings of the EOS/ESD Symposium, 2A.4, 88–97.
- [2] ESD Association. 4 March 2005. *Electrostatic Discharge (ESD) Association Technology Roadmap*. <http://www.esda.org/documents/ElectrostaticDischargeRoadmap-March42004--ESDA--Final.pdf>.
- [3] Electronic Polymers, Inc. 2000. Electronic Polymers Website, EPI-FLO™ Surface Mount and Connector Array ESD Suppressors. <http://www.electronicpolymers.com>.

- [4] Shrier, Karen. 3–5 May 2005. “ESD Protection of an RF Integrated Circuit by Embedding Protection in the IC Package Printed Circuit Board.” IMAPS Workshop and Exhibition on Military, Aerospace and Homeland Security.

REPORT DOCUMENTATION PAGE

*Form Approved
OMB No. 0704-0188*

The public reporting burden for this collection of information is estimated to average 1 hour per response, including the time for reviewing instructions, searching existing data sources, gathering and maintaining the data needed, and completing and reviewing the collection of information. Send comments regarding this burden estimate or any other aspect of this collection of information, including suggestions for reducing this burden, to Department of Defense, Washington Headquarters Services, Directorate for Information Operations and Reports (0704-0188), 1215 Jefferson Davis Highway, Suite 1204, Arlington, VA 22202-4302. Respondents should be aware that notwithstanding any other provision of law, no person shall be subject to any penalty for failing to comply with a collection of information if it does not display a currently valid OMB control number.

PLEASE DO NOT RETURN YOUR FORM TO THE ABOVE ADDRESS.

1. REPORT DATE (DD-MM-YYYY) 00-08-2008		2. REPORT TYPE JPL Publication		3. DATES COVERED (From - To)	
4. TITLE AND SUBTITLE Embedded ESD Protection Proof of Concept - Final Report				5a. CONTRACT NUMBER NAS7-03001	
				5b. GRANT NUMBER	
				5c. PROGRAM ELEMENT NUMBER	
6. AUTHOR(S) Gerke, R. David, and Herrmann, Bill				5d. PROJECT NUMBER 102197	
				5e. TASK NUMBER 2.33.6	
				5f. WORK UNIT NUMBER	
7. PERFORMING ORGANIZATION NAME(S) AND ADDRESS(ES) Jet Propulsion Laboratory California Institute of Technology 4800 Oak Grove Drive Pasadena, CA 91009				8. PERFORMING ORGANIZATION REPORT NUMBER JPL Publication 08-25	
9. SPONSORING/MONITORING AGENCY NAME(S) AND ADDRESS(ES) National Aeronautics and Space Administration Washington, DC 20546-0001				10. SPONSORING/MONITOR'S ACRONYM(S) NASA	
				11. SPONSORING/MONITORING REPORT NUMBER	
12. DISTRIBUTION/AVAILABILITY STATEMENT Unclassified—Unlimited					
Subject Category 33 Electronics and Electrical Engineering					
Availability: NASA CASI (301) 621-0390 Distribution: Nonstandard					
13. SUPPLEMENTARY NOTES					
14. ABSTRACT The purpose of this project is to characterize and correlate Electrostatic Discharge (ESD) sensitivity levels of an Integrated Circuit (IC) package using Transmission Line Pulse (TLP) and Human Body Model (HBM) methods. This characterization will be used as a baseline ESD sensitivity level to demonstrate improvement to the ESD sensitivity of the IC package through the use of EPI-FLOTM Polymer Voltage Suppression (PVS) protection devices developed and manufactured by Electronic Polymers, Inc. (EPI).					
15. SUBJECT TERMS ESD					
16. SECURITY CLASSIFICATION OF:			17. LIMITATION OF ABSTRACT UU	18. NUMBER OF PAGES 19	19a. NAME OF RESPONSIBLE PERSON STI Help Desk at help@sti.nasa.gov
a. REPORT U	b. ABSTRACT U	c. THIS PAGE U			