Synopsis V1.0
SEE Test Report for the MT29F2G08B Micron NAND Flash Memory

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I. Introduction

This study was undertaken to determine the susceptibility of the Micron MT29F2G08B 2 Gbit NAND Flash memory to destructive and nondestructive single-event effects (SEE). The device was monitored for SEUs and for destructive events induced by exposing it to a heavy ion beam at Michigan State University's SEE Test Facility.

II. Devices Tested

We tested a total of 4? Micron MT29F2G08B devices marked with date code 0524. Note that with commercial devices, the same lot date code is no guarantee that the devices are from the same wafer diffusion lot or even from the same fabrication facility. However, we believe that since these devices are fabricated in the still relatively rare 90 nm feature-size technology and were supplied by the manufacturer that their provenance is traceable.

The device technology is 90 nm minimum feature size CMOS NAND Flash memory.

III. Test Facility

Facility: SEETF at the National Superconducting Cyclotron Facility, Michigan State University
Flux: (5×10^2 to $1. \times 10^5$ particles/cm^2/s).
Fluence: All tests were run to (1×10^6 p/cm^2) or until destructive or functional events occurred.

Table I: Ions/Energies and LET for this test

Ion/Energy per AMU	**Approx. LET on die (MeV•cm^2/mg)**
Xe/105	25
Xe/69.8	40

IV. Test Conditions

Test Temperature: Room Temperature for SEU, 85°C
Operating Frequency: (0-10 MHz).
Power Supply Voltage: (3.3V+10% for SEL, 3.3V and 3.3V-10% for SEU).

V. Test Methods

Because Flash technology uses different voltages and circuitry depending on the operation being performed, testing was performed for a variety of test patterns and bias and operating conditions.

Test patterns included all 0's, all 1's, checkerboard and inverse checkerboard. In general all these patterns were used until a worst-case pattern was established, and then testing was conducted using only the worst-case pattern.

Bias and operating conditions included:

1) Static/Unbiased irradiation, in which a pattern was written and verified, and then bias was removed from the part and the part was irradiated. Once the irradiation reached the desired fluence, it was stopped, bias was restored, and the memory contents were read and errors tallied.

2) Static irradiation, which was similar to unbiased irradiation, except that bias was maintained throughout irradiation of the part.

Note that these conditions provide no opportunity to monitor functional or hard failures that may occur during the irradiation.

3) Dynamic Read, in which a pattern was written to memory and verified, then subsequently read continuously during irradiation. This condition allows determination of functional, configuration and hard errors, as well as bit errors.

4) Dynamic Read/Write, which was similar to the Dynamic Read, except that a write operation is performed on each word found to be in error during the previous Read.

5) Dynamic Read/Erase/Write, which again was similar to the Dynamic Read and Read/Write, except that a word in error was first erased and then rewritten. Because the Erase uses the charge pump, it is expected that the Flash could be more vulnerable to destructive conditions during this operation.

The Block diagram for control of the DUT is shown in Figure 1. The FPGA based controller interfaces to the FLASH daughter card and to a laptop, allowing control of the FPGA and uploading of new FPGA configurations and instructions for control of the DUT. Power for the FLASH is supplied by means of a computer-controlled power supply. The National Instruments Labview interface monitors the power supply for overcurrent conditions and shuts down power to the DUT if such conditions are detected.

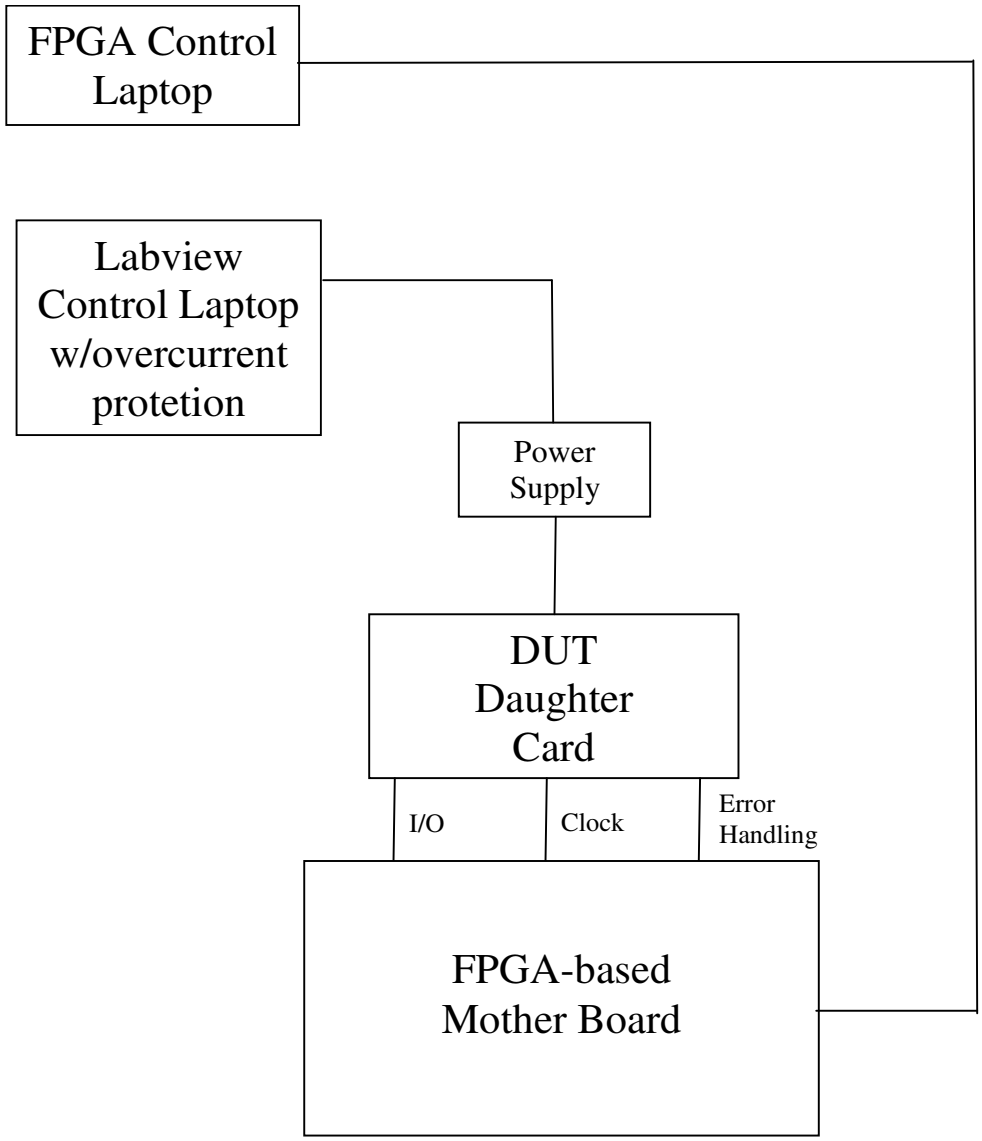

Figure 1. Overall Block Diagram for the testing of the NSC LM-117.

VI. Results

During testing, the MT29F2G08B was irradiated with a single ion, Xenon, but at multiple energies to provide a greater range of incident LETs. The DUT was oriented normal to the incident beam, and in one run at 45 degrees to the normal to yield a higher effective LET of ~40 MeV•cm^2/mg. Errors were seen for all LETs and all bias/operating conditions. Table II shows the errors observed for each test condition and each ion LET.

Table II: Summary of Error Modes vs. Bias/Operating Conditions

LET (MeVcm^2/mg)	Modes Tested	Single bit errors (cm^2)	Page errors (cm^2)	SEFI (cm^2)	Erase/Write Fail (cm^2)	Stuck bits
~25	1,2,3,4,5	1: 3.1E-5, 2: 1.6E-5, 3: 1.6E-5, 4: 1.8E-5, 5: 6.0E-6	1: >0, 2: 1.2E-7, 3: 2.4E-7, 4:not seen, 5: ??	3: 3.7e-7, 4: not seen, 5: 1.8E-6	4: 1.4E-7, 5: 3E-8	4: (TID or SEE?)
~40	5	5: >0	5: >0	5: >0	5: 1.1E-7	

In all cases, the All-0's was found to be the worst-case pattern, so after the first few runs, all subsequent runs were carried out with this pattern.

Even for the unbiased and static cases, bit errors and Page/Block errors were evident in the patterns of upsets observed. It is likely that the Page/Block errors arise due to upsets in configuration registers in the memory array. Because the rate at which errors came in could not be gauged, we could not determine exactly when a page/block error occurred, so cross sections are approximate for these error modes.

For the Dynamic Read condition, the parts showed exhibited SEFIs in addition to the bit and Page/Block errors. For Dynamic Read/Write and Dynamic Read/Erase/Write, functional failures were observed that made it impossible to Erase or Write to the memory. Page/Block and SEFI errors were not identified, but this may have been due to interference effects from the hard errors, which occurred at comparable rates. A detailed attempt to identify SEFI and Page/Block errors would have required sacrificing several additional parts, so we decided to reserve this test for a facility where greater variety in LET was more easily obtainable.

In addition to the above errors, stuck bits were seen during testing . These apparently tended to anneal rapidly (a timescale of minutes), although 3 bits seemed to be persistent. The persistence of these stuck bits beyond the time of testing could not be investigated due to the functional failure of the die on which they were observed.

VII. Recommendations

In general, devices are categorized based on heavy ion test data into one of the four following categories:

Category 1: Recommended for usage in all NASA/GSFC spaceflight applications.
Category 2: Recommended for usage in NASA/GSFC spaceflight applications, but may require mitigation techniques.
Category 3: Recommended for usage in some NASA/GSFC spaceflight applications, but requires extensive mitigation techniques or hard failure recovery mode.
Category 4: Not recommended for usage in any NASA/GSFC spaceflight applications.
Research Test Vehicle: Please contact the P.I. before utilizing this device for spaceflight applications

The Micron MT29F2G08B 2 Gbit NAND Flash memory is a Category 3 device.

VIII. Further Test Requirements

This test represents a preliminary characterization of SEE vulnerability of the Micron MT29F2G08B. Additional testing is required before these devices can be considered for space applications. A minimum qualification involves determination of threshold and cross section vs. LET curves for all of the vulnerabilities identified in this test. Such a test should involve irradiation with multiple ions and multiple LETs. Since high-energy heavy-ion irradiation facilities do not exist with such capabilities, this characterization will have to take place at a lower-energy facility and will require modification of the part (e.g by repackaging or thinning of the die for backside irradiation) so that the die can be exposed directly to the ion beam.

In prior TID testing, these devices showed some promise for applications with moderate dose levels. Additional TID testing is recommended to fully characterize TID degradation.