Total Dose Test Report for STMicroelectronics
1G NAND Flash Nonvolatile Memory

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I. Introduction

The purpose of this test was to determine the susceptibility to total ionizing radiation dose (TID) of the STMicroelectronics 1G NAND flash nonvolatile memory (part number NAND01GW3B2ANGE, Lot Date Code 0604). This test was supported by the NASA Electronics Parts and Packaging (NEPP) Program.

II. Devices Tested

The STMicroelectronics NAND Flash Memory is a non-volatile memory that uses a floating gate NAND cell. It also provides a standard interface for pin and function drop-in compatibility. We believe these parts were burned-in before leaving the factory, so it is not possible to do a controlled experiment to look at burn-in effects. In any case, there is no plan to do our own burn-in. Detailed device information is provided in Table I. The parts have 2048 blocks, up to 40 of which can be “bad,” as identified by the manufacturer. In this case, eight samples were irradiated, of which four had some bad blocks. There was also one unirradiated control device, which had no bad blocks. The parts have a nominal 3.3 V power supply, plus an internal charge pump to generate higher voltages for writing and erasing.
Table I. Device information

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<tbody>
<tr>
<td><strong>Full Part Number</strong></td>
<td>NAND01GW3B2ANGE</td>
</tr>
<tr>
<td><strong>Manufacturer:</strong></td>
<td>STMicroelectronics</td>
</tr>
<tr>
<td><strong>Lot Date Code (LDC):</strong></td>
<td>604</td>
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<tr>
<td><strong>Quantity Tested:</strong></td>
<td>9</td>
</tr>
<tr>
<td><strong>Serial Numbers of Control Sample:</strong></td>
<td>9</td>
</tr>
<tr>
<td><strong>Serial Numbers of Radiation Samples:</strong></td>
<td>1,2, 3, 4, 5, 6,7,8</td>
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<tr>
<td><strong>Part Function:</strong></td>
<td>NAND Flash Memory</td>
</tr>
<tr>
<td><strong>Part Technology:</strong></td>
<td>CMOS</td>
</tr>
<tr>
<td><strong>Case Markings:</strong></td>
<td>ST NAND01GW3B2ANGE GA02U 8G CHN 88 604</td>
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<tr>
<td><strong>Package Style:</strong></td>
<td>48 pin TSOP</td>
</tr>
<tr>
<td><strong>Test Equipment:</strong></td>
<td>Power Supply (+3.3V) Digital test board. Multimeters</td>
</tr>
<tr>
<td><strong>Test Engineer:</strong></td>
<td>M. Friendlich</td>
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<td><strong>Dose Levels (krad (Si)):</strong></td>
<td>10, 20, 30, 50, 75, and 100krads(Si) continuing in 50krads (Si) steps until functional failure.</td>
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<td><strong>Target dose rate (rad (Si)/min):</strong></td>
<td>1200-1800</td>
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III. Test Facility

Testing was at the Co-60 facility at GSFC, which is a room air source, where the pencils are raised up out of the floor, during exposures. Active dosimetry is performed, using air ionization probes. Testing is done in a step/stress manner, using a standard Pb/Al filter box. Dose rate typically varies slightly from one exposure to the next, up to 30 rads/s. Most exposures are near the maximum dose rate, as required by MIL-STD Test Method 1019.6. Time intervals for testing between exposures are also within the limits stated in 1019.6 (one hour after exposure to start electrical characterization, two hours to begin the next exposure). Parts were under DC bias during exposures, but not actively exercised.
IV. Test Procedure

The test devices were programmed with a checkerboard pattern (AA) during exposures, and biased at 3.6 V (3.3 V nominal power supply, plus 10%), but the devices were not actively exercised during exposures. Four parts were read (only) between exposures, to look for problems related to the integrity of the individual bits. The other four parts were exercised between exposures—read, erased, and written into four different patterns. The patterns were checkerboard (AA), checkerboard complement (55), all ones, and all zeroes. In each of these tests, the entire memory is read, or erased, or programmed in one operation, with the commands entered manually. There is also a dynamic test mode, where each block is read, erased, and programmed, then the next block, and so on until the entire memory is completed. There is a cache-mode read option, as well as a standard, or non-cache read option. All the reads were done using both options. A block diagram of the test apparatus is shown in Fig. 1.

Fig. 1. Block diagram of the flash memory test apparatus.
V. Results

DUTs 1-4 were tested in read-only mode, while DUTs 5-8 were exercised in all the test patterns and the dynamic mode, as described above. DUTs 1, 4, 7, and 8 had some bad blocks, while DUTs 2, 3, 5, and 6 had no bad blocks. The unirradiated control DUT also had no bad blocks. At the 10, 20, and 30 krad (SiO$_2$) exposure levels, there were no errors in any device, in any test mode, except those identified in the bad blocks prior to irradiation. At the 50 krad (SiO$_2$) exposure level, DUTs 7 and 8 would no longer erase (these are the two devices fully exercised, that had bad blocks to begin with). DUTs 5 and 6, exercised the same way, but with no bad blocks, still had no errors in any test mode. DUTs 1-4, read-only mode, had only the errors identified pre-irradiation, in DUTs 1 and 4. At the 75 krad (SiO$_2$) exposure level, DUTs 5 and 6 were exercised in all test modes, again, with no errors of any kind. DUTs 2 and 3, which had no pre-irradiation errors, did start to have errors. The number of errors varied some on successive reads, but DUT 2 had 109-161 errors in non-cache mode, and 45-61 errors with cache. DUT 3 had 2-4 errors in non-cache mode, and 1-2 with cache. There was also some variation in the number of errors from read to read on DUTs 1 and 4, but the number of radiation-induced errors (if any) was much less than the number of pre-irradiation errors. For this reason, it was difficult to draw any conclusion on these samples. At the 100 krad (SiO$_2$) exposure level, DUTs 5 and 6 had no errors in the initial read operation, but they could not be exercised because the erase function had failed. DUTs 2 and 3 had a few hundred to a few thousand errors, with generally about twice as many in non-cache mode as with cache. DUT 4, which had about 670,000 errors pre-irradiation, had a small, but definite, increase in the number of errors. On DUTs 2-4, we decided to try to erase the errors, to see if they could be reset. In all three of these devices, the erase function had failed. DUT 1 still had no increase in the pre-irradiation error count, so it was exposed again, to 150 krad (SiO$_2$). At that point, about 20,000 new errors were observed, which could not be reset, because the erase function had failed. Leakage current was monitored throughout the test. Total current during exposure was 24 mA initially, for all eight samples, or an average of 3 mA each. This current level, 3 mA per device, was confirmed for each device, when they were tested individually. At the end of the test, when the devices failed, leakage current was either 3 or 4 mA for each device. In other words, there was very little increase in standby leakage current during the exposure sequence.
VI. Recommendations

In general, devices are categorized based on heavy ion test data into one of the four following categories:

Category 1: Recommended for usage in all NASA/GSFC spaceflight applications.
Category 2: Recommended for usage in NASA/GSFC spaceflight applications, but may require mitigation techniques.
Category 3: Recommended for usage in some NASA/GSFC spaceflight applications, but requires extensive mitigation techniques or hard failure recovery mode.
Category 4: Not recommended for usage in any NASA/GSFC spaceflight applications.

Research Test Vehicle: Please contact the P.I. before utilizing this device for spaceflight applications.

The STMicroelectronics NAND01GW3B2ANGE NAND flash has not yet been characterized for Single Event Effects (SEE). It is expected to be Category 3, when more complete data is available.