Total Dose Test Report for Freescale 4M MRAM (Magnetoresistive RAM) Nonvolatile Memory

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I. Introduction

The purpose of this test was to determine the susceptibility to total ionizing radiation dose (TID) of the Freescale 4M MRAM nonvolatile memory (part number MR2A16A, LDC 0629). The same part was also tested with protons, with the most significant results being attributed to TID. These tests were supported by the NASA Electronics Parts and Packaging (NEPP) Program.

II. Devices Tested

The MRAM is a non-volatile memory that uses a cell with a toggled magnetic tunnel junction (MTJ) [ref]. It is intended as a replacement for a 4M EEPROM, and has the same pin assignments. We believe these parts were burned-in before leaving the factory, so it is not possible to do a controlled experiment to look at burn-in effects. In any case, there is no plan to do our own burn-in. detailed device information is provided in Table I. In this case, five samples were irradiated. There was also one unirradiated control device. The parts have a nominal 3.3 V power supply.

Generic Part Number:	
Full Part Number	MR2A16A
Manufacturer:	Freescale
Lot Date Code (LDC):	0629
Quantity Tested:	6
Serial Numbers of Control Sample:	1
Serial Numbers of Radiation Samples:	2, 3, 4, 5, 6
Part Function:	Magnetoresistive memory
Part Technology:	CMOS
Case Markings:	MR2A16ATS35 CUOYAN0629
Package Style:	44 pin TSOP
Test Equipment:	Power Supply (+3.3V) Digital test board. Multimeters
Test Engineer:	M. Friendlich, A. Pham
Dose Levels (krad (Si)):	To failure
Target dose rate (rad (Si)/min):	30 rads/sec

Table I. Device information

III. Test Facility

The primary test was at the Co-60 facility at GSFC, which is a room air source, where the pencils are raised up out of the floor, during exposures. Active dosimetry is performed, using air ionization probes. Testing is done in a step/stress manner, using a standard Pb/Al filter box. Dose rate typically varies slightly from one exposure to the next, up to 30 rads/s. Most exposures are near the maximum dose rate, as required by MIL-STD Test Method 1019.7. Time intervals for testing between exposures are also within the limits stated in 1019.7 (one hour after exposure to start electrical characterization, two hours to begin the next exposure). Parts were under DC bias during exposures, but not actively exercised.

The other test was performed at IUCF (Indiana University Cyclotron Facility), using 89 and 189 MeV protons. There were a total of 18 exposures, with fluences ranging from 2E10 to 1E11 particles/cm^2.

IV. Test Procedure

The test devices were programmed with a checkerboard pattern (AA) during exposures, and biased at 3.6 V (3.3 V nominal power supply, plus 10%), but the devices were not actively exercised during exposures. Two parts were read (only) between exposures, to look for problems related to the integrity of the individual bits. The other three parts were exercised between exposures—read, erased, and written into four different patterns. The patterns were checkerboard (AA), checkerboard complement (55), all ones, and all zeroes. In each of these tests, the entire memory is read, or erased, or programmed in one operation, with the commands entered manually. There is also a dynamic test mode, where each block is read, erased, and programmed, then the next block, and so on until the entire memory is completed. A block diagram of the test apparatus is shown in Fig. 1.

In the proton tests, the parts were biased at 3.3 V, with a checkerboard pattern (AA) stored. There were three test modes, static, dynamic, and read/modify/write. In the static mode, a pattern is stored, but the DUT is not actively exercised during exposure. After the exposure, the pattern is read, and errors counted. In the dynamic mode, the pattern is read continuously during the exposure. The purpose of this test is to detect errors induced by transient noise in the read circuit. Read/modify/write is similar to the dynamic mode described above, except that the proton beam is on.

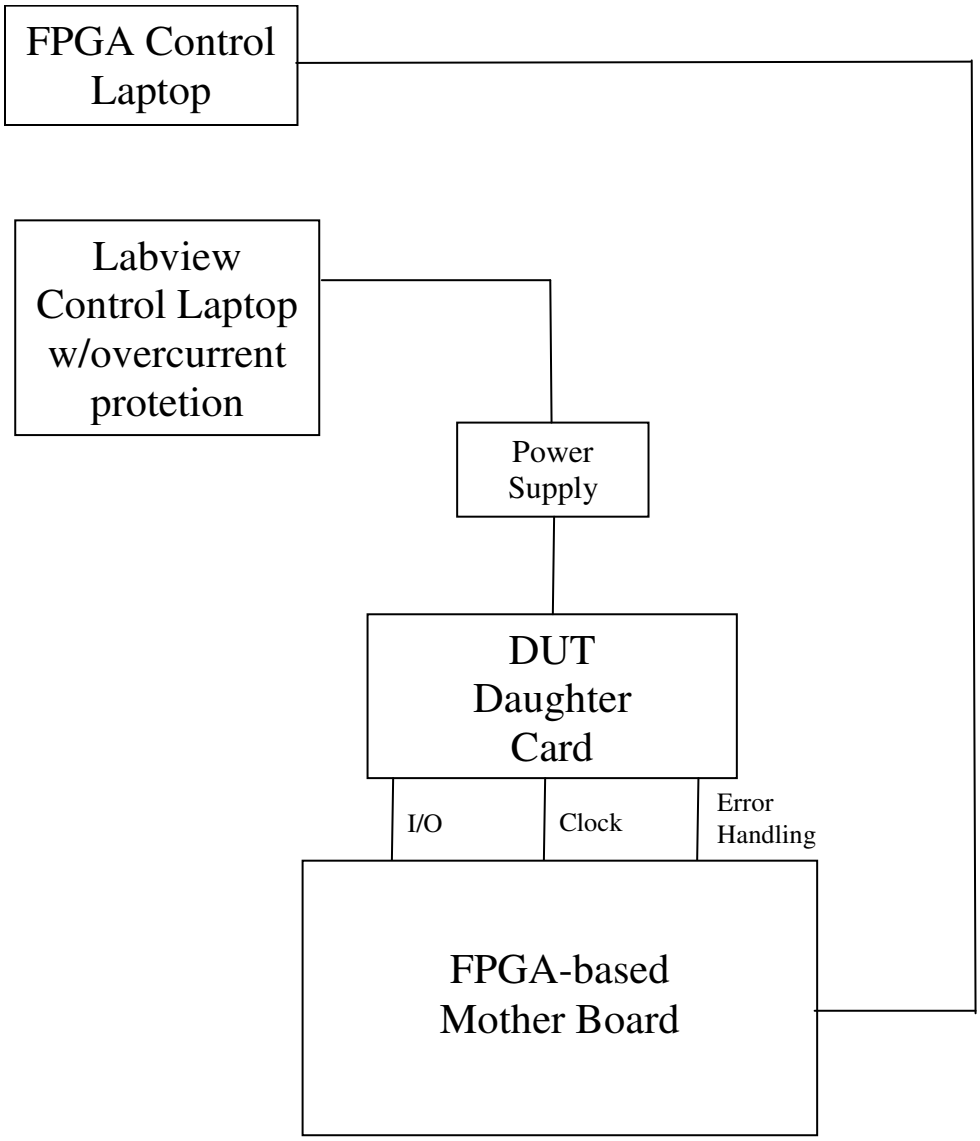

Fig. 1. Block diagram of the flash memory test apparatus.

V. Results

DUTs 1-2 were tested in read-only mode, while DUTs 3-5 were exercised in all the test patterns and the dynamic mode, as described above. Up to the 90 krad (SiO_2) exposure level, there were no errors in any device, in any test mode. The power supply current was between 8.5 and 9.0 mA for all samples prior to the first radiation exposure. The power supply current had increased by 1-1.5 mA per device at the 90 krad level, but there was no other indication of any radiation damage. At the 100 krad (SiO_2) exposure level, DUTs 1 and 2 (read only) had one bit error, and none, respectively. DUTs 3-5 (exercised) had 29,2, and 1 bit errors in the initial read, respectively. When these DUTs were programmed with other patterns, DUT 5 had one error for the 00 pattern, but none in any other pattern, including when AA was restored. DUT 4 had one error in 00, and one error when AA was restored. DUT 3 had 33-522 errors, depending on the pattern, including 81 when AA was restored. These errors are likely due to damage to the

control circuits, rather than to the magnetic bits, because the error count went up when the control circuits were activated. DUT 3 could have been removed from the test at this point, on the grounds that it had failed, but it was left in the test to see how much the error count would increase with additional dose. Power supply current ranged from 11.8 mA (DUT 4) to 13.0 mA (DUT 1). DUT 3, with the most errors, was 12.5 mA. At the 110 krad (SiO_2) exposure level, all five DUTs had errors in the initial read. DUTs 1 and 2 had 113 and 7 errors, respectively. DUTs 3-5 had 681, 979, and 8 errors, respectively, in the initial read. The error count was generally either higher or lower for other patterns. DUT 3 had from 272 errors to 63,672, depending on the pattern, with 815 when AA was restored. DUT 4 had 145-1754 errors, with 1031 when AA was restored. DUT 5 had 6 errors when AA was restored, up to 189. Power supply current ranged from 14.6-16.8 mA. At this point, all five DUTs could be considered to have failed, and the test could have been terminated. However, we decided to give the parts one more increment of dose to see how many more errors occurred at the next level. At 120 krads (SiO_2), DUT 1 805 errors, compared to 113 previously. DUT 2 had 61, compared to 7. DUT 3 had 62,188, which is about the same as previously, but the minimum for any pattern was 1054, compared to 274. DUT 4 had 3088, compared to 979. DUT 5 had 37 errors, compared to eight previously. The three exercised DUTs also had 298 to 13,838 errors in the dynamic SEU mode. Power supply current actually went down in some cases, ranging from 12.7 to 16.0 mA.

In the proton tests, there were no errors in any test mode, with three exceptions. In the first of these cases, there were many errors which could not be reset without cycling power to the whole test board. The results were attributed to interactions of scattered secondary particles with the FPGA. In the other two cases, the DUTs experienced functional failure, and had to be replaced. TID damage was suspected. The parts were monitored for latchup (SEL) during the tests. No SEL was observed, but the parts were not at high temperature or high voltage during the test.

VI. Recommendations

The first errors occurred between 90-100 krads (SiO_2), which can be taken as the failure level, in general. While error correction, or other work-arounds, might be used to correct a few bits, and extend the life of the chips, the error count increases rapidly with dose after the first errors are observed. Even heroic measures would only extend the life of the chips by 10-20%, which is not significant, given the other uncertainties yet to be addressed. NASA systems often have 50 krads as the system specification, and a 2x margin (to 100 krads) is desirable. This Freescale MRAM comes close in this test. If the test were repeated at lower dose rates, which are typical in space, the parts would have more time to recover during the exposure, and they would probably meet the 100 krad level, perhaps with a wide margin. For this reason, the initial TID response of these parts is encouraging for NASA applications, but further testing at low dose rate should be done. But the parts cannot be recommended for NASA applications until the SEE (Single Event Effects) response is also determined, which has not been done yet. It is expected that the magnetic storage element will be highly resistant to SEE, and that the circuit sensitivity will be that of the CMOS peripheral circuits, but further testing is required to demonstrate this.