

Total Dose Test Report for Micron
4G NAND Flash Nonvolatile Memory

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I. Introduction

The purpose of this test was to determine the susceptibility to total ionizing radiation dose (TID) of the Micron 4G NAND flash nonvolatile memory (part number MT29F4G08AAAWP, Lot Date Code 748). This test was supported by the NASA MMS (Magnetosphere MultiScale) Program.

II. Devices Tested

The Micron NAND Flash Memory is a non-volatile memory that uses a floating gate NAND cell, implemented in 73 nm technology. It also provides a standard interface for pin and functional drop-in compatibility. We believe these parts were burned-in before leaving the factory, so it is not possible to do a controlled experiment to look at burn-in effects. In any case, there is no plan to do our own burn-in. Detailed device information is provided in Table I. The parts have 4K blocks, a few of which can be “bad,” as identified by the manufacturer. The blocks are 128Kx8, with 64 pages, each 2Kx8. In this case, nine samples were irradiated, all of which had some bad blocks. There was also one unirradiated control device. The parts have a nominal 3.3 V power supply, plus an internal charge pump to generate higher voltages for writing and erasing. Error correction was not used during the test, but, in general, it is recommended by the manufacturer.

Generic Part Number:	
Full Part Number	MT29F4G08AAAWP
Manufacturer:	Micron
Lot Date Code (LDC):	0748
Quantity Tested:	9
Serial Numbers of Control Sample:	10
Serial Numbers of Radiation Samples:	1-9
Part Function:	NAND Flash Memory
Part Technology:	CMOS
Case Markings:	
Package Style:	48 pin TSOP
Test Equipment:	Power Supply (+3.3V) Digital test board. Multimeters
Test Engineer:	M. Friendlich
Dose Levels (krad (Si)):	10, 20, 30, 50, 75, and 100krads(Si) continuing in 50krads (Si) steps until functional failure.
Target dose rate (rad (Si)/min):	1200-1800

Table I. Device information

III. Test Facility

Testing was at the Co-60 facility at GSFC, which is a room air source, where the pencils are raised up out of the floor, during exposures. Active dosimetry is performed, using air ionization probes. Testing is done in a step/stress manner, using a standard Pb/Al filter

box. Dose rate typically varies slightly from one exposure to the next, up to 30 rads/s. Most exposures are near the maximum dose rate, as required by MIL-STD Test Method 1019.6. Time intervals for testing between exposures are also within the limits stated in 1019.6 (one hour after exposure to start electrical characterization, two hours to begin the next exposure). Parts were under DC bias during exposures, but not actively exercised.

IV. Test Procedure

The test devices were programmed with a checkerboard pattern (AA) during exposures, and biased at 3.6 V (3.3 V nominal power supply, plus 10%), but the devices were not actively exercised during exposures. Four parts were read (only) between exposures, to look for problems related to the integrity of the individual bits. The other five parts were exercised between exposures—read, erased, and written into four different patterns. The patterns were checkerboard (AA), checkerboard complement (55), all ones, and all zeroes. In each of these tests, the entire memory is read, or erased, or programmed in one operation, with the commands entered manually. There is also a dynamic test mode, where each block is read, erased, and programmed, then the next block, and so on until the entire memory is completed. A block diagram of the test apparatus is shown in Fig. 1.

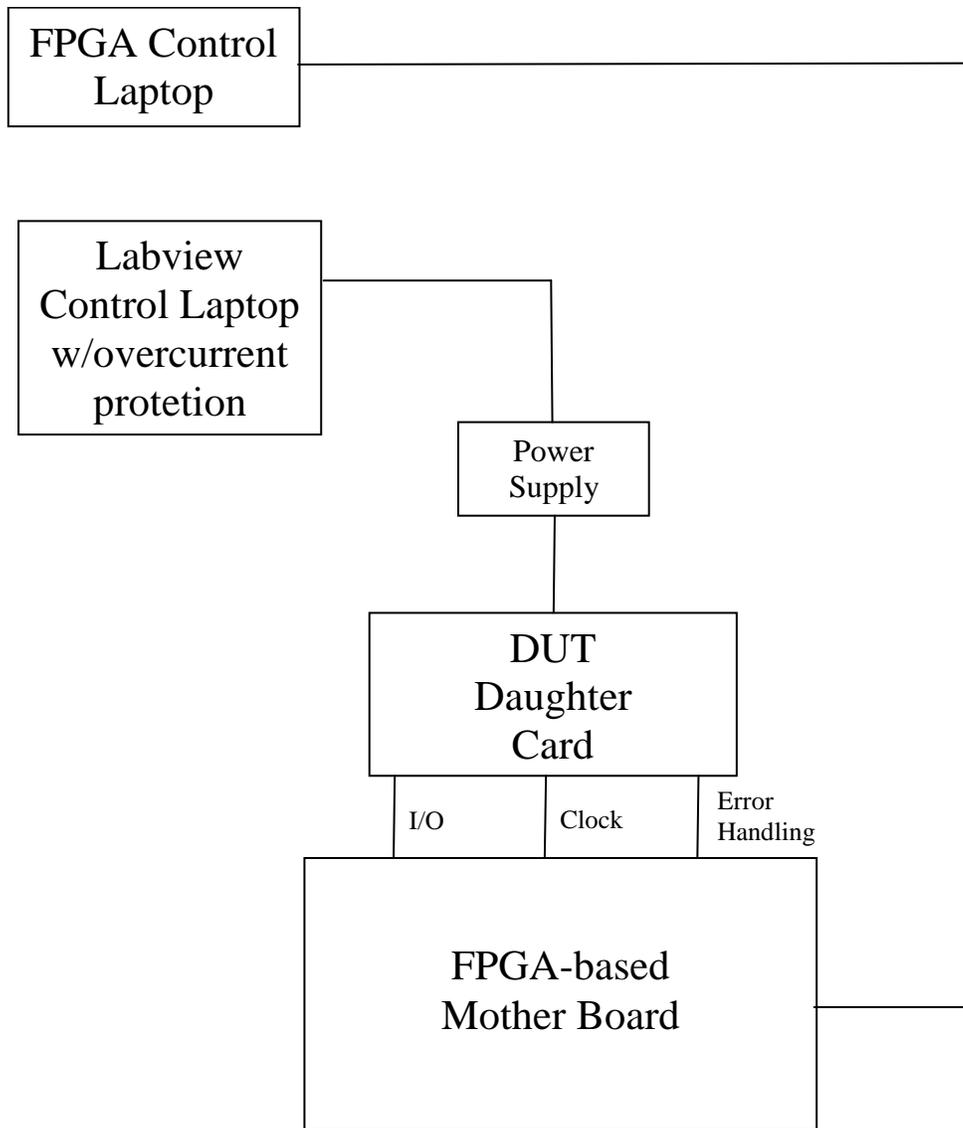


Fig. 1. Block diagram of the flash memory test apparatus.

V. Results

DUTs 1-4 were tested in read-only mode, while DUTs 5-9 were exercised in all the test patterns and the dynamic mode, as described above. All the DUTs had some bad blocks, which were screened out. Up to, and including the 65 krad (SiO_2) exposure, there were no errors in any of the DUTs, in any test mode. This exposure level is already well above the system requirement, so the parts are considered to have passed. However, the test was continued for a while, to determine where the parts would begin to fail. At the 70 krad (SiO_2) exposure, DUT 2 (read-only) had 16 errors in non-cache mode, and one error with cache. DUT 4 (also read only) had five errors, in both cache and non-cache modes. These errors were not reset at this point. Of the exercised parts, DUT 5 had one new bad block, which was detected in all patterns. DUT 6 had no errors in the initial read, but had 126 M errors when the AA pattern was rewritten later. These errors were successfully

reset, and did not recur. DUT 6 also had 2048 errors in the dynamic SEU mode, observed for the first time, which were not always observed on subsequent shots.

At the 80 krad (SiO₂) level, of the read-only devices DUT 2 had a few more errors, 13 cache mode and 17 non-cache mode. DUT 4 also had more errors, 70 and 8 errors respectively. In addition, DUT 3 appeared to have one new bad block. None of these parts were reset at this point. Of the exercised parts, DUT 5 appeared to have two bad blocks, one more than on the previous exposure. DUT 7 had three bad blocks, but there were no errors on the other three DUTs.

At the 90 krad (SiO₂) level, for the read-only devices, DUT 2 had 167 and 144 errors, non-cache and cache modes, respectively. Similarly, DUT 4 had 742 and 702 errors. DUT 3 had an additional bad block, for a total of two. At this point, these errors were reset successfully, except for the bad blocks on DUT 3. For the exercised parts, DUT 5 continued to have two bad blocks, and DUT 7 had two more, for a total of five bad blocks. In addition, DUT 9 had 2048 errors in the dynamic SEU mode, which did not recur at the next exposure.

At 100 krad (SiO₂), for the read-only parts, DUT 3 had yet another bad block, for a total of three. DUT 4 had seven errors in non-cache mode (only). Again, the bad blocks could not be reset, but the other errors were reset successfully. For the exercised parts, DUT 5 continued to have two bad blocks. DUT 7 had one more bad block, for a total of six. In addition, DUT 8 had two bad blocks.

At 110 krad (SiO₂), for the read-only parts, DUT 3 had only two bad blocks, one less than the previous exposure. In addition, DUT 4 had one bad block, for the first time. For the exercised parts, all the DUT had at least one bad block: two for DUT 5; one for DUT 6; only four for DUT 7, two fewer than before; three for DUT 8; and two for DUT 9.

At 120 krad (SiO₂), only DUT 1 still had no errors at all. For the read-only parts, DUT 2 had one bad block, and DUTs 3 and 4 each had two. For the exercised parts, DUT 5 had one bad block; DUT 6 had two initially, although one seemed to reset; DUT 7 had three; DUT 8 had five; and DUT 9 had two.

At 130 krad (SiO₂), for the read-only devices, DUT 1 continued with no errors, and DUTs 2-4 each had two bad blocks. For the exercised parts, DUT 5 had one bad block. DUT 6 this time had none—the other block also reset. DUT 7 had four bad blocks: DUT 8 had five; and DUT 9 had one.

At 140 krad (SiO₂), for the read-only parts, DUT 1 had no errors, DUT 2 had four bad blocks, and DUT 4 had three. DUT 3 had no bad blocks, but there were 1004 single bit errors in cache mode, and 1017 without cache. These errors reset successfully. For the exercised parts, DUTs 5, 7 and 9 had one bad block, each. DUT 6 had two, and DUT 8 had five.

At 150 krad (SiO₂), for the read-only devices, DUT 1 had no errors. DUTs 2 and 4 had three bad blocks, and DUT 3 had one. For the exercised parts, DUTs 5, 7, and 9 had one bad block each. DUTs 6 and 8 each had three bad blocks.

At 160 krad (SiO₂), for the read-only parts DUT 1 started to have errors: 14 single bits without cache, 13 with cache. These errors were not reset at this point. DUTs 2 and 4 had two bad blocks, and DUT 3 had one. For the exercised parts, DUTs 5, 7, and 9 still had one bad block, each. DUTs 6 and 8 still had three bad blocks, each.

At 170 krad (SiO₂), DUT 1 had more errors, 524 without cache, and 439 with cache. DUTs 2 and 4 had two bad blocks, each, and DUT 3 had one. For the exercised parts, DUT 5 had one bad block. DUT 6 had three bad blocks. DUT 7 had two bad blocks in the initial read, but many more errors occurred when other patterns were written, with some variation with the pattern. The largest error count was 1.8 M, when the original AA pattern was rewritten after exercising the other patterns. The erase function seemed to be successful, each time, but errors occurred with the write operation. DUT 7 was left in the test, but the error count continued to increase with additional exposures. For this reason, it could have been declared to have failed at this point, and removed from the test. DUT 8 had three bad blocks, and DUT 9 had no errors at all.

At 180 krad (SiO₂), for the read only parts, DUT 1 had 1830 errors without cache, and 1623 with cache. DUTs 2 and 4 had two bad blocks, each. DUT 3 had no errors—the one block bad previously had apparently recovered. For the exercised parts, DUT 5 had one bad block. DUTs 6 and 8 had three bad blocks, each. DUT 7 had more errors, up to 3 M, depending on the pattern. DUT 9 had no errors, again.

At 190 krad (SiO₂), for the read-only devices, DUT 1 had 8881 errors without cache, and 8190 with cache. DUTs 2 and 3 each had two bad blocks. DUT 4 had one bad block, when read with cache, but only 2048 errors when read without cache. We note that 2048 addresses is the page width, so the block error is probably detected as only a page error in this case. The reason for this difference is unclear. For the exercised parts, DUT 5 had one bad block, and DUTs 6 and 8 had three bad blocks, each. DUT 7 had more than 6M errors. DUT 9 had no errors.

At 200 krad (SiO₂), DUT 1 had two bad blocks, its first block errors. DUTs 2 and 4 each had one bad block. DUT 3 had no errors, which is the second time it has appeared to recover. For the exercised parts, DUT 5 had one bad block. DUT 6 had three bad blocks, and DUT 8 had two. DUT 9 still had no errors. DUT 7 had as many as 18M, depending on the pattern, which makes it still the only clear failure of the nine parts tested. After this exposure, the test was stopped, because the test equipment had to be shipped to TAMU for the SEE test. Because the parts had already passed the system requirement, we decided there was no point to resuming the test later.

However, one additional measurement was performed, about three weeks after the test, to check for annealing effects. The general result was that annealing did not appear to be significant. DUT 1 had 85K errors in the initial read without cache, and 79K with cache.

These errors all reset. DUTs 2 and 4 each had one bad block, which did not reset. DUT 3 had no errors. For the exercised parts, DUT 5 had one bad block, still. DUT 6 had three bad blocks. DUT 7 had had up to 15M errors, slightly fewer than the last previous result. DUT 8 had two bad blocks, and DUT 9 had no errors. These results are almost the same as the previous results. We had previously tested other Micron parts (same part number as here, but different LDC) at both high dose rate and low dose rate, to look for annealing effects. In those tests, there was virtually no difference in failure levels at the different dose rates, which also indicates minimal annealing effects.

VI. Recommendations

The TID response of the Micron 4G NAND flash memory (MT29F4G08AAAWP) is extremely good. There were no errors at all up to 65 krad (SiO₂), and no functional failures until 170 krad (SiO₂), which is well beyond the requirements of most NASA systems, including MMS. Indeed eight of nine DUTs had only a few block errors, which could be screened out. They were still within the manufacturer's specification for bad blocks at 200 krad (SiO₂) when the test was terminated. We note that the charge pump circuit was still working in eight of the nine parts tested, and its failure is what had limited the TID response in nearly every other flash memory test we had ever performed.

This part has also been tested for SEE, and significant destructive SEE effects have been reported, so it cannot be recommended for space applications, despite the favorable TID response observed here.