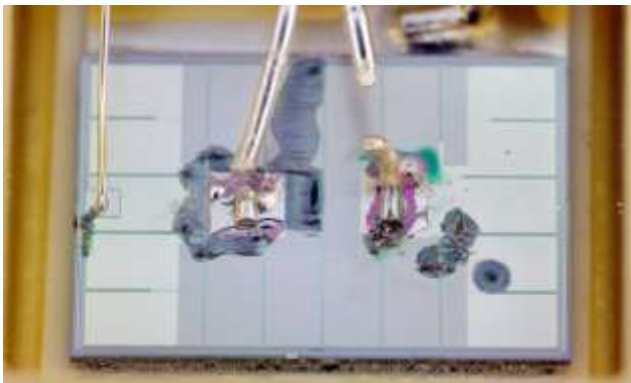




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## A Look at Failure: Noise leads to overstress



*Power Transistor – logic fault caused by electrical noise which resulted in shoot-through current in the drive circuit and massive electrical overstress damage.*

## To Catch a Counterfeit

One of the first steps in the implementation of a Counterfeit Electronic Parts Control Plan is managing parts availability, but this can be problematic for Aerospace/DoD products that may use proven, heritage designs, or whose life cycle may be decades long compared to the relatively short life cycle of the devices installed inside these products.

In these instances, redesign with newer, readily available devices is the best option, but not often practical from a schedule or cost standpoint.

These constraints compel the Parts Engineer to specify hard-to-find or obsolete components that may only be available on the open market or through independent distributors—but those sources must only be used as a last resort because the risk of receiving fraudulent or counterfeit parts is much greater when venturing outside traditional, better protected supply channels.

This does not mean procuring authentic parts is impossible, but additional risk mitigation processes must be followed when this acquisition process is pursued.

Consider this actual, recent event:

A user purchases electronic devices from independent distribution and subjects them to an industry-recognized, triple-tiered inspection process for counterfeit detection.

Tier 1: Inspection consists of a manufacturer data sheet review, visual inspection and marking permanency tests.

Tier 2: De-capsulation and inspection verifies the die matches the manufacturer's data.

Tier 3: I/O characterization electrical tests are compared with those of a known good device.

The user authorizes the distributor to ship devices that pass tier level tests, and as part of their internal receiving process sends the device manufacturer images of the device markings to confirm Lot and Date Codes.

The manufacturer confirms the Lot Code, but doesn't confirm the Date Code. Why? Because it's discovered the Date Code markings correspond to a date several years after the last manufacturing date—but it appears the package wasn't remarked. The parts are declared *suspect counterfeit* and scrapped by the user.

This event leads one to the following minimum number of questions:

1. What can the user (or supplier) do to ensure against a recurrence of this type of event?
2. Does the user have or should the user consider any recourse with the distributor/test facility? After all, the user paid for component compliance verification and may now have a lower level of confidence in the distributor's ability to detect counterfeits.
3. How can the user specify better compliance verification testing requirements?
4. Can the supplier suggest or offer better compliance verification testing?
5. Can the user improve their own process and where should those improvements take place?

Today a growing number of companies claim they have the best solution for screening out counterfeits. The reality is that there is no standard for compliance verification testing to screen fraudulent/counterfeit parts.

An international industry standard is being developed that should be available within a year. Even if parts are deemed genuine, there is still concern as to how they were handled and stored after leaving the manufacturer or authorized distributor—Were they exposed to ESD, temperature, vibration or shock?

Users and suppliers access Manufacturer's Product Discontinuation Notices (PDNs). Can a review of this information and a comparison of parts' markings early in the compliance verification process reduce or eliminate the need for additional testing? Comments or questions? Contact Phil Zulueta 818-354-1566.

**Foil Resistors Design and Selector Guide for High Precision Resistors** This document is a design resource and can be downloaded for free at [www.vishaypg.com/doc?49789](http://www.vishaypg.com/doc?49789)

**Task Group Update: Class Y for MIL-PRF-38535 (Xilinx Virtex-4/-5 FPGAs and similar devices)** The G12 membership approved Class Y Task Group charter states "this task group will develop requirements, including qualification and screening standards, for non-hermetic, ceramic-based microcircuits suitable for space applications. Initial effort will be focused on support for devices using flip-chip ceramic column grid array packaging, with resulting requirements to be submitted as a proposal for consideration to DLA Land and Maritime."

DLA-VA is currently conducting an Engineering Practice (EP) Study, which is a peer review on a very large scale. User community comments must be submitted to DLA by Sept. 10, 2011. Contact Shri Agarwal 818-354-5598.

**Testing Column Grid Array (CGA) Limits**  
The area array devices after solder-column attachment may be limited for operation over temperature. Some estimates put the solder melting point at about 180°C.

Once assembled, can the finished CGAs be electrically tested over the military case temperature range of -55°C to +125°C? Would it be prudent to subject CGAs to +125°C case temperature? Could there be solder brittleness concerns at -55°C case temperature?

What tests should be performed on the CGAs prior to their installation on flight boards? User community comments are invited. Contact Shri Agarwal 818-354-5598.

### **Manufacturing Readiness Level Deskbook**

This Department of Defense 'Best Practice' resource link addresses MRL's relationship to system milestones, Technology Readiness Levels, and technical reviews: [http://www.dodmrl.com/MRL\\_Deskbook\\_V2.pdf](http://www.dodmrl.com/MRL_Deskbook_V2.pdf)

### **NASA parts specialists recently supported DLA Land and Maritime Audits of:**

Kyocera, San Diego, California; Microcross Components, Orlando, Florida; Microsemi, Ireland; Microcross Components, Austin, Texas; Aeroflex Colorado Springs, Colorado; International Rectifier, Leominster, Massachusetts.

### **Upcoming Meetings**

- MEWS Microelectronics Workshop: Tsukuba International Congress Center, Japan October 13-14, 2011 <https://eeepitnl.tksc.jaxa.jp/mews/en/index.htm>
- JEDEC JC-13 Meeting: Columbus, OH, Oct. 3-6, 2011

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<http://atpo.jpl.nasa.gov/nepag/index.html>

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#### **Previous Issues:**

**JPL:** <http://atpo/nepag/index.html>

#### **Other NASA centers:**

<http://nepp.nasa.gov/index.cfm/12753>

#### **Public Link (best with Internet Explorer):**

<http://trs-new.jpl.nasa.gov/dspace/handle/2014/41402>

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[www.nasa.gov](http://www.nasa.gov)

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