Reliability Evaluation of Base-Metal-Electrode Multilayer Ceramic Capacitors for Potential Space Applications

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Abstract

Base-metal-electrode (BME) ceramic capacitors are being investigated for possible use in high-reliability space-level applications. This paper focuses on how BME capacitors' construction and microstructure affects their lifetime and reliability.

Examination of the construction and microstructure of commercial off-the-shelf (COTS) BME capacitors reveals great variance in dielectric layer thickness, even among BME capacitors with the same rated voltage. Compared to PME (precious-metal-electrode) capacitors, BME capacitors exhibit a denser and more uniform microstructure, with an average grain size between 0.3 and 0.5 μm, which is much less than that of most PME capacitors. BME capacitors can be fabricated with more internal electrode layers and thinner dielectric layers than PME capacitors because they have a fine-grained microstructure and do not shrink much during ceramic sintering. This makes it possible for BME capacitors to achieve a very high capacitance volumetric efficiency.

The reliability of BME and PME capacitors was investigated using highly accelerated life testing (HALT). Most BME capacitors were found to fail with an early avalanche breakdown, followed by a regular dielectric wearout failure during the HALT test. When most of the early failures, characterized with avalanche breakdown, were removed, BME capacitors exhibited a minimum mean time-to-failure (MTTF) of more than 10^5 years at room temperature and rated voltage.

Dielectric thickness was found to be a critical parameter for the reliability of BME capacitors. The number of stacked grains in a dielectric layer appears to play a significant role in determining BME capacitor reliability. Although dielectric layer thickness varies for a given rated voltage in BME capacitors, the number of stacked grains is relatively consistent, typically around 12 for a number of BME capacitors with a rated voltage of 25V. This may suggest that the number of grains per dielectric layer is more critical than the thickness itself for determining the rated voltage and the life expectancy of the BME capacitor.

The leakage current characterization and the failure analysis results suggest that most of these early avalanche failures are due to the extrinsic minor construction defects introduced during fabrication of BME capacitors. The concentration of the extrinsic defects must be reduced if the BME capacitors are considered for high reliability applications. There are two approaches that can reduce or prevent the occurrence of early failure in BME capacitors: (1) to reduce the defect concentration with improved processing control; (2) to prevent the use of BME capacitors under harsh external stress levels so that the extrinsic defects will never be triggered for a failure. In order to do so appropriate dielectric layer thickness must be determined for a given rated voltage.

Introduction

Multilayer ceramic capacitors (MLCCs) are key building blocks in modern electronics. MLCCs make up ~30% of the total components in a typical hybrid circuit module such as a DC-DC converter. Presently, more than 95% of MLCCs manufactured worldwide use BME capacitors. Although the use of BMEs rather than the more traditional PMEs is due to the sky-high price of palladium, the performance and reliability of BME capacitors have been significantly improved over the last 20 years [1]. Today, the quality of MLCCs with BME technology has reached the standard of air-fired MLCCs with Pd/Ag inner electrodes.

One of the advantages of using BME capacitors is that the extremely high capacitance volumetric efficiency ($\mu F/cm^3$) can be achieved at a relatively low cost. The dielectric thickness of a BME capacitor has been reduced to submicrons, and there may be several hundred dielectric layers per capacitor. This makes it almost economically impossible to use PME material, especially considering that the price ratio of palladium to nickel was about 80:1 in 2000 [2]. Recently, a BME chip ceramic capacitor with a capacitance of 22μF and voltage rating of 25V, in an EIA chip size of 2012, has been demonstrated [3].

Although BME technology is predominant in the fabrication of MLCCs today, the MLCCs for high-reliability space applications have always required mature technology with robust design and proven reliability. All MLCCs used in space programs must meet at least the established military standards of MIL-PRF-123 or MIL-PRF-55681. These standards not only require 2,000- to 4,000-hour qualification life testing, but they also require the ceramic capacitors to have a minimum dielectric thickness of at least 0.8 mils (~20 μm) for a 50V MLCC, or 1.0 mil (~25 μm) for above 50V [4]. Recently, NASA Goddard Space Flight Center has permitted a reduction in the dielectric thickness to as low as 0.4 mil (10 μm), and an EIA chip size of 0402 for 5V, 10V, and 16V PME ceramic capacitors [5]. This effort reflects the high demand for the miniaturization of capacitors in potential space applications. The increasing use of MLCCs with BME technology has led to the need for a comparative study of BME capacitors and traditional PME capacitors with thinner dielectric layers (< 20 μm).

There are two primary concerns with regard to using BME capacitors for high-reliability applications. First, the reliability of BME capacitors with thinner dielectrics has always been a concern for space applications, particularly since the commercial sector has led to a reduction in dielectric layer thickness to 2 μm or less. The minimum dielectric thickness requirement for high reliability per MIL-PRF-123 demonstrates its importance for MLCC products. However, a very recent report from Intel Corporation showed a worrying trend with respect to the life reliability of high-capacitance BME capacitors in the range of 2.2 to 100 μF. As capacitance density has increased, the usable life has been reduced to hundreds, then tens, and now to even less than 5 years. This rapid life reliability degradation has been attributed to the method by which the capacitance density of BME MLCCs has increased, i.e., reducing dielectric layer thickness and stacking up of hundreds of layers of dielectric material between layers of base-metal electrodes. As the dielectric layer thickness is reduced, the rated voltage of the capacitors is also reduced, thereby adversely impacting the BME capacitor's life reliability [6]. This Intel report confirms a longstanding concern that capacitance density of BME MLCCs cannot be increased without limit. There must be a minimum dielectric layer thickness at which the capacitance value is limited and the reliability meets the lifetime expectancy requirements.

Secondly, BME capacitors must be sintered in a reducing atmosphere to prevent the inner nickel electrodes from oxidization. However, in a reducing atmosphere, $BaTiO_3$ dielectric materials are reduced to a non-stoichiometric state, forming a significant amount of doubly ionized oxygen vacancies. As a result, the insulation resistance (*IR*) of a $BaTiO_3$ dielectric decreases by more than 10 orders of magnitude after sintering in a reducing atmosphere [7]. The success of BME technologies in the last 20 years has been the development of dielectric materials and processing techniques that can maintain high insulating resistance (IR) after sintering. The efforts include:

- *Ba*-site excess or the addition of transition metal oxides such as MnO and Cr_2O_3 to occupy the *Ti*-site in $BaTiO_3$ can behave as acceptors to compensate for the excess of electrons generated by oxygen vacancies

[8, 9]. Poor ceramic microstructure and humidity resistance due to the acceptor-doping can be significantly improved when a low-melting glass phase is introduced to the dielectric sintering process [10].

- Controlled re-oxidation and rare-earth doping has been proven to be the most effective method for improving the *IR* in BME ceramic dielectrics. After sintering BME capacitors in a reducing atmosphere, a subsequent re-oxidation annealing at lower temperatures significantly reduces the number of oxygen vacancies by diffusing oxygen into the oxygen-deficient $BaTiO_3$ lattice and refilling the vacancies [11]. Some trivalent rare-earth cations, including Y^{+3}, Ho^{+3}, Er^{+3}, and Dy^{+3}, were found to show an "amphoteric" behavior, i.e., to partially occupy both *Ba-* and *Ti-*sites in $BaTiO_3$ and to form a so-called donor-acceptor complex, which results in superior dielectric insulation and life reliability [12-14].

Although the above efforts have significantly reduced the number of oxygen vacancies and slowed down their migration in BME capacitors, studies have shown that when BME capacitors are life tested under a DC bias, there is a gradual increase in the oxygen vacancy concentration across the dielectric layers towards the cathode. Additionally, within each $BaTiO_3$ grain, there is a pileup of oxygen vacancies at the cathode side of the grain [15, 16]. This observed oxygen vacancy segregation in BME dielectric layers, as well as its impact on long-term reliability, need to be further understood.

In this paper, commercially available high-capacitance BME MLCCs and PME MLCCs with thinner dielectrics were evaluated for construction, microstructure, and life reliability, per the requirements of MIL-PRF-123. Both highly accelerated life testing (HALT) and regular life testing at 125°C with twice the rated voltage have been used for the evaluation (the regular life testing results will be discussed elsewhere). In addition, a short-term survivability test of these capacitors under a time-varying stress has also been investigated. Results of the time-varying stress testing will be reported in a separate paper [17].

**Constructional Analysis of BME and PME Capacitors**

In order to understand the reliability differences between BME and PME capacitors, commercially available BME capacitors and PME capacitors with thinner dielectric layers were selected and processed for construction analysis per MIL-PRF-123. The construction analysis procedure follows EIA standard EIA/ECA-469D.

The BME capacitors were selected based upon the following criteria: (1) the BME manufacturer shall be a primary supplier of BME capacitor products; (2) only BME capacitors with a rated voltage of 25V or less were selected for the beginning of this study, based on the fact that dielectric layer thickness gets thinner as the rated voltage is reduced, and BME capacitors with thinner dielectrics pose the greatest interest for future applications; (3) a chip size of 1206 or smaller was selected due to the miniaturization requirement for potential space applications; (4) for a given chip size and rated voltage, the BME capacitors with the higher capacitance were selected. These high-CV parts represent the best fabrication capability of a manufacturer.

Capacitor samples for physical construction and microstructure characterizations were prepared by either epoxy potting or fracturing and were then investigated using cross-section scanning electron microscope (SEM) and energy dispersive X-ray spectroscopy (EDX). Figure 1 shows front and end side views of a typical BME MLCC from manufacturer A. The physical meaning of "side margin," "end margin," and "cover plate" are also illustrated. The minimum requirements for these geometric parameters according to EIA-469D, paragraph 5.1.3 are summarized in Table I. Other important physical characteristics of MLCC devices, such as dielectric thickness, internal electrode thickness, manufacturing defects, and number of layers, etc., can also be obtained from these construction examinations.

Table I. Minimum requirements in construction margins per EIA-469D for MLCCs

| Geometric Parameters	Rated Voltage (V)	Minimum Requirements μm(inch)
Side Margins	25 or less	25 (0.001)
End Margins	25 or less	40 (0.0016)
Cover Plate Thickness	25 or less	40 (0.0016)
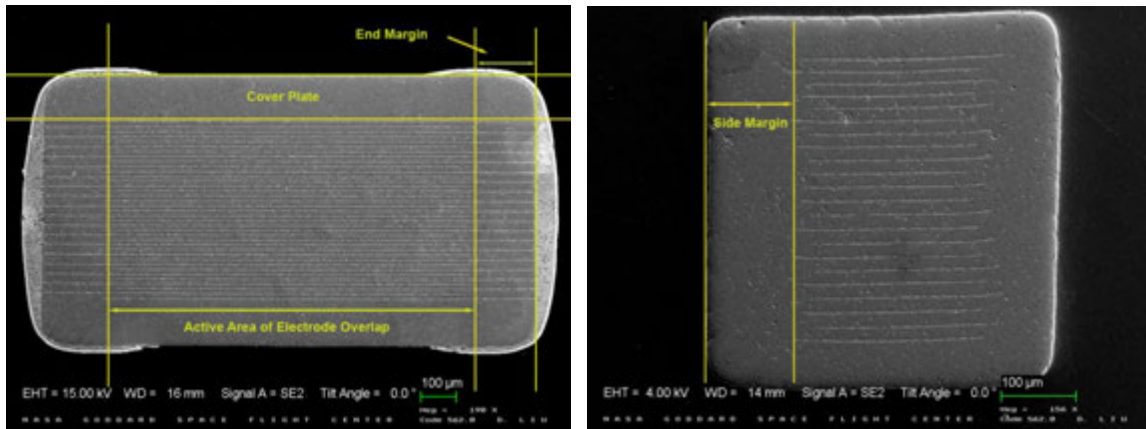
Figure 1. Front (left) and end (right) side SEM views of a typical BME MLCC from manufacturer A. The end margin, side margin, and cover plate are labeled.

Figures 2 and 3 compare SEM images of a BME capacitor and a military-grade PME capacitor for dielectric/electrode, end margin, and cover plate thickness. The BME capacitor is 18,000 pF, 25V-rated, and 0402 in chip size, while the PME capacitor is 39,000 pF, 50V-rated, and 1206 in chip size. Although the capacitance of
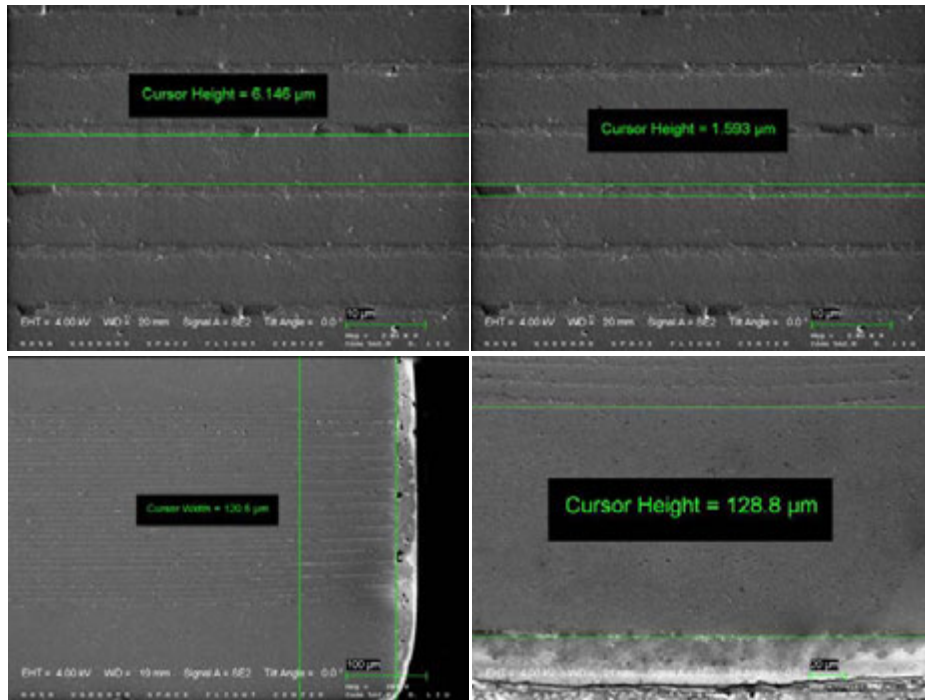
Figure 2. Cross-section SEM images of a BME capacitor show an average dielectric thickness of 6.2 μm, internal electrode thickness of 1.6 μm, end margin of 120 μm, and cover plate thickness of 130 μm. This capacitor is 18,000 pF, 25V-rated, 0402 in chip size, and was fabricated by manufacturer B.
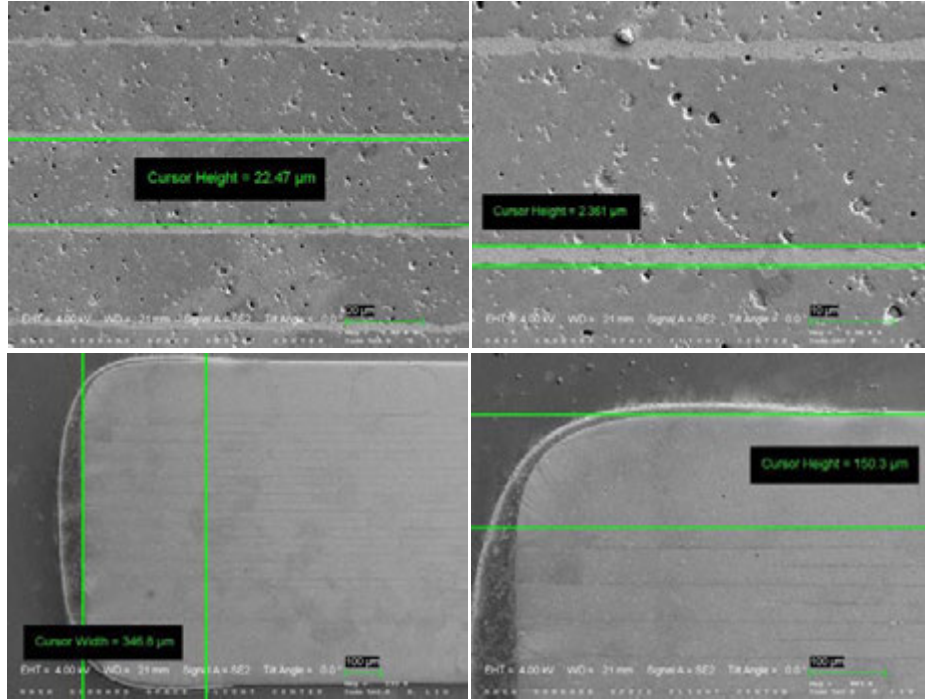
Figure 3. Cross-section SEM images of a PME capacitor show an average dielectric thickness of 22.5 μm, internal electrode thickness of 2.4 μm, end margins of 350 μm, and cover plate thickness of 150 μm. This capacitor is 39,000 pF, 50V-rated, 1206 in chip size, military grade, and is fabricated by manufacturer D.

the PME device is twice that of the BME device, the volumetric efficiency (μF/cm^3) of the BME device is 27 times better than that of the PME device, showing significant advantages in device miniaturization using BME technology.

Table II summarizes the construction analysis results for some of the BME and PME capacitors examined in this study. This table represents an ongoing effort in the characterization of capacitor constructions.
Based on the analysis results in Table II, some important characteristics are revealed:

- Every capacitor examined showed margins at least twice that of the minimum requirements outlined in Table II. Although reduction in dielectric layer thickness is the most effective method for increasing volumetric efficiency, a significant amount of capacitance can be readily achieved if the construction margin areas are fully utilized.
- The dielectric thickness varies dramatically depending on the rated voltage, capacitance, chip size, and manufacturer, from as thin as 2.0 μm to as thick as 12.0 μm in all BME capacitors inspected, while the PME capacitor had a minimum dielectric layer thickness of 12.4 μm.
- As many as 750 dielectric layers were revealed for A12X22606, a BME capacitor with a capacitance of 22μF and voltage rating of 6.3V, in an EIA chip size of 1206, from manufacturer A. However, for many BME capacitors, even with the same rated voltage, both dielectric thickness and number of dielectric layers varied from product to product and from manufacturer to manufacturer.

Table II. Construction analysis results of BME and PME capacitors

| Capacitor ID*	Construction Parameters				
	Dielectric (Electrode) Thickness (μm)	No. of Dielectric Layers	Cover Plate Thickness (μm)	Side Margins (μm)	End Margins (μm)
A04C33116	4.5 (1.8)	46	100	100	100
A04C33125	10.0 (2.2)	29	70	140	110
A06X47425	4.2 (1.3)	150	60	125	100
A06X10425	7.9 (2.5)	62	85	160	100
A06C10225	12.0 (2.2)	36	130	175	175
A08X22525	4.4 (2.0)	275	62	135	150
A12X22606	2.0 (1.3)	750	75	160	140
A12X10616	3.5 (1.4)	300	65	190	150
A12X47425	10.5 (2.3)	75	175	340	220
B04X10406	2.5 (1.5)	70	85	110	110
B04X10416	2.0 (2.2)	65	100	95	95
B04X47325	4.0 (2.2)	49	125	125	110
B04X18325	6.2 (1.6)	33	130	120	120
B06X22425	4.2 (1.8)	120	100	140	120
B08X10525	4.6 (1.6)	150	80	120	120
B08X33425	5.8 (1.8)	110	120	140	115
B12X10606	3.5 (1.3)	250	75	120	115
C04X10410	2.6 (1.7)	77	65	105	90
C04X10416	3.4 (1.5)	80	60	105	95
C04X47325	4.4 (1.7)	60	55	105	90
C04C10250	4.0 (1.0)	77	65	105	100
C08X10606	2.0 (1.2)	575	75	65	105
C06X10525	3.1 (1.2)	150	75	125	110
C06C39250	3.5 (1.2)	150	75	190	165
C08X56425	4.0 (1.4)	170	80	120	110
C08X47516	2.5 (1.5)	250	110	105	100
D04X10310	15.1 (2.0)	22	65	100	120
D06X10405	12.4 (2.2)	24	80	120	160
D08X10425	20.2 (2.2)	23	120	260	220
D12X39350	22.5 (2.4)	22	150	350	350

*: Capacitor ID: C (manufacturer ID); 08 (EIA chip size, 08=0805); X (dielectric type, X=X7R); 475 (cap values, 475=4,700,000 pF); 16 (rated voltage).
   For example: D06X36405 = 360000pF, 5V, 0603, from manufacturer D.

Microstructure Examination of BME and PME Capacitors

Cross-section SEM images of a number of BME capacitors are shown in Figure 4. All BME capacitors demonstrate somewhat similar microstructures, with a dense, uniform grain matrix. The average grain sizes are in the submicrons and are typically around 0.3~0.5 μm. No second phase or glass phase was seen, although some BME capacitors had segregated fine particles.

(a)   (b)

(c)   (d)

(e)   (f)
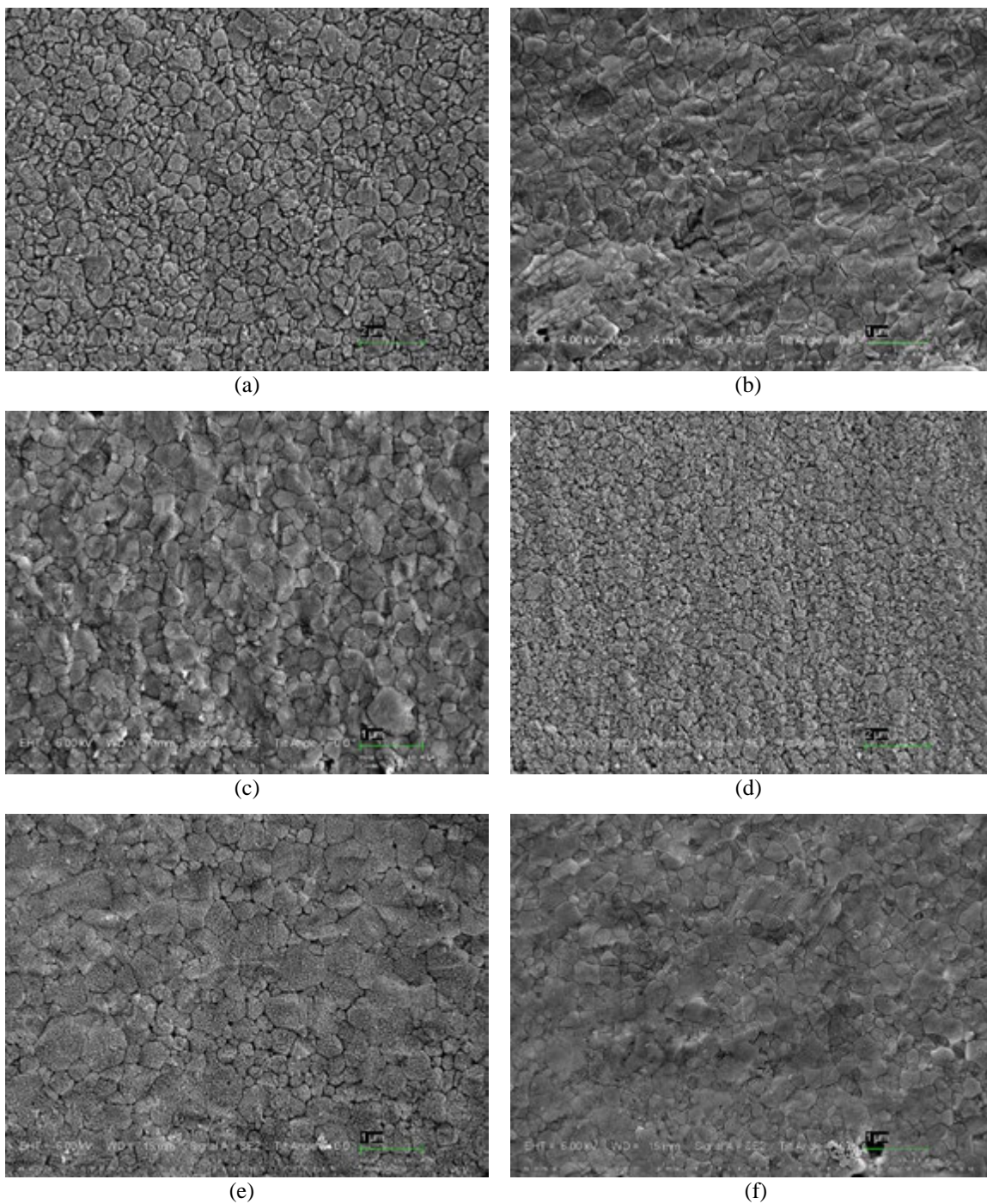
Figure 4. Cross-section SEM images reveal the microstructure of a number of BME capacitors from different manufacturers. All of these BME capacitors with SEM examination exhibit a similar microstructure and grain size.

(a) 0.1 µF, 25 V, 0603, manufacturer A. (b) 1.0 µF, 16 V, 0603, manufacturer A.
(c) 47000 pF, 25 V, 0402, manufacturer B. (d) 1.0 µF, 25 V, 0806, manufacturer B.
(e) 0.1 µF, 10 V, 0402, manufacturer C. (f) 4.7 µF, 16 V, 0805, manufacturer C.

Figure 5 compares the microstructures of a BME and a PME capacitor. The microstructure of the PME capacitor was found to be quite different from that of the BME capacitor; the PME capacitor had larger (average grain size is ~0.68 μm, with a number of grains more than 1 μm in diameter), non-uniform grains, and there appears to be a second glass phase that surrounds the BaTiO₃ grains. The EDX analysis showed that the internal electrodes of the BME capacitors are pure nickel, while those of the PME capacitors are a palladium/silver alloy. In addition, all of the PME capacitors inspected in this study had a similar microstructure; a typical example is shown in Figure 5(b). Features of this structure are that all the round-shape BaTiO₃ grains are surrounded by the liquid phase, and a typical core-shell grain structure can be identified in some grains [18, 19]. The similarity in microstructures suggests that all of the PME capacitors investigated in this study were fabricated with similar compositional formulations and processing steps.
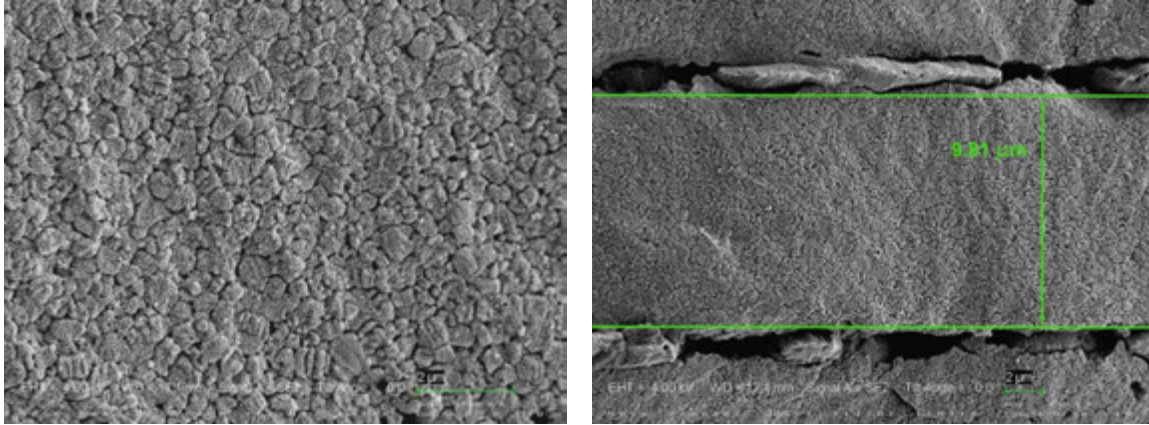
(a) 0.15 μF, 25 V, 0805, manufacturer A, with an average grain size of 0.46 μm.
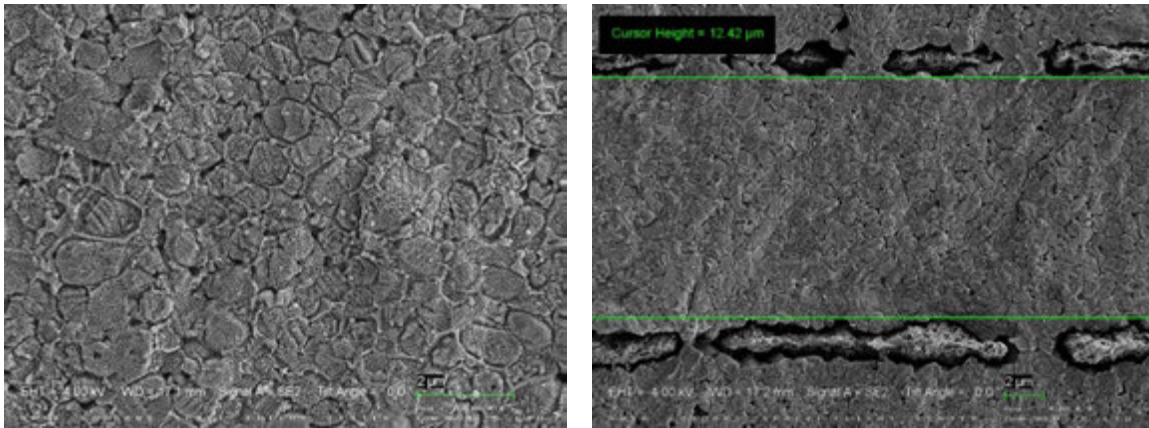
(b) 0.10 μF, 5 V, 0603, manufacturer D, with an average grain size of 0.68 μm.

Figure 5. Microstructure comparison between a BME (a) and a PME (b) capacitor. The PME capacitor has a different microstructure, with larger, non-uniform grains and a surrounding glass phase.

As can be seen in Figure 4, all BME capacitors exhibit denser microstructures, with smaller and more uniform grains. This difference in microstructure between BME and PME capacitors can be explained by their difference in sintering conditions.

In general, ceramic capacitor sintering involves two stages: recrystallization (grain growth) and densification (shrinkage). The grain growth occurs at the early stage of sintering, characterized by the grain size increase from the initial compressed, deformed ceramic powders. The grain growth takes place by material transport between

neighboring grains. Only the grains that are over a certain critical size will have a high enough nucleation rate to grow. When grain size reaches a certain value, almost all of the adjacent grains are impinging on each other. Depending on the size difference, the larger grains incorporate the smaller grains due to the energetic difference at the grain surface. This incorporation process is called "secondary recrystallization" and is characterized by the disappearance of grain boundaries and the formation of large grains with straight grain boundaries, as well as significant volume shrinkage in the ceramic body (densification) [20].

The dense, uniform grain structure in BME capacitors suggests a uniform distribution in the initial $BaTiO_3$ powder size, which results in a fairly high nucleation rate at the beginning of recrystallization, such that grain growth occurs at most of the original ceramic powder locations. This prohibits the formation of large grains prior to the secondary recrystallization process, and so ceramic shrinkage is minimal during the sintering of BME capacitors.

On the other hand, in order to utilize the silver/palladium alloy as an internal electrode, the sintering temperature of the $BaTiO_3$ dielectric must be reduced to around 1300 °C. Because the material transport rate during sintering is highest in the liquid phase, a low-temperature melting glass is used since it is extremely effective in reducing the densification temperature of ceramic sintering. The high material transport rate in the liquid phase also significantly increases the growth rate of larger grains and results in secondary recrystallization, characterized by the appearance of large and non-uniform grains in the final ceramic microstructure. This is typical in the sintering process of PME capacitors with the addition of a low-temperature melting glass phase as a sintering aid [Figure 5(b)].

This significant difference in ceramic microstructure between BME and PME capacitors plays an important role in their performance and reliability. A recent report [6] showed that as the dielectric became thinner, a BME capacitor's life expectancy was reduced dramatically. MIL-PRF-123 sets a clear minimum acceptable dielectric thickness for PME capacitors, i.e., 20 μm for rated voltages of 50V or less. This clearly indicates the importance of dielectric thickness and microstructure for the reliability of both BME and PME capacitors. When dielectric thickness is reduced below a certain value, the reliability deteriorates. In addition, all X7R BME and PME capacitors use ferroelectric $BaTiO_3$ as the dielectric material. It has been found that the reliability of ferroelectric materials is highly dependent on the properties of the grain boundary regions [21, 22]. In order to sustain certain levels of rated voltage, each dielectric layer must have a certain number of stacked grains so that the electrical field will not be applied on only one or a few grains.

Highly Accelerated Life Testing of BME and PME Capacitors

1. Accelerating Factor and Weibull Model
The essential issue in highly accelerated life testing is determining each of the failure modes of interest in the planned use of the part and then determining the acceleration of the rate of failure caused by each failure mode as the applied stresses are increased. For capacitors, the applied stresses are usually the voltage and temperature, and they are normally held constant during the testing. For a wide class of failure modes, the failure rate at one temperature T_1 is related to the failure rate at a second temperature T_2 by an Arrhenius relation:

$$A_T = \frac{Rate(T_1)}{Rate(T_2)} = e^{-\left(E_S/k_B\right)\left(\frac{1}{T_1}-\frac{1}{T_2}\right)} \tag{1}$$

where A_T is the temperature acceleration factor, E_S is an activation energy, k_B is the Boltzman constant, and the temperatures are measured on an absolute scale.

Empirical work has often found that the applied voltage changes the failure rate following an inverse power law:

$$A_V = \frac{Rate(V_1)}{Rate(V_2)} = \left(\frac{V_2}{V_1}\right)^n \tag{2}$$

where A_V is the voltage acceleration factor and n is an empirical parameter. Prokopowicz and Vaskas have proposed that the rate of failure caused by a single failure mode when both V and T are changed is the product of the separate acceleration factors:

$$A_{VT} = \frac{Rate(T_1)}{Rate(T_2)} \cdot \frac{Rate(V_1)}{Rate(V_2)} = \left(\frac{V_2}{V_1}\right)^n \cdot e^{-(E_S/K_B)\left(\frac{1}{T_1}-\frac{1}{T_2}\right)}. \tag{3}$$

This is the well-known Prokopowicz and Vaskas equation (P-V equation). The P-V equation has proven useful in the capacitor industry for testing MLCCs at various testing conditions. An average of $n \sim 3$ has been generally found for the voltage acceleration factor and an average value of $1 < E_S < 2$ eV is typical for the temperature acceleration factor.

When a *2*-parameter Weibull model is applied, the cumulative distribution function CDF that provides the probability of failure at time t is given by:

$$F(t) = 1 - e^{-\left(\frac{t}{\eta}\right)^\beta} \tag{4}$$

where e is the base for natural logarithms, t the failure time, slope β is the dimensionless shape parameter whose value is often characteristic of the particular failure mode under study, and η is the scale parameter that represents the point at which 63.2% of the population has failed and that is related to all other characteristic times such as mean-time-to-failure (MTTF):

$$MTTF = \eta\Gamma(1 + 1/\beta), \tag{5}$$

where $\Gamma(x)$ is the gamma function of x. (Note, for example, that $\Gamma(1+1/\beta)$ ranges from 0.887 to 0.900 as β ranges from 2.5 to 3.5.)

When both A_V and A_T are combined for HALT testing, the Weibull distribution scale parameter η can be expressed as:

$$\eta(V,T) = \frac{C}{V^n} \cdot e^{\left(\frac{B}{T}\right)} \tag{6}$$

where C and $B = E_S/k_B$ are constants. When Eqs. (4), (5), and (6) are combined, the cumulative distribution function $F(t)$ and $MTTF$ can be expressed as:

$$F(t) = 1 - e^{-\left(\frac{t\cdot V^n e^{-\left(\frac{B}{T}\right)}}{C}\right)^\beta} \tag{7}$$

and

$$MTTF = \frac{C}{V^n} \cdot e^{(B/T)}\Gamma(1 + 1/\beta). \tag{8}$$

By taking advantage of the maximum likelihood estimation method described by Nelson [32], reliability and accelerating parameters B, β, C, and n in Eq. (7) can all be determined.

The purpose of HALT testing is to predict the median life of capacitors under a normal, non-accelerated operating condition. In this study, the "normal use level" condition refers to the capacitors being at room temperature (300K)

and at rated voltage. When accelerating factors n and $B = E_S/k_B$ are known, the reliable life t_R of a unit for a specified reliability, starting the mission at zero, can be determined by:

$$t_R = \eta \cdot \{-ln[1 - F(t_R)]\}^{1/\beta} = \frac{C}{V^n} \cdot e^{\left(\frac{B}{T}\right)} \cdot \left\{ -ln\left[e^{-\left(\frac{t_R \cdot V^n e^{-\left(\frac{B}{T}\right)}}{C}\right)^{\beta}} \right] \right\}^{1/\beta} \quad (9)$$

Note that this is the life for which the unit will function successfully with a reliability of $[1 - F(t_R)]$. If $[1 - F(t_R)] = 0.5$, then t_R = the median life [23].

2. HALT Results and Discussion

A 20-position printed circuit board (PCB) testing card was used for the characterization of BME and PME capacitors throughout this study. The PCB card was made from polyimide material and was used for high-temperature accelerated life testing up to 200 °C. All capacitors were solder-reflow attached on the testing card prior to testing. The soldering reflow condition followed MIL-PRF-55681. No-clean solder paste with RMA flux was used. Only one reflow cycle was applied.

BME and PME capacitors with 25V rated voltage and various chip sizes and capacitances were tested at various accelerated stress levels. The HALT tests were performed at three different temperatures and at three voltages, as shown in Table III.

Table IV summarizes the microstructure data of all of the 25V BME capacitors and the PME capacitors with thin dielectrics to be HALT tested. The capacitor ID nomenclature was explained in Table II of this paper. All of PME

Table III. HALT conditions for 25V BME capacitors

Temperatures	Voltage level 1	Voltage level 3	Voltage level 3
155 °C		250 V	
165 °C	150 V	200 V	250 V
175 °C		150 V	

**Table IV. Microstructure Data of 25V BME Capacitors and PME Capacitors with Thin Dielectrics**

Capacitor ID	Processing Technology	Dielectric Thickness (µm)	Avg. Grain Size (µm)
A08X22525	BME	3.5	0.31
A08X15425	BME	9.8	0.46
A06X10425	BME	7.6	0.47
B06X22425	BME	4.2	0.34
B08X33425	BME	5.8	0.42
B08X10525	BME	4.6	0.40
C06X10525	BME	3.1	0.44
C08X56425	BME	4.0	0.39
D06X10405	PME	12.4	0.68
D04X10310	PME	15.1	0.65
D08X10425	PME	20.2	0.61

capacitors are from manufacturer D, and one of them is rated at 5V; the other is rated at 10V. The reason for including the 5V and 10V PME units when all of the other capacitors are rated at 25V is because these PME capacitors have relatively thick dielectric layers when compared to all of the other BME capacitors, but they are still thinner than the minimum dielectric thickness requirement per MIL-PRF-123.

Figure 6 shows the cumulative failure rate as a function of time-to-fail on a Weibull plot for a 0.22 μF, 25V, 0603 BME capacitor from manufacturer B (B06X22425). The test conditions for each HALT data set are labeled for temperature and voltage. The corresponding contour plot is also illustrated in Figure 6.

A contour plot can be used to give a visual picture of confidence bounds on the β and η for a 2-parameter Weibull distribution at a certain confidence level (typically 95%). Plot is often applied to compare different data sets for distinguished failure modes and to determine whether two sets are significantly different. When sample size is small (≤ 20), a reduced bias adjustment is usually required to ensure contour plot accuracy [24]. Contour plot has been a useful tool to evaluate if the stress levels are set appropriately in an accelerated life testing. If there is no overlap between two adjacent 95% contours, then the two data sets are statistically different, with a confidence of 95%, indicating that the selected stress levels are well separated from each other. When a horizontal line, which represents a constant value of β, is drawn in a contour plot and can cross all of the contours, it indicates that the failure mode cannot be distinguished among all of these data sets.

The contour plots shown in Figure 6 reveal that all of the contours are well separated, with no obvious crossovers, indicating an acceptable accelerating testing profile. When a horizontal line is drawn near $\beta \sim 2.2$, it appears to cross all contours, indicating that the data sets obtained at different stress levels share a single failure mode.
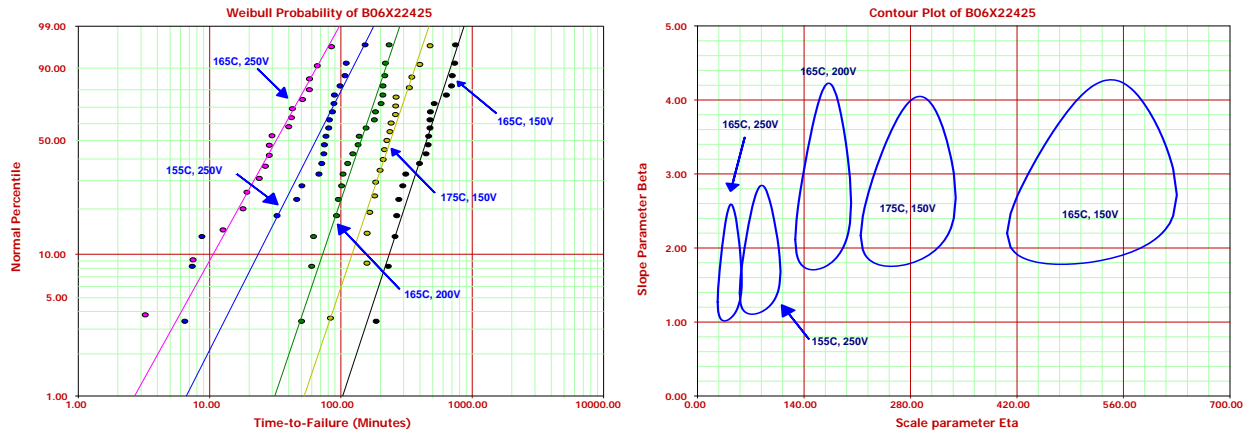
Figure 6. Weibull plot of failure percentile as a function of time-to-failure (left) and corresponding contour plot (right) for a 0.22 μF, 25 V, 0603 BME capacitor made by manufacturer B. All of the contours are well separated, with no crossovers, indicating an acceptable accelerating testing profile, as shown in Table II.

Figure 7 shows use-level Weibull probability plots of a number of BME and PME capacitors that have been HALT tested in this study. The use-level conditions are set as 300K and rated voltage (25V for all BME capacitors). Each data point in Figure 7 was extrapolated using Eq. (9). This is done for each failure and for any suspensions that are entered, and then the median ranks of the failures are determined. The data points are "best fitted" using a single 2-parameter Weibull model, based on the assumption that only one failure mode should be dominant in a valid HALT test. The voltage and temperature accelerating factors n and E_s are determined from Eq. (3).

The advantages of this "normalized" use-level probability plot include: (1) it reveals the testing data better if multiple failure modes exist, and (2) it is convenient for comparing calculated Weibull reliabilities among different capacitors.
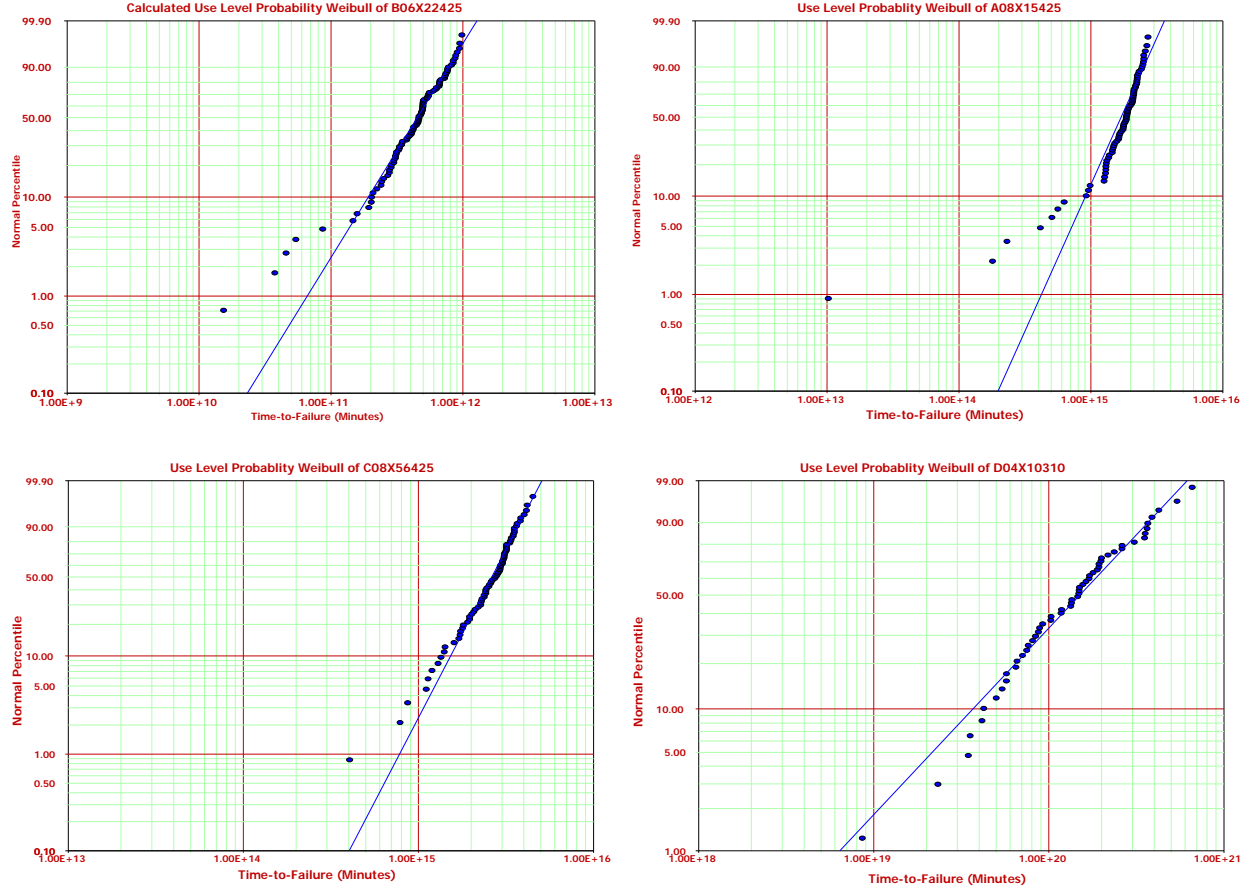
Figure 7. Use-level Weibull probability plots of BME and PME capacitors with 25V rating. All data points are extrapolated using Eq. (9) and best fitted using a single *2*-parameter Weibull model.

Upper left: 0.22 µF, 0603, manufacturer B; Upper right: 0.15 µF, 0805, manufacturer A;
Lower left: 0.56 µF, 0805, manufacturer C; Lower right: 0.01 µF, 0402, manufacturer D.

In Figure 7, although the majority of the data points fit the Weibull model very well, the deviating points, which represent "early time failures," are always shown in the lower left corner near the fitted curve for almost every BME capacitor. However, no such "early time failures" are found in any PME capacitors. In addition, military-grade D08X10425 PME capacitors (0.1 µF, 25V, 0805, from manufacturer D) did not exhibit any failures during HALT testing, suggesting that the test conditions were not accelerated enough to generate failures for this PME capacitor with a measured dielectric thickness of 20.4 µm. On the other hand, most of the A08X22525 BME capacitors (2.2 µF, 25V, 0805, made by manufacturer A), were found to be electrically shorted at the very beginning of HALT testing, indicating that the test conditions were too aggressive for this capacitor.

The "early time failures" always cause a slight curve at the bottom of the distribution, indicating a subpopulation that fit a line with a smaller β value (shown in Figure 7). The presence of offsets has been attributed to the minor construction defects such as voiding, cracks, and delamination during the manufacturing of the capacitors. These "early time failures" are usually ignored and not used in statistical calculations when the typical dielectric wearout mechanism is the point of interest [25]. However, as will be discussed later, these "early time failures" play a significant role if the BME capacitors are to be considered for potential high-reliability space applications.

Figure 8 summaries the use-level Weibull plots for all of the BME and PME capacitors listed in Table IV, except A08X22525 and D08X10425. Table V shows the Weibull reliability data and voltage accelerating factor *n* of the

BME and PME capacitors shown in Figure 8. These results have revealed some interesting behaviors for these capacitors:
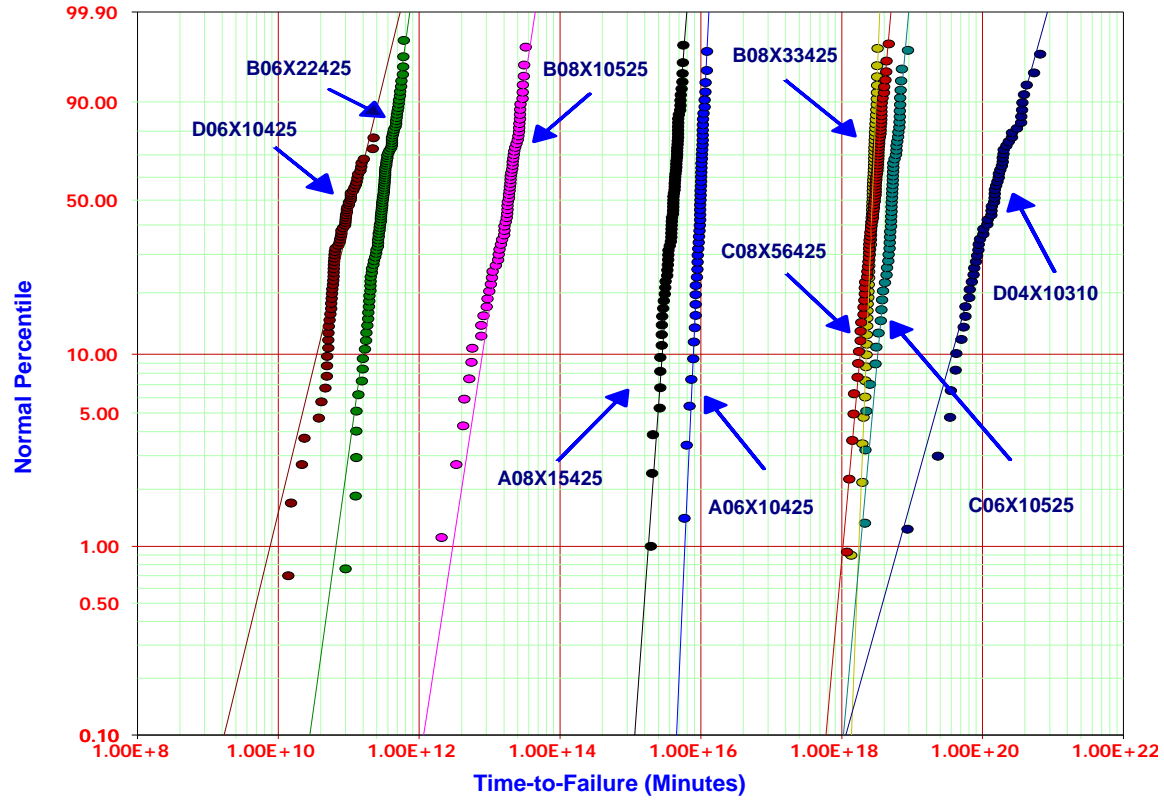
Figure 8. Modeling results for HALT testing capacitors with rapid wearout. Early time failures were removed.

Table V. Weibull reliability modeling results for MLLCs with 25 V rated voltage

Capacitor ID	Electrode	Dielectric Thickness (μm)	Avg. Grain Size (μm)	No. of grain stacking	β	E$_s$(eV)	n	MTTF (yrs)
A08X22525	BME	3.5	0.31	11.29	All units were short during HALT			
A08X15425	BME	9.8	0.46	21.30	5.21	1.52	4.63	7.62E09
A06X10425	BME	7.6	0.47	16.17	8.47	1.70	3.86	1.84E10
B06X22425	BME	4.2	0.34	12.35	2.71	1.00	4.58	6.11E05
B08X33425	BME	5.8	0.42	13.81	9.54	1.45	4.35	1.73E12
B08X10525	BME	4.6	0.40	11.50	2.42	1.24	4.92	3.39E07
C06X10525	BME	3.1	0.44	7.05	4.14	1.82	8.70	9.72E11
C08X56425	BME	4.0	0.39	10.26	3.99	1.57	4.82	1.11E11
D06X10405	PME	12.4	0.77	16.11	1.54	0.99	2.83	2.62E05
D04X10310	PME	15.1	0.68	22.21	1.34	1.01	3.04	3.81E12
D08X10425	PME	20.2	0.61	33.11	No failures during HALT			

- All of the BME capacitors reveal a Weibull slope parameter β in the range of 2.42 to 9.54, with most of them over 4.0, indicating a typical dielectric wearout failure mode. A β approaching 1.0 has been found for the two PME capacitors, indicating a classic random failure mode. Most of the BME capacitors had a temperature accelerating factor E_s of 1.0~2.0 eV and a voltage accelerating factor of n = 4~5, with some offsets. Average values of n ~3 and E_s ~1 eV was obtained for the two groups of PME capacitors, which are consistent with others' assumptions [26-30]. The higher values of accelerating factors also indicate that BME capacitor reliability is more temperature- and voltage- dependent than that of PME capacitors.
- Although all BME capacitors under HALT testing are 25V-rated, their dielectric layer thicknesses vary significantly. However, the number of stacked grains (dielectric layer thickness /average grain size) per dielectric layer is relatively consistent, typically around 12. This may suggest that the number of grains per dielectric layer is more critical than the thickness itself for determining the rated voltage and the reliability of BME capacitors. It is worth noting that the number of grains per layer does not change much even though the BME capacitors are from different manufacturers, with different capacitances and chip sizes.
- As shown in Figure 8, the capacitors with the lowest and highest MTTFs are D06X10405 and D04X10310, respectively. Both of them are PME capacitors. Since the two capacitors had the same statistical calculation results and accelerating factors, the difference in MTTF can then be attributed to their difference in dielectric thickness.
- It is interesting that all of the MTTFs for BME capacitors are bracketed between the two PME capacitors, with widely spread MTTFs. This indicates that equal life reliability can be attained for BME capacitors with smaller dielectric layer thickness. This may be due to the fact that BME capacitors exhibit much smaller grain size. More HALT testing is required and more data must be accumulated in order to truly reveal the correlations between dielectric layer thickness and life reliability of BME capacitors.

3. Characterization of "Early Time Failures" in BME Capacitors

As shown in Figure 8, when all "early time failures" were removed from the use-level Weibull plot, the MTTFs of BME capacitors are at least 10^5 years and should be acceptable for high-reliability space applications. However, in reality, the removal of so-called "early time failures" would not be easy. In this section, the focus will be on how to eliminate the "early time failures" and thereby to improve the reliability of BME capacitors.

During the HALT testing of ceramic capacitors, each capacitor's DC leakage current is monitored as a function of test time, and the part is considered "failed" when its leakage current reaches 100 μA. Three patterns of leakage current failures have been observed for all of the failed capacitors, as shown in Figure 9.

- An avalanche breakdown, characterized by a sudden and extremely rapid increase in leakage current without any initial gradual increase in leakage current, always occurred first, regardless of the combinations of temperature and accelerating voltage. As testing time increases, there is a decrease in the number of capacitors that fail with this pattern.
- A slow degradation, characterized by a slow but gradual increase in the leakage current eventually reaching the failure criterion of 100 μA, was always observed in a number of BME capacitors. This degradation was very rarely observed in any of the PME capacitors, indicating that the failure pattern is unique to BME capacitors.
- A thermal runaway failure, characterized by an initial slow but substantial increase in leakage current and a gradually accelerated increase to failure, was observed for most capacitor units that failed last.

A detail observation indicates that the capacitors with a slow degradation failure pattern will eventually fail with a thermal runaway breakdown if they are not disconnected from the testing circuit after the failure criterion (100 μA) has been met. This indicates that the slow degradation failure pattern and the thermal runaway are fundamentally the same, although the thermal runaway breakdown in a slow degradation failure will occur at a much higher leakage current level that is far over the 100 μA failure target.
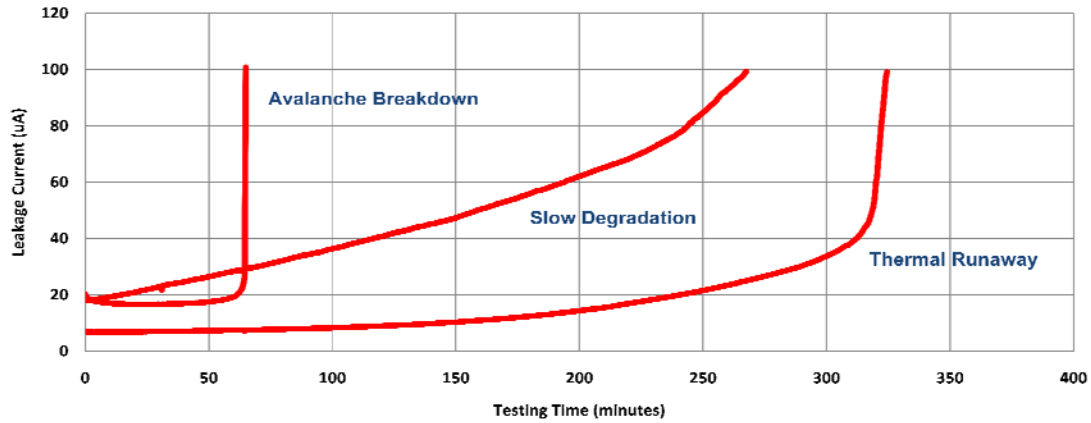
Figure 9. Three distinguishable failure patterns observed in leakage current in BME and PME capacitors.

In order to gain insights into the leakage current failure patterns and their correlations to the physical failure mechanism in MLCCs, a number of failed BME capacitors were subjected to a failure analysis. Figure 10 shows a cross-section SEM image and an EDX map of a BME capacitor failed with an avalanche breakdown. The SEM image shows voiding at the defect site. The matching EDX map appears to show a short between opposing electrodes of the capacitor. A white arrow points to the location of carbon and calcium, contaminations likely introduced during manufacturing.
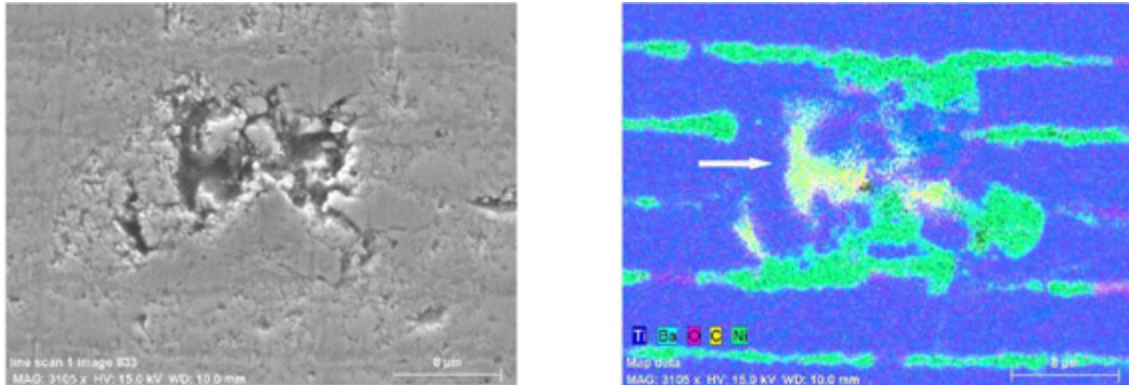
Figure 10. Cross-section SEM image (left) and an EDX map (right) of a BME capacitor failed with an avalanche breakdown pattern. The voiding and carbon calcium contamination introduced during manufacturing are revealed.

More failure analysis data indicate that almost all of the BME capacitors that failed with a leakage-current avalanche breakdown have essentially the same contamination and/or processing defects, such as voiding, delamination, and cracks. The oxygen depletion near the nickel was also indentified in a few samples. This clearly indicates that the BME capacitors' failure with an avalanche breakdown can be attributed to the extrinsic construction defects introduced during the capacitor fabrication. However, these defects are not infant mortalities that can be screened out during a regular burn-in process. Indeed, these construction defects are minor and may not cause any failure for years when used at regular use-level conditions [25]. But minor construction defects and contamination were also revealed in the capacitors that failed either with a slow degradation or with a thermal runaway, as shown in Figure 9. Finally, many BME capacitors that failed with slow degradation did not have any noteworthy physical features, suggesting an intrinsic failure mode that involves a dielectric chemistry change or regular wearout [31].

If the extrinsic minor construction defects are the root cause of the "early time failures," the external levels of stresses are the trigger for the failures. When the stress level is set moderately, some of the extrinsic defects will

result in early avalanche failures, while others will stay benign for a long time and may never fail. As the external stress level increases, the extrinsic minor defects that may not cause any failure at lower stress levels will begin to fail quickly. Some of the extrinsic defects may never cause actual failures prior to the failure occurrence due to another failure mechanism.

The dielectric thickness must have played an important role for the occurrence of "early time failures." At a given testing voltage level, the capacitors with thicker dielectrics will have less intense electric strength and therefore will either delay or not trigger the existing defects to cause failure if the same voltage level will cause "early time failures" in BME capacitors with thinner dielectrics. As a result, the dielectric thickness is more like a secondary trigger mechanism than the cause of an early avalanche breakdown in BME capacitors. Therefore, there must be a minimum dielectric thickness for a BME capacitor with a certain rated voltage so that the capacitors will be failure-free for a desired period of time at the regular use-level stress (i.e., room temperature and rated voltage) and will also survive the life testing requirements at higher stress levels (e.g., 125 °C, twice the rated voltage). For high-reliability applications, the actual dielectric thickness should be determined with enough margins to prevent the occurrence of early failures. As shown in Figure 8, the MTTF of PME capacitor D04X10310 is better than that of all of the BME capacitors that are 25V-rated; however, this PME capacitor is only rated at 10V, with a measured dielectric thickness of ~15 μm.

In order to eliminate/minimize "early time failures" in BME capacitors, the concentration of extrinsic defects must be carefully controlled and reduced during the manufacturing of the BME capacitors. Manufacturers are advised to review their fabrication steps carefully to avoid any contaminations and to modify their processing to prevent the introduction of stress that may result in cracks and delamination. Secondly, an appropriate dielectric thickness needs to be determined so that the actual stress level will not trigger any of the "early time failures" at a use-level for the desired life cycles of the capacitors. When the dielectric layer thickness goes to micron or submicron levels, the impact of the dielectric layer thickness on reliability becomes more crucial. This is due to the fact that a slight change in the thickness will result in a significant change in the external stress level when the dielectric layer is very thin.

Summary

A number of commercial high-capacitance BME capacitors and some PME capacitors with thinner dielectrics (<20 μm) were evaluated for potential high-reliability applications. The capacitors were first subjected to a construction analysis per EIA standard EIA/ECA-469D. All of the capacitors met the requirements, with a significant margin area available for the construction of extra capacitance.

Cross-section SEM examination shows that all BME capacitors exhibit a dense and uniform microstructure, with an average grain size of 0.3~0.5 microns that is much less than that of PME capacitors. This is the main reason that BME capacitors can be fabricated with much thinner dielectric layers than PMEs at the same rated voltage, and it also explains why high capacitance volumetric efficiency can be achieved in BME capacitors. All PME capacitors exhibit a microstructure with large grains and a low-melting liquid phase.

Highly accelerated life testing has been applied for the reliability evaluation of BME and PME capacitors. Most of the BME capacitors reveal a regular dielectric wearout failure mode, characterized with Weibull slope parameter β of 2.4~9.5, temperature activation energy E_s of 1.0~2.0 eV, and voltage accelerating factor $n = 4$~5. A number of "early time failures" characterized with avalanche breakdown were also found for most BME capacitors. When "early time failures" are removed from the Weibull calculations, BME capacitors exhibit a minimum median life of more than 10^5 years. On the other hand, all PME capacitors reveal a classic random failure mode with β~1, E_s ~1.0 eV, and n~3.0, indicating the failure mode in PME capacitors is different from that in BME capacitors.

Dielectric thickness was found to be a critical parameter for the reliability of BME capacitors. The number of stacked grains in a dielectric layer appears to play a significant role in determining BME capacitor reliability. Although the dielectric layer thickness varies, the number of stacked grains is relatively consistent for BME

capacitors with the same rated voltage. This may indicate that the number of grains per dielectric layer is more critical than the thickness itself for determining the rated voltage and the life expectancy of a BME capacitor.

Failure analysis data indicate that the "early time failures" of BME capacitors, characterized by leakage-current avalanche breakdown, can be attributed to extrinsic minor construction defects that were introduced during the fabrication of the BME capacitors. Whether an extrinsic defect will actually result in a failure depends on the external stress levels.

There are two approaches to prevent/reduce "early time failures": (1) reduction of extrinsic defects with improved BME capacitor processing technology, and (2) prevention of BME capacitors from being used under harsh external stress levels. This requires the careful control of dielectric layer thickness for a given rate voltage. A minimum dielectric thickness is necessary for BME capacitors if they are used for high-reliability applications. As the dielectric layer thickness goes to the micron or submicron range, the role of dielectric thickness and the number of stacking grains will be more significant for the life reliability of BME capacitors.

Acknowledgements

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