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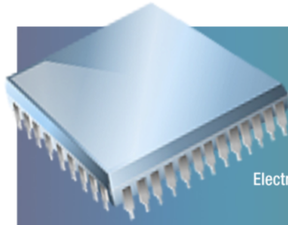

EEE Parts Bulletin

Electrical, Electronic, and Electromechanical

A periodic newsletter of the JPL/OSMS Assurance Technology Program Office (ATPO), NASA EEE Parts Assurance Group (NEPAG), and Section 514, of the Jet Propulsion Laboratory.

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Class Y Special Issue

This issue of the *EEE Parts Bulletin* introduces Class Y, a new category of microcircuits. Class Y brings the Xilinx Virtex-4 field-programmable gate array (FPGA), the Virtex-5 FPGA, and similar devices into the Qualified Manufacturer List (QML) as standard space products. The Class Y development is an effort to infuse new packaging technology into the QML with the benefits of schedule and cost savings to flight projects. The space community has been working to develop the necessary screening and qualification requirements for Class Y. The snapshot below summarizes these activities, and the diagram on the next page provides major milestones for this development.

Task Group Inputs

- Government
- Manufacturers
- Primes
- Others

G12 Class Y Task Group Non-Hermetics in Space

Task Group Activities

- ☑ Review M. Sampson Idea
- ☑ Class Y Concept Development
- ☑ EP Study (DLA-VA)
- ☐ Coordination Meeting at DLA Land & Maritime (April 2012)
- ☐ Add Class Y Requirements to 38535 and 883 (DLA-VA)
- ☐ Manufacturer Certification to QML-Y (DLA-VQ)

Supplier PIDTP* Presentation

- ☑ Aeroflex (October 2011)
- ☑ Xilinx (February 2012)
- ☐ Honeywell (May 2012)
- ☐ BAE (October 2012)

Conference

- ☑ Non-Hermetic Conference Jan. 2012, Orlando
- ☑ CMSE (Feb. 2012), LA

Newly Formed Task Groups with Class Y Interest

- JC13.2 Electronic Parameters & B.I. Standardization
- JC13.2 Flip-chip Package BGA / CGA Requirements
- G12 & G11 Passives Device Requirements in 38535

Other Task Groups with Class Y Interest

- G12 Plastics Subcommittee
- JC13.2 5004/5 vs. 38535 Tables & 883 vs. 38535 Comparison
- JC13 Overlapping Device Definitions 38534 vs. 38535

* PIDTP = Package Integrity Demonstration Test Plan

Milestones on the Road to QML–Y Space Flight Parts Procurement

- ☑ G12 approval of TG charter
- ☑ G-12 Class Y Task Group to develop requirements
- ☑ G12 approval for DLA-VA to commence EP study
- ☑ DLA-VA to conduct EP study
- ☑ DLA-VA to release “final” report
- ☐ Coordination meeting at DLA Land and Maritime (April 2012)
- ☐ DLA-VA to update 38535 and 883 with Class Y requirements
- ☐ DLA-VQ to begin audit of suppliers to Class Y requirements
  – Users to procure QML-Y flight parts from certified/qualified suppliers

The Why of Class Y: Infusing New Technology into the QML System

The Class Y development’s primary effort is to bring advancements in packaging technology into the Qualified Manufacturer List (QML) system.

Advancements in packaging technology, increasing functional density, and increasing operating frequency have resulted in single-die System-on-a-Chip (SoC) with non-hermetic flip-chip construction in high-pin-count ceramic column-grid array (CGA) packages. The “Poster Child” for this is the Virtex 4 (V-4) field-programmable gate array (FPGA) from Xilinx.

Such products have been evaluated for radiation and reliability, and they have drawn the attention of the space user community. The diagram on the previous page illustrates the status of this effort.

Class Y originated with the posing of this question: how can we bring Xilinx V-4 FPGA and similar microcircuits into the QML system as standard space products. Class V is not appropriate because that classification is intended only for hermetic devices. Mike Sampson, the Manager of NASA Electronic Parts and Packaging (NEPP) Program, suggested that a new category be created: “Class Y”. In early 2010, G12 opened a Task Group to develop screening and qualification requirements for Class Y.

Failing to pursue development of Class Y would be a detriment for the space community and the QML program at large because the industry users would be limited to ordering via Source Control Drawings (SCDs), which is counterproductive to Mission Assurance, prevents standardization, and is expensive.

G12 Task Group TG2010-01

Shri Agarwal, Manager of the NASA EEE Parts Assurance Group (NEPAG), was asked to lead the new G12 Task Group, TG 2010-01, which was formed to address non-hermetic microcircuits for space. This task was challenging because it:

- Was far more involved than typical G12 tasks.
- Required development of a new concept.
- Used system-on-a-chip—one of the most complicated device types.
- Needed to be simple and easily understood.
- Possessed sketchy testing and board-assembly boundaries.
- Was needed to procure a standard QML product as quickly as possible.

Current Status

The Document Standardization Division of Defense Logistics Agency (DLA-VA) has completed an Engineering Practice (EP) study for Class Y. The EP study is the peer review on a very large scale: done by the agencies, military services, part manufacturers, and other space-application parts user communities (prime contractors and others).

G12 Class Y Task Group (TG) Summary

- The Class Y TG is run by representatives from NASA, The Aerospace Corporation, Boeing Corporation, and DLA-VA, with management support from NASA, DLA-VA, DLA-VQ, G12, and JC13.
- The TG developed requirements, including qualification and screening standards for non-hermetic, ceramic-based microcircuits suitable for space applications. The effort focused on support for devices using flip-chip ceramic CGA packages. The resulting requirements were submitted to DLA-VA for coordination and documentation.
- Boeing’s proposed “simplified approach” was adopted. Paragraphs were proposed to be added to existing MIL-PRF-38535, Appendix B, showing differences for Class Y (from those for Class V). One key element that distinguishes Class Y from Class V is the Package Integrity Demonstration Test Plan (PIDTP). The manufacturers will be required to submit a PIDTP to the Qualifying Activity (QA) of DLA.

This plan must address issues unique to non-hermetic construction and materials, such as potential materials degradation, interconnect reliability, thermal management, resistance to processing stresses, resistance to thermo-mechanical stresses, and shelf life. The PIDTP plan shall be approved by QA after consultation with the space community.

- To date, ten manufacturers have expressed interest in offering Class Y products: Xilinx, Aeroflex, Honeywell, BAE, Actel, Intersil, TI, e2v, 3D Plus, and Cypress.
- According to a poll of major manufacturers, the set of 38535 classes, with Class Y added, will cover microcircuits for the next several years.
- It is impractical to subject any CGA configuration to all the regular screening steps required for flight-worthy microcircuit devices. Users should be aware of this limitation of CGAs.
- DLA Land & Maritime is hosting a Class Y coordination meeting (April 2012) for discussion on the final report of the EP study with the agencies, military services, part manufacturers, and other space-application parts user communities (prime contractors and others).
- Task group meeting discussions led to the realization that there were other related important issues that needed attention. These issues related to non-hermeticity needed to be separated from those related to solder terminations. Additionally, there were some generic issues that applied to both hermetic and non-hermetic devices. Therefore, additional task groups were formed to begin addressing these new issues. Given below is a brief description:
  - Clarification is needed on burn-in (B.I.), electricals, and delta requirements. This is a major issue for all microcircuits, and it applies to Class Y products as well. For instance, statements such as, “A certain FPGA device has undergone 4000 hours of life test with parts biased in a static condition,” begs the question as to why an FPGA (basically a digital part) was not subjected to a dynamic condition. Conversely, doing a dynamic B.I. on a voltage reference should not be a requirement. There are other questions related to the activation energy, low-temperature burn-in, etc. A JC13 Task Group (chaired by Brent Rhoton of Texas Instruments) was formed to clarify and update requirements in MIL-STD-883, Method 5004, which defines the screening requirements for microcircuits.
  - Due to their tiny sizes and low-voltage operation, the Base Metal Electrode (BME) capacitors are preferred for use in microcircuit packages. The screening/qualification requirements for BME signal conditioning capacitors should be clearly stated (refer to MIL-PRF-38535, Paragraphs 3.15 and 3.15.1). What is the attachment method of the BME capacitors used in many designs? During the G12 meeting, some manufacturers commented that they use epoxy or silver glass die attachment material to adhere the capacitor to the internal portion of the IC package. Others use only solder attachment. A JC13 Task Group (chaired by Larry Harzstark) was opened to address these issues. The BMEs are commercial parts and require screening and qualification. They are not considered as reliable as the widely used MIL-qualified Precious Metal Electrode (PME) construction capacitors. Because of their tiny size, the BMEs pose handling and testing challenges. We would not want any performance degradation of a Class Y part due to the failure (e.g., shorting of terminals) of a vastly less costly part. A team of capacitor experts will be assembled to recommend the proper screening requirements for BMEs. It should be noted that not all manufacturers are using BMEs.
  - Solder-terminated parts (either hermetic or non-hermetic) need attention. The Class Y TG proposed a paragraph to add to MIL-PRF-38535, Appendix B. To define this language, the JC-13.2 Task Group on solder terminations has been formed (chaired by Trish Hertog of Honeywell). The broad issues include: solderability, storage and shelf life, electrical testing, reworks, pull test, and termination definition (e.g., tin–lead solder based). Some specific questions being addressed are:
    - What is the shelf life of the CGA? Specifically, how long will these parts be 100% solderable? Is this guaranteed?
    - As the columns would tend to oxidize when exposed to atmosphere, should they be stored in sealed dry bags or stored in dry nitrogen?
    - Do all internal and external portions of the flip-chip package pass MIL-STD-883, Method 5011 (re-eval of polymeric materials)?
    - Once assembled, can the finished CGA (like all other microcircuits, transistors, and hybrids) be functionally tested at –55°C, +25°C, and +125°C? If the solder melting point is estimated at about 180°C, it could be risky to electrically test the parts at +125°C case temperature. Conversely, are there any cold brittle concerns at –55°C?
    - What board-level / assembly-level tests have been run on CGAs?
    - What is the maximum number of allowable column reworks for space products?
    - What are the specifications for column-pull test?
    - What is being done to avoid handling damage and ESD-related damage to the parts?
    - What are the needed details for inspection of CGAs (area arrays, in general)?

- What tests should be done on CGAs prior to their installation on flight boards?
- Are application notes needed on CGAs after column attach so that the users understand any temperature limitations, adequacy of visual inspection, cleanliness, fluxes to avoid, etc.?
- Coordination with IPC: what are the boundaries that separate JEDEC work from IPC?

NASA OSMA-Funded Tasks

The NASA Office of Safety and Mission Assurance (OSMA) NEPP Program (co-managed by Mike Sampson and Ken LaBel of GSFC) has funded several tasks in FY12 to provide support to the Class Y effort. At JPL, the NEPP and NEPAG programs are run under the auspices of the Assurance Technology Program Office (ATPO), Office 502, managed by Dr. Chuck Barnes. The evaluations of underfill and BME capacitors are examples of the tasks being worked.

Summary

An effort as large as Class Y requires extensive work given the many technical issues involved specific to the technologies being dealt with. It is also necessary to coordinate with the community, and the manufacturers while following the established processes. The continued collaboration of the Class Y team with NASA, JC13, G12, DLA Land & Maritime, and other entities is critical to the completion of this task. Periodic progress will be reported via these bulletins. The milestones list at the top of page 2 shows the progress towards flight parts procurement.

For further information, contact:

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GIDEP Alerts/Advisories

Contact your GIDEP Representative for a copy of:

Suspect Counterfeit	HO6-A-12-01 Microcontroller 12 kbytes flash; L1-A-12-04 Switch, Protected Power; DU5-A-12-01 Quad Low Power Video Buffer; B5-A-12-02 8-bit Microcontroller; ZW-A-11-01B RS-232 Transceiver; B5-A-12-02 8-Bit Microcontroller; E1C-A-12-01 Microcircuit, Linear; GG5-A-12-03 Transparent Asynchronous Transmitter/Receiver Interface; GG5-A-12-04 Digital Programmable Clock Generator; B9-A-12-06 Sensor; B9-A-12-07 Microcontroller; B9-A-12-08 Microcircuit, Low Power; B9-A-12-09 Flash File Memory
Misc.	AKZ-P-12-01 Traceability issue with supplier; SC7-P-12-01 Signal Coupling in Deeply-Cascaded SRAM Blocks, RTAX-S/SL/DSP, FPGA; EJ7-P-12-01 Detector Assembly, Overheat, Fire, Upper Fan; SC7-P-12-02 Silicon Sculptor II software Support of AX1000, AX2000, RTAX2000S/SL/DSP and RTAX4000S/SL/DSP Devices; UV5-A-12-01A Microcircuits, Schottky, Bipolar

NASA parts specialists recently supported DLA Land and Maritime Audits of:

Sensitron, NY; MIcrosemi, MA; Micropac Industries, Inc., TX; e2v Aerospace & Def., CA; Microsemi Corp. (Actel), CA; Microsemi Lawrence, MA; Cypress Semiconductor, CA; Teledyne Cougar Inc., CA; International Rectifier, CA; Semicoa Corp., CA; IBM (Aeroflex), NY.

Upcoming Meetings

- ECTC 2012, 62nd Electronic Components and Technology Conference, San Diego, May 29–June 1, 2012 http://www.ectc.net
- JEDEC JC-13, Committee on Government Liaisons at the Chateau Bourbon, New Orleans, May 21–24, 2012

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