<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>PREP BY</th>
<th>DESCRIPTION</th>
<th>DATE</th>
<th>APPROVAL</th>
</tr>
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<tr>
<td></td>
<td>Maurice J. Robertson</td>
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<td></td>
<td>Albert Lunchick</td>
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</table>

**TITLE**

Screening Procedure for a Medium Power, ENP, Silicon Transistor (2N4236)

**SP 73-15070**

Branch - Parts
Division - Quality Assurance
Project - IUE

GODDARD SPACE FLIGHT CENTER
GREENBELT, MARYLAND
1. **SCOPE**

This procedure covers the screening requirements for a Medium Power, EPN, Silicon Transistor (2N4236).

2. **APPLICABLE DOCUMENTS**

The following documents form a part of this specification to the extent specified herein.

- **MIL-STD-202** Test Methods for Electronic and Electrical Component Parts
- **MIL-STD-750** Test Methods for Semiconductor Devices

3. **TEST PROCEDURES AND REQUIREMENTS**

3.1 **External Visual Inspection**

Examine all transistors with a microscope at a minimum of 10X magnification:

(a) Verify that all markings are in accordance with the manufacturer's data sheets.

(b) Inspect all transistors for defects in workmanship.

(c) Verify that all materials, design and construction are in accordance with the manufacturer's data sheets. Determine if the leads are solder or gold plated.

3.2 **Initial Measurements**

Make all the electrical parameter measurements listed in Table I. All measurements made at $T_A = 298 \, K \pm 3 \, K$ unless otherwise specified. Devices shall be serialized at this time.

3.3 **High Temperature Storage**

473 K for 48 hours. (If the leads are tinned or solder plated, reduce the test temperature to 398 K.)
3.4 Thermal Shock (Temperature Cycling)

Method 1051 of MIL-STD-750 (Method 107 of MIL-STD-202), Test Condition C, except 10 cycles total, 15 minute rest at each temperature extreme. (If the leads are tinned or solder plated, reduce the test temperature to 398 K.)

3.5 Acceleration

MIL-STD-750, Method 2006, at 20,000 G, in Y1 orientation only, one time only. The one minute hold-time requirement shall not apply.

3.6 Hermetic Seal (Fine Leak) Test

Test for a maximum leak rate of $10^{-8}$ atm cc/sec per Test Condition G or H of Method 1071 of MIL-STD-750.

3.7 Hermetic Seal (Gross Leak) Test

Test Condition C of Method 1071 of MIL-STD-750.

3.8 Reverse Bias Burn-In

<table>
<thead>
<tr>
<th>Time</th>
<th>Temperature</th>
<th>Collector to Base Voltage</th>
<th>Emitter Current</th>
</tr>
</thead>
<tbody>
<tr>
<td>(T)</td>
<td>(T_A)</td>
<td>(V_CB)</td>
<td>(I_E)</td>
</tr>
<tr>
<td>48 hours</td>
<td>448 K for gold plated leads; 398 K for tinned leads</td>
<td>-60 Vdc</td>
<td>0</td>
</tr>
</tbody>
</table>

After the 48 hour burn-in, the collector to base voltage ($V_{CB}$) shall be maintained on the devices until the ambient temperature ($T_A$) is 303 ± 5 K.

3.9 Postburn-In Electrical Parameter Measurements

The postburn-in electrical parameter measurements shall be made within 24 hours of the conclusion of burn-in. The test measurements are listed in Table II and shall be performed at an ambient temperature ($T_A$) of 298 K ± 5 K. These test measurements will be used as preburn-in electrical parameter measurements for the power burn-in and used in the calculation of the delta ($\Delta$) changes during and following the power burn-in.
3.10 Power Burn-In

<table>
<thead>
<tr>
<th>Time</th>
<th>Temperature (T)</th>
<th>Collector to Base Voltage (T_A)</th>
<th>Total Power Dissipation (V_CB)</th>
<th>(P_T)</th>
</tr>
</thead>
<tbody>
<tr>
<td>168 hours</td>
<td>298 K ±3 K</td>
<td>-10 Vdc</td>
<td>1.0 W</td>
<td></td>
</tr>
</tbody>
</table>

Notes: 1. Before burn-in of the lot is started, three transistors from the lot shall be subjected to a 24-hour burn-in followed by the postburn-in measurements. If any part fails the postburn-in limits or delta criteria, the burn-in test setup shall be reevaluated.

2. After 96 hours of burn-in remove devices from test and subject them to the postburn-in tests. Then continue the burn-in for the remaining 72 hours.

3.11 Postburn-In Electrical Parameter Measurements

Make all the electrical parameter measurements listed in Table II. All measurements made at T_A = 298 K ±3 K unless otherwise specified.

3.12 Parameter Change Criteria

All devices exhibiting parameter changes between the preburn-in electrical parameter measurements (paragraph 3.9) and the postburn-in electrical parameters which are not within the ranges indicated below, shall be rejected.

\[
\Delta I_{CB0} = 100\% \text{ or 25 nanoamperes, whichever is greater}
\]

\[
\Delta h_{FE} = \pm 15\%
\]

3.13 Final Measurements

Make all the electrical parameter measurements listed in Table I. All measurements made at T_A = 298 K ±3 K unless otherwise specified.
4. LOT ACCEPTANCE

When more than 10 percent of the lot fails screening, the entire lot shall be subject to rejection. The Applications Section shall be notified when any lot is subject to rejection.

5. DATA

A copy of the data generated during this test shall be sent to the Applications Section.

6. MARKING

Each device that is screened to the requirements of this specification shall receive a serial number that remains with the device when it is returned to the requester along with the test data.
### Table 1. Initial and Final Electrical Measurements

<table>
<thead>
<tr>
<th>Test</th>
<th>Symbol</th>
<th>Method</th>
<th>Details</th>
<th>Limits</th>
<th>Unit</th>
</tr>
</thead>
</table>
| Collector-emitter sustaining voltage      | BVCEO(sus)              | 3011   | $I_C = 100 \, \text{mA}$  \(I_B = 0\)  
Bias Condition D  
See Note 1 | 80     | Vdc  |
| Collector to emitter cutoff current       | ICE0                    | 3041   | $V_{CE} = 60 \, \text{Vdc}$  
$V_{BE(off)} = 1.5 \, \text{Vdc}$  
Bias Condition D | ---    | 1.0  mAdc |
| Collector to emitter cutoff current       | ICEX                    | 3041   | $V_{CE} = 80 \, \text{Vdc}$  
$V_{BE(off)} = 1.5 \, \text{Vdc}$  
Bias Condition D | ---    | 0.1  mAdc |
| Emitter to base cutoff current            | IEB0                    | 3061   |  $V_{EB} = 7.0 \, \text{Vdc}$  
$I_C = 0$  
Bias Condition D | ---    | 0.5  mAdc |
| Forward current transfer ratio            | $h_{FE}$                | 3076   | $V_{CE} = 1.0 \, \text{Vdc}$  
$I_C = 100 \, \text{mA}$  
See Note 1 | 40     | ---  |
| Forward current transfer ratio            | $h_{FE}$                | 3076   | $V_{CE} = 1.0 \, \text{Vdc}$  
$I_C = 1.0 \, \text{A}$  
See Note 1 | 10     | ---  |
| Small signal forward current transfer ratio | $h_{fe}$               | 3306   | $V_{CE} = 10 \, \text{Vdc}$  
$I_C = 50 \, \text{mA}$  
$f = 1.0 \, \text{kHz}$ | 2.5    | ---  |
<table>
<thead>
<tr>
<th>Test</th>
<th>Symbol</th>
<th>Method</th>
<th>Details</th>
<th>Limits</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Base-emitter saturation voltage</td>
<td>VBE(sat)</td>
<td>3066</td>
<td>I_C = 1.0 Adc, I_B = 100 mAde, See Note 1</td>
<td>1.5</td>
<td>Vdc</td>
</tr>
<tr>
<td>Collector emitter saturation voltage</td>
<td>VCE(sat)</td>
<td>3071</td>
<td>I_C = 1.0 Adc, I_B = 125 mAde, See Note 1</td>
<td>0.6</td>
<td>Vdc</td>
</tr>
<tr>
<td>Collector to base cutoff current</td>
<td>I_CBO</td>
<td>3036</td>
<td>V_CB = 80 Vdc, I_E = 0, Bias Condition D</td>
<td>100</td>
<td>nAde</td>
</tr>
<tr>
<td>Base-emitter on voltage</td>
<td>VBE(on)</td>
<td>3066</td>
<td>I_C = 250 mAde, V_CE = 1.0 Vdc</td>
<td>1.0</td>
<td>Vdc</td>
</tr>
<tr>
<td>Output capacitance</td>
<td>C_0b</td>
<td>3236</td>
<td>V_CB = 10 Vdc, I_E = 0, f = 100 kHz</td>
<td>100</td>
<td>pF</td>
</tr>
<tr>
<td>Forward current transfer ratio</td>
<td>h_FE</td>
<td>3076</td>
<td>V_CE = 1.0 Vdc, I_C = 250 mAde, See Note 1</td>
<td>30-150</td>
<td></td>
</tr>
</tbody>
</table>

Note 1. Pulse Test: PW ≤ 300 µs, Duty Cycle ≤ 2%.
### TABLE II. PREBURN-IN AND POSTBURN-IN ELECTRICAL PARAMETER MEASUREMENTS

<table>
<thead>
<tr>
<th>Test</th>
<th>Symbol</th>
<th>Method</th>
<th>Details</th>
<th>Limits</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Collector to base cutoff current</td>
<td>$I_{CB0}$</td>
<td>3036</td>
<td>$V_{CB} = 80 \text{ Vdc}$ $I_E = 0$ Bias Condition D</td>
<td>--</td>
<td>100</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>nAdc</td>
</tr>
<tr>
<td>Forward current transfer ratio</td>
<td>$h_{FE}$</td>
<td>3076</td>
<td>$V_{CE} = 10 \text{ Vdc}$ $I_C = 250 \text{ mA}_{dc}$ See Note 1</td>
<td>30</td>
<td>150</td>
</tr>
</tbody>
</table>

Note 1. Pulse Test: $PW \leq 300 \mu s$, Duty Cycle $\leq 2\%$. 