REVISIONS

SYMBOL	DESCRIPTION	DATE	APPROVAL
---	Released	7/22/94	

SHEET REVISION STATUS

SH	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
REV	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--
SH	21	22	23	24																
REV	--	--	--	--																
SH																				
REV																				

ORIGINATOR R. Williams/UNISYS	DATE 7/20/94	FSC: 5962
APPROVED S. Archer-Davies / UNISYS	7/24/94	Control Drawing for a Radiation Tolerant, 32K X 8 CMOS EEPROM (Generic No. U28C256E)
CODE 311 APPROVAL B. Fafaul / GSFC	7/21/94	
CODE 311 SUPERVISORY APVL R. Chinnapongse / GSFC	7/21/94	
		S-311-P-783

NATIONAL AERONAUTICS AND SPACE ADMINISTRATION
GODDARD SPACE FLIGHT CENTER
GREENBELT, MARYLAND 20771

CAGE CODE: 25306

1.0 SCOPE

1.1 Scope. This specification control drawing defines the requirements for a radiation tolerant, 32K X 8 CMOS Electrically Erasable Programmable Read-only Memory (EEPROM) herein after referred to as the "device".

1.2 Part number. The part number shall be as shown:

G311P-783-200

1.2.1 Device type. The device is a 28C256 CMOS EEPROM, capable of withstanding a minimum of 10 Krad (Si) total dose irradiation in space and still meeting the electrical requirements herein.

1.2.2 Die type. The die in the device is monolithic silicon (32k x 8) 256k EEPROM, EPI substrate, SEEQ manufacture @ Signetic foundry P/N U28C256E, Process P402/QL1U Rev. J, Layer Rev. 5845, XSC1021 series, SIG22 Fab.

1.2.3 Case outline. The case shall be a 28 lead, dual-in-line package as specified in Figure 1.

1.3 Absolute maximum ratings

All input and output voltages (including VCC)1/	-0.5 VDC to 6.0 VDC
Operating case temperature range	-55°C to +125°C
Storage temperature range	-65°C to +150°C
Voltage for chip clear (Vh)	+15.0 VDC
Maximum power dissipation (Pd)	1.0 W

1.4 Recommended operating conditions.

Supply voltage range (VCC)	+4.5 VDC to +5.5 VDC
Case operating temperature (TC)	-55°C to +125°C
Input voltage, low range (VIL)	-0.1 VDC to +0.8 VDC
Input voltage, high range (VIH)	+2.0 VDC to VCC +0.3 VDC

2.0 APPLICABLE DOCUMENTS

2.1 The following documents form a part of this drawing to the extent specified herein. In the event of conflict between this control drawing, the procurement document and applicable documents, the order of precedence shall be the procurement document, this control drawing and the applicable documents.

SPECIFICATIONS

Military

MIL-I-38535	Integrated Circuits (Microcircuits) Manufacturing, General Specification for
MIL-M-38510/261	Microcircuits, Memory, Digital, CMOS 32 X 8-bit, Electrically Erasable Programmable Read-only Memory (EEPROM), Monolithic Silicon
MIL-M-55565	Microcircuits, Preparation for Delivery of

STANDARDS

Military

MIL-STD-883 Test Methods and Procedures for Microcircuits
MIL-STD-1285 Marking of Electrical and Electronic Parts
MIL-STD-45662 Calibration System Requirements

HANDBOOKS

Military

DOD-HDBK-263 Electrostatic Discharge Control Handbook for Protection of Electrical and Electronic Parts, Assemblies and Equipment

2.2 Order of precedence. In the event of a conflict between the text of this specification and the references cited herein, the text of this specification shall take precedence.

3.0 REQUIREMENTS

3.1 Detail specification. The device shall conform to engineering practices consistent with the requirements in this control drawing and MIL-STD-883 as specified herein. Details of design, construction, materials, and finishes not specified herein shall be such that the device shall meet all the requirements of MIL-I-38535, Appendix 'A'.

3.2 Design, construction and physical dimensions. The design, construction and physical dimensions shall be as specified herein.

3.2.1 Terminal connections. The terminal connections shall be as specified in Figure 2.

3.2.2 Truth table.

3.2.2.1 Unprogrammed or erased devices. The truth table for unprogrammed devices shall be as specified in Figure 3.

3.2.2.2 Programmed devices. The requirements for supplying programmed devices are not part of this specification.

3.2.3 Case outlines. The case outlines shall be as specified in 1.2.3.

3.3 Lead finish. Lead finish shall be in accordance with MIL-M-38510, Type C, gold plated.

3.4 Electrical performance characteristics. Unless otherwise specified, the electrical performance characteristics are as specified in Table I, and shall apply over the full case operating temperature range specified. Test conditions for the specified electronic performance characteristics are as specified in Table I.

3.5 Electrical test requirements. The electrical test requirements shall be the subgroups of Table II. The electrical tests for each subgroup are described in Table I.

3.6 Marking. Marking shall be in accordance with MIL-STD-883. The parts shall be marked with the part number listed in 1.2 herein, date code, serial number, vendor logo and/or CAGE code, and country of origin.

3.7 Programming of EEPROMS. When specified, devices shall be programmed in accordance with the procedures and characteristics specified in 4.5.3.

3.8 Certificate of conformance. A certificate of conformance as required in MIL-STD-883 shall be provided with each lot of microcircuits delivered to this specification.

4.0 QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Inspection procedures shall be in accordance with MIL-STD-883, Method 5005, except as modified herein.
4.2 Screening. Screening shall be in accordance with Method 5004 of MIL-STD-883, Method 5004, for Class S and shall be conducted on all devices prior to qualification and quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, Method 1015 of MIL-STD-883.

(1) Test condition D using the circuits shown in Figure 4.

(2) TA = 125°C, minimum

(3) Prior to burn-in the devices shall be programmed (see 3.7) with the data pattern shown in Figure 5. The pattern shall be read before and after burn-in. Devices having bits not in the proper state after burn-in shall constitute a device failure.

b. Interim and final test parameters shall be as specified in Table II. The following data patterns shall be included in Group A, Subgroup 7: All 0's, all 1's, checkerboard, and checkerboard complement. Each temperature shall include, at a minimum, the programming of one data pattern. Subgroups 9, 10 and 11 shall be performed on devices containing a checkerboard and a checkerboard complement data pattern or equivalent alternating bit and complementary data patterns.

c. After the completion of all screening, the devices shall be erased and verified prior to delivery.

4.3 Quality conformance inspections. Quality conformance inspection shall be in accordance with Method 5005 of MIL-STD-883, Groups A, B, C, and D.

4.3.1 Group A inspection. Group A inspection shall be in accordance with MIL-STD-883, Method 5005, Table I and as follows:

a. Electrical test requirements shall be as specified in Table II herein.

b. Subgroups 4, 5 and 6 of MIL-STD-883, Method 5005, Table I shall be omitted.

4.3.2 Group B inspection. Group B inspection shall be in accordance with MIL-STD-883, Method 5005, Table II, Class S except as modified herein.

a. End-point electrical tests shall be as specified in Table II herein.

b. All devices requiring end-point electrical testing shall be programmed with the pattern shown on figure 5.

c. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition D as specified in figure 4.

(2) Ambient temperature = 125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

(4) Read the pattern after burn-in and perform end-point electrical tests in accordance with table II herein for group C.

(5) Sample size shall be LTPD=10 or 22(0).

d. An endurance test, in accordance with method 1033 of MIL-STD-883, shall be added to group B inspection prior to performing the steady state life test (see 4.3.2c) and extended data retention (see 4.3.2e). Cycling may be block, byte, or page from devices passing group A after the completion of the requirements of 4.2 herein. Initially, two groups shall be formed cell 1 and cell 2.

The following conditions shall be met:

(1) Cell 1 shall be cycled at -55°C and cell 2 shall be cycled at +125°C for a minimum of 10,000 cycles.

(2) Perform group A subgroups 1, 7, and 9 after cycling. Form two new cells (cells 3 and cell 4) for steady-state life and extended data retention. Cell 3 for steady-state life test consists of one-half of the devices from cell 1 and one half of the devices from cell 2. Cell 4 for extended data retention consists of the remaining devices from cell 1 and cell 2.

(3) The sample plans for cell 1, cell 2, cell 3, and cell 4 shall individually be the same as for group B, as specified in method 5005 of MIL-STD-883.

e. Extended data retention shall test consist of the following:

(1) All devices shall be programmed with a charge on all memory cells in each device, such that the cell will read opposite the state that the cell would read in its equilibrium state (e.g., worst case pattern).

(2) Unbiased bake for 1000 hours (minimum) at +150°C (minimum). The unbiased bake time may be accelerated by using higher temperature in accordance with the Arrhenius Relationship.

$$AF = e^{\frac{E_A}{K}\left[\frac{1}{T_1} - \frac{1}{T_2}\right]}$$

E_A = activation energy
AF = acceleration factor (unitless quantity) = t_1/t_2
T = temperature in Kelvin (i.e., $t_1 + 273$)
t_1 = time (hours) at temperature T_1
t_2 = time (hours) at temperature T_2
K = Boltzmanns constant = 8.62×10^{-5} ev/°K using an apparent activation energy (EA) of 0.6 volt

The maximum storage temperature shall not exceed +200°C for packaged devices or +300°C for unassembled devices.

(3) Read the pattern after bake and perform end-point electrical tests for table II herein for group B.

4.3.3 Group C inspection. Group C inspection is not required for Class S devices.

4.3.4 Group D inspection. Group D inspection shall be in accordance with MIL-STD-883, Method 5005, Table IV and as follows:

a. End-point electrical tests shall be as specified in Table II herein.

b. The devices selected for testing shall be programmed with the pattern shown in Figure 5. After completion of all testing, the devices shall have the programmed pattern read, then be erased and verified. When the use of electrical rejects is permitted, no programming or erasure or verification is required.

4.4 Electrostatic discharge sensitivity. These devices are classified as Class 2 ESD sensitive devices per RAC, Electrostatic Discharge Susceptibility Data, Volume 1, 1989.

4.5 Methods of inspection. Methods of inspection shall be as specified in the appropriate tables and as follows.
4.5.1 Voltages and current. All voltages given are referenced to the microcircuit ground terminal. Currents given are conventional and positive when flowing into the referenced terminal.

4.5.2 Life test, burn-in, cooldown, and electrical test procedure. When devices are measured at +25°C following application of the steady-state life or burn-in test condition, all devices shall be cooled to +35°C or within +10°C of power stable condition prior to removal of bias voltages/signals. Any electrical tests required shall first be performed at -55°C or +25°C prior to any required tests at +125°C.

4.5.3 Programming procedure. The waveforms and timing relationships shown in Figure 6 (as applicable) and the conditions specified in Table I shall be adhered to. Initially and after each chip erasure , all bits are in the high state (output at VOH).

4.5.4 Erasing procedure. The waveforms and timing relationships shown in Figure 6 (as applicable) and the conditions specified in Tables I and III shall be adhered to. Initially and after each chip erasure, all bits are in the high state (output at VOH).

4.5.5 Test Equipment and Inspection Facilities. The manufacturer may use its own or any other facilities suitable for the performance of the inspection requirements. Test and measuring equipment shall have sufficient accuracy to permit performance of the required inspection. The supplier shall ensure that a calibration system is utilized and maintained to control the accuracy of the measuring and test equipment in accordance with MIL-STD-45662.

5.0 PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510.

6.0 NOTES

TABLE I. Electrical performance characteristics.

Test	Symbol	Condition $-55°C \le T_C \le +125°C$ $V_{SS} = 0$ V 1/ $4.5V \le V_{CC} \le 5.5$ V unless otherwise specified	Group A Subgroups (test method)	Limits		Unit
				Min	Max	
Supply current (active)	I_{CC1}	$\overline{CE} = \overline{OE} = V_{IL}$, $\overline{WE} = V_{IH}$, all I/O's = open, inputs = Vcc = 5.5 V	1, 2, 3 (3005)		80	mA
Supply current (TTL standby)	I_{CC2}	$\overline{CE} = V_{IH}$, OE = V_{IL}, all I/O's = open, inputs = V_{CC} - 0.3 V	1, 2, 3 (3005)		3	mA
Supply current (CMOS standby)	I_{CC3}	$\overline{CE} = V_{CC}$ - 0.3 V, all I/O's = open inputs = V_{IL} or V_{CC} -0.3 V	1, 2, 3 (3005)		350	µA
Input leakage (high)	I_{IH}	V_{IN} = 5.5 V	1 (3010)	-100	+100	nA
			2, 3 (3010)	-1	+1	µA
Input leakage (low)	I_{IL}	V_{IN} = 0.1 V	1 (3009)	-100	+100	nA
			2, 3 (3009)	-1	+1	µA
Output leakage (high)	I_{OHZ} 2/	V_{OUT} = 5.5 V $\overline{CE} = V_{IH}$	1 (3021)	-500	+500	nA
			2, 3 (3021)	-10	+10	µA
Out leakage (low)	I_{OLZ} 2/	V_{OUT} = 0.1 V $\overline{CE} = V_{IH}$	1 (3020)	-500	+500	nA
			2, 3 (3020)	-10	+10	µA
Input voltage (low)	V_{IL} 3/		1, 2, 3 (3008)		0.8	V
Input voltage high	V_{IH} 3/		1, 2, 3 (3008)	2.0		V

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Condition $-55°C \le T_C \le +125°C$ $V_{SS} = 0$ V 1/ $4.5V \le V_{CC} \le 5.5$ V unless otherwise specified	Group A Subgroups (test method)	Limits		Unit
				Min	Max	
Output voltage low	V_{OL}	I_{OL} = 2.1 mA, V_{IH} = 2.0 V V_{CC} = 4.5 V, V_{IL} = 0.8 V	1, 2, 3 (3008)		0.45	V
Output voltage high	V_{OH}	I_{OL} = -400 µA, V_{IH} = 2.0 V V_{CC} = 4.5 V, V_{IL} = 0.8 V	1, 2, 3 (3008)		0.45	V
OE high leakage (chip erase)	I_{OE}	V_H = 13 V	1, 2, 3	-10	100	µA
Input capacitance	C_I 4/, 5/	V_I = 0 V, V_{CC} = 5.0 V, T_A = +25°C, f = 1 MHz	4 (3012)		10	pF
Output capacitance	C_O 4/, 5/	V_O = 0 V, V_{CC} = 5.0 V, T_A = +25°C, f = 1 MHz	4 (3012)		10	pF
Read cycle time	t_{AVAV} 6/	See Figure 6 (as applicable) 7/	9, 10, 11 (3003)	120 150 200 250		ns
Address access time	t_{AVQV}		9, 10, 11 (3003)	 250	120 150 200	ns
Chip enable access time	t_{ELQV}		9, 10, 11 (3003)		120 150 200 250	ns
Output enable access time	t_{OLQV}		9, 10, 11 (3003)		100	ns
Chip enable to output n low Z low Z	t_{ELQX} 5/		9, 10, 11 (3003)	0		ns
Chip disable output in high Z	t_{EHQZ} 5/		9, 10, 11 (3003)		80	ns

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Condition $-55°C \le T_C \le +125°C$ $V_{SS} = 0$ V 1/ $4.5V \le V_{CC} \le 5.5$ V unless otherwise specified	Group A Subgroups (test method)	Limits		Unit
				Min	Max	
Output enable output in low Z	t_{OLOX} 5/	See Figure 6 (as applicable 7/	9, 10, 11 (3003)	0		ns
Output disable to output in high Z	t_{OHOZ} 5/		9, 10, 11 (3003)		80	ns
Output hold from address change	t_{AXOX} 6/		9, 10, 11 (3003)	0		ns
Write cycle time	t_{WHWL1} t_{EHEL1} 6/	See Figure 6 (as applicable) 8/	9, 10, 11 (3003)		10	ns
Address setup time	t_{AVEL} t_{AVWL} 6/		9, 10, 11 (3003)		20	ns
Address hold time	t_{ELAX} t_{WLAX} 6/		9, 10, 11 (3003)	150		ns
Write setup time	t_{WLEL} t_{ELWL} 6/		9, 10, 11 (3003)	0		ns
Write hold time	t_{EHWH} t_{WHEH} 6/		9, 10, 11 (3003)	0		ns
OE setup time	t_{OHEL} t_{WHOL} 6/		9, 10, 11 (3003)	20		ns
OE hold time	t_{EHOL} t_{WHOL} 6/		9, 10, 11 (3003)	20		ns
WE pulse width (page or byte) write)	t_{ELEH} t_{WLWH1} 6/		9, 10, 11 (3003)	.150	1	µs

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Condition $-55°C \le T_C \le +125°C$ V_{SS} = 0 V 1/ $4.5V \le V_{CC} \le 5.5$ V unless otherwise specified	Group A Subgroups (test method)	Limits		Unit
				Min	Max	
Data setup time	t_{DVEH} t_{DVWH} 6/	See Figure 6 (as applicable) 8/	9, 10, 11 (3003)	50		ns
Delay to next write	t_{DVWL} t_{DVEL} 6/		9, 10, 11 (3003)		10	µs
Data hold time	t_{EHDX} t_{WHDX} 6/		9, 10, 11 (3003)	10		ns
Byte load cycle	t_{WHWL2} 6/ 9/ 11/	See Figure 6 (as applicable)	9, 10, 11 (3003)	.20	149	µs
Last byte loaded to data polling	t_{WHEL} t_{EHEL} 6/ 8/		9, 10, 11 (3003)		650	µs
CE setup time	t_{ELWL} 6/	See Figure 6 (as applicable) 10/	9, 10, 11 (3003)	5		µs
Output setup time	t_{OVHWL} 6/		9, 10, 11 (3003)	5		µs
CE hold time	t_{EHWH} t_{WHEH} 6/		9, 10, 11 (3003)	5		µs
OE hold time	t_{WHOH} 6/		9, 10, 11 (3003)	5		µs
High voltage	V_H 5/		9, 10, 11	12	13	V
WE pulse width (chip erase)	t_{WLWH2} 6/	See Figure 6 (as applicable)	9, 10, 11	150		ns
Data in high	t_{DHWL} 6/		9, 10, 11	5		µs

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Condition $-55°C \le T_C \le +125°C$ $V_{SS} = 0$ V 1/ $4.5V \le V_{CC} \le 5.5$ V unless otherwise specified	Group A Subgroups (test method)	Limits		Unit
				Min	Max	
Data high hold	t_{WHDX} 6/,10/		9, 10, 11	5		µs
Erase recovery	t_{OHEL} 5/		9, 10, 11		50	ms

1/ DC and read mode.

2/ Connect all address inputs and OE to V_{IH} and measure I_{OLZ} and I_{OHZ} with the output under test connected to V_{OUT}. Terminal conditions for the output leakage current test shall be as follows:

a. $V_{IH} = 2.0$ V; $V_{IL} = 0.8$ V.

b. For I_{OLZ}: Select an appropriate address to acquire a logic 1, on the designated output apply V_{IH} to CE. Measure the leakage current while applying the specified voltage.

c. For I_{OHZ}: Select an appropriate address to acquire a logic 0 on the designated output. Apply V_{IH} to $\overline{CE}$. Measure the leakage current while applying the specified voltage.

3/ A functional test shall verify the DC input and output levels and applicable patterns as appropriate. All address locations shall be tested.
Terminal conditions are as follows:

a. Inputs: H = 2.0 V; L = 0.8 V.

b. Outputs: H = 2.4 V minimum and L = 0.4 V maximum.

c. The functional tests shall be performed with $V_{CC} = 4.5$ V and $V_{CC} = 5.5$ V.

4/ All pins not being tested are to be open.

5/ Tested only after any design changes that affect that parameter. Guaranteed to the limits specified in Table I.

6/ Tested by application of specified timing signals and conditions, including:

a. Output load: 1 TTL gate and C1 = 100 pF (minimum) or equivalent circuit (see Figure 7.)

b. Input rise and fall times ≤ 10 ns.

c. Input pulse levels: 0.4 V and 2.4 V.

d. Timing measurements reference levels:

(1) Inputs: 1 V and 2 V.

(3) Outputs: 0.8 V and 2 V.

7/ Timing diagrams appear on Figure 6 as applicable. Subgroups 9, 10 and 11 shall be performed with V_{CC} = 4.5 V and V_{CC} = 5.5 V.

8/ These tests in Subgroups 9, 10 and 11 are the byte write cycle limits. These parameters shall be verified during functional testing, Subgroups 7 and 8 by application of the timing limits in Table I. Timing diagrams appear in Figure 6 (as applicable). Subgroups 7, 8, 9, 10 and 11 shall be performed with V_{CC} = 4.5 V and V_{CC} = 5.5 V. WE and CE both must be active to initiate a write cycle; therefore, the sequence of WE or CE (e.g., for WE or CE controlled write) is verified interchangeable without duplicate testing.

9/ These tests in Subgroups 9, 10 and 11 are the page mode write cycle limits. These parameters shall be verified during functional testing, Subgroups 7 and 8, by application of the timing limits and signal levels in Table I. Timing diagrams appear in Figure 6 (as applicable). Subgroups 7, 8, 9, 10 and 11 shall be performed with V_{CC} = 4.5 V and V_{CC} = 5.5 V.

10/ These tests in Subgroups 9, 10 and 11 are the chip erase cycle limits. These parameters shall be verified during functional testing, Subgroups 7 and 8, by application of the timing limits and signal levels in Table I. Timing diagrams appear in Figure 6 (as applicable). Subgroups 7, 8, 9, 10 and 11 shall be performed with V_{CC} = 4.5 V and V_{CC} = 5.5 V.

11/ During a page write operation, the cycle time defined by t_{WLWH} and t_{WHWL2} shall not be less than 1 µs.

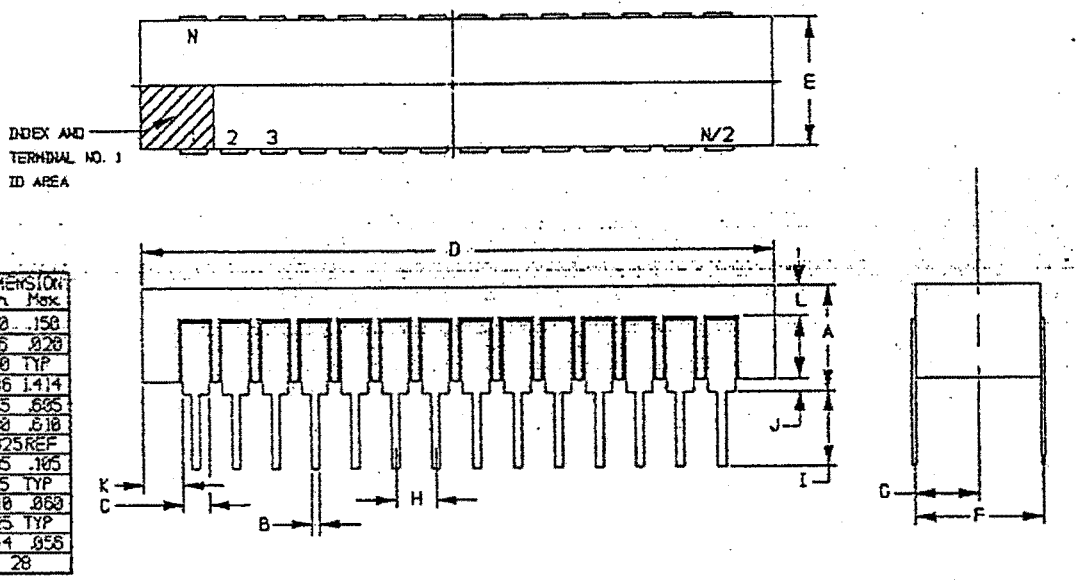
TABLE II. Burn-in and electrical test requirements.

Line no.	Applicable tests and MIL-STD-883 test method	Class S device	
		Reference paragraph 1/2/3/	Table I Subgroups
1	Interim electrical parameters (Method 5004)		1, 7, 9
2	Static burn-in I		1, 7, 9
3	Same as line 1		
4	Static burn-in II		1, 7, 9
5	Same as line 1		
6	Dynamic burn-in (method 1015)	4.2.a 4.6.2	Required
7	Final electrical parameters (method 5004)		1, 2, 3, 7, 8, 9, 10, 11
8	Group A test requirements (Method 5005)	4.3.1	1, 2, 3, 7, 8, 9, 10, 11
9	Group B test requirements (Method 5005)	4.3.2	1, 2, 3, 7, 8, 9, 10, 11
10	Group C test requirements (Method 5005)	4.3.3	Not applicable
11	Group D test requirements (Method 5005)	4.3.4	1, 2, 3, 7, 8, 9, 10, 11

1/ For all electrical tests, the device shall be programmed to the data pattern specified.

2/ Any or all subgroups at the same temperature may be combined when using a multifunction tester.

3/ Subgroups 7 and 8 shall consist of writing and reading the data patterns specified in accordance with the limits of Table I, Subgroups 9, 10 and 11.



SYMBOL	DIMENSIONS Min	Max
A	.130	.150
B	.015	.020
C	.050	TYP
D	1.386	1.414
E	.585	.595
F	.590	.610
G	.3025	REF
H	.095	.105
I	.175	TYP
J	.040	.060
K	.025	TYP
L	.044	.056
N	28	

NOTES ALL DIMENSIONS ARE IN INCHES

FIGURE 1. Case outline.

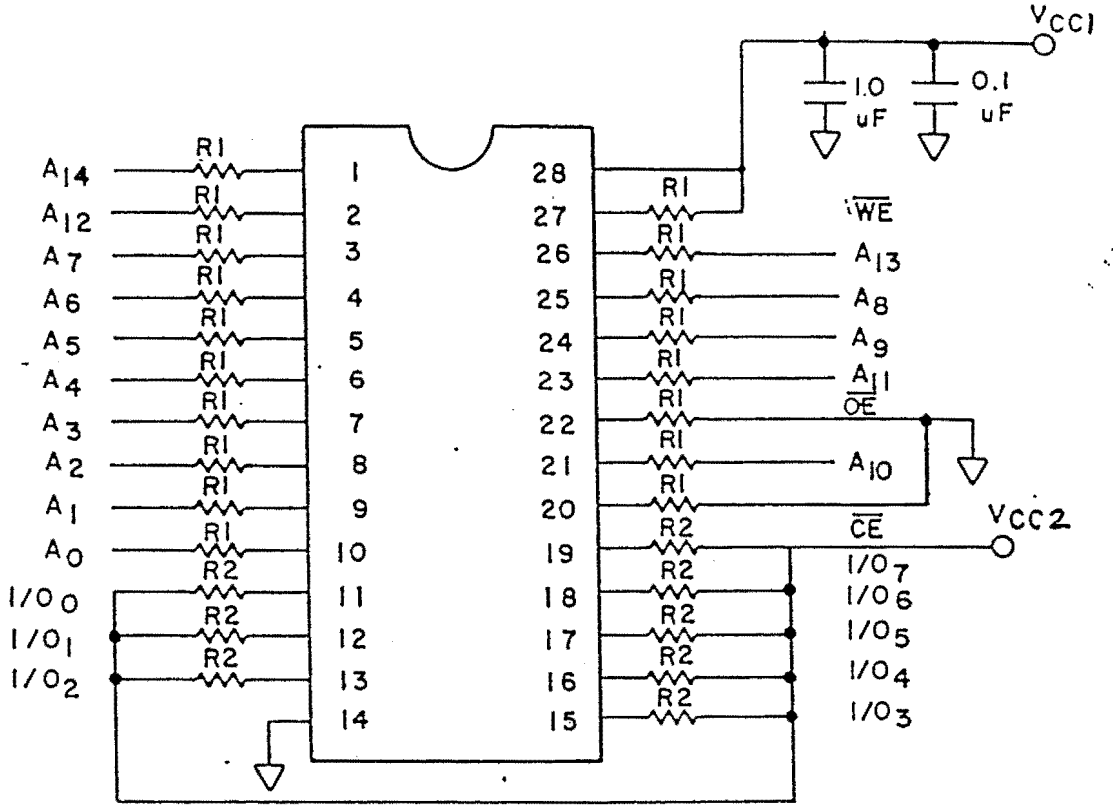
Terminal Number	Terminal Symbol
1	A_{14}
2	A_{12}
3	A_7
4	A_6
5	A_5
6	A_4
7	A_3
8	A_2
9	A_1
10	A_0
11	I/O_0
12	I/O_1
13	I/O_2
14	GND
15	I/O_3
16	I/O_4
17	I/O_5
18	I/O_6
19	I/O_7
20	$\overline{CE}$
21	A_{10}
22	$\overline{OE}$
23	A_{11}
24	A_9
25	A_8
26	A_{13}
27	$\overline{WE}$
28	V_{CC}

FIGURE 2. Terminal connections.

Mode	CE	OE	WE	I/O
Read	V_{IL}	V_{IL}	V_{IH}	Dout
Standby	V_{IH}	X	X	High Z
Chip clear	V_{IL}	V_H	V_{IL}	$D_{IN} = V_{IN}$
Byte write	V_{IL}	V_{IH}	V_{IL}	D_{IN}
Write inhibit	X	V_{IL}	X	High Z/D_{OUT}
Write inhibit	X	X	V_{IH}	High Z/D_{OUT}

Table definitions:
V_{IH} = High logic level
V_{IL} = Low logic level
V_H = Chip clear voltage (15)
X = Do not care
High Z = High impedance state
D_{IN} = Data input
D_{OUT} = Data output

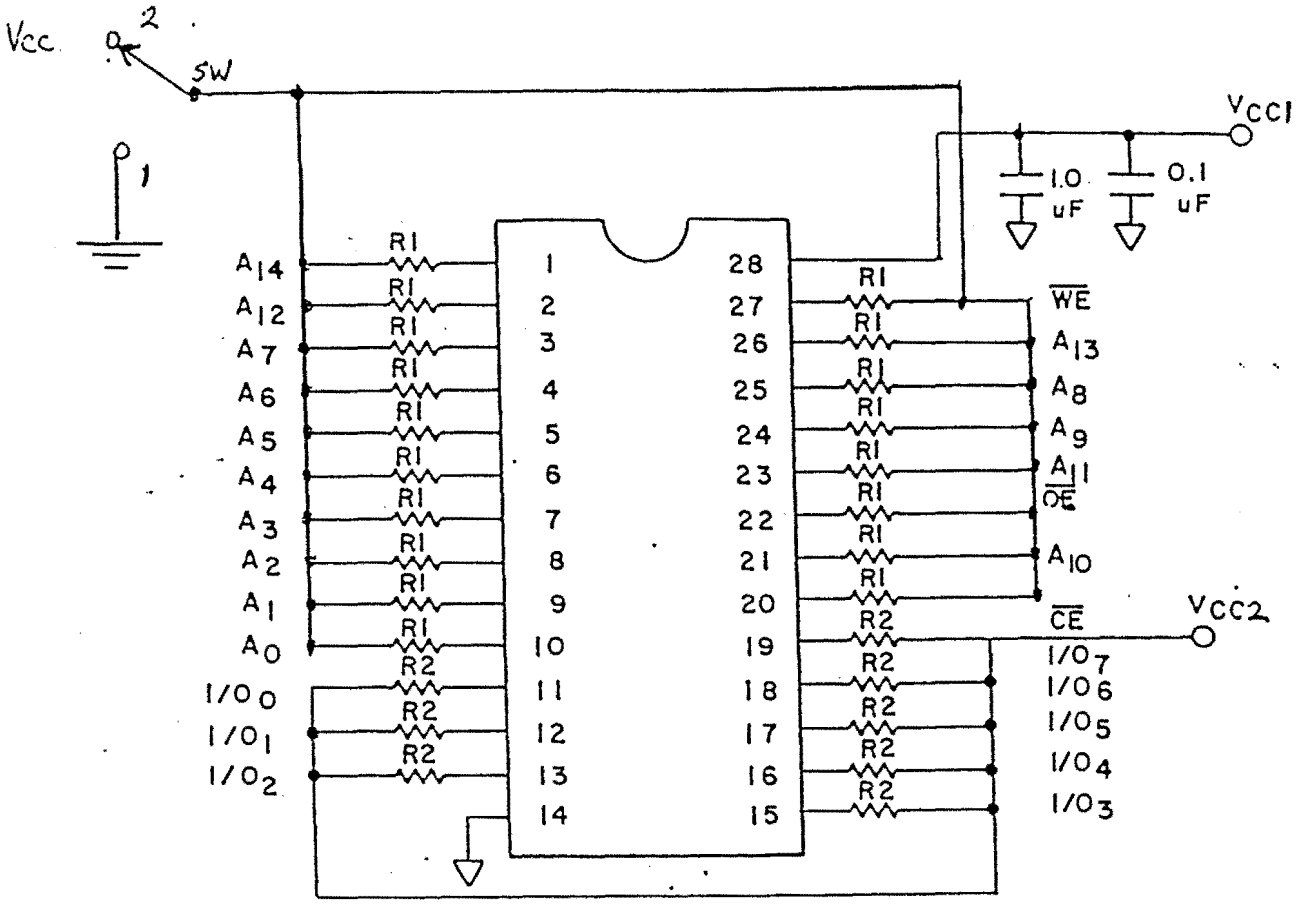
Figure 3. Truth table for unprogrammed devices.



NOTES:

1. All resistors labeled R1 are 3.3 kΩ, .25 W, 5% metal film, at every socket.
2. All resistors labeled R2 are 2.2 kΩ, .25 W, 5% metal film, at every socket.
3. There is a 1.0 µF decoupling capacitor between pin 28 and GND at every socket.
4. There is a 0.1 µF decoupling capacitor between V_{CC} and GND at every socket.
5. V_{CC1} = 5.25 V, V_{CC2} = 2.25 V. All voltage levels are ±0.25 V.
6. Power up sequence: V_{CC1}, V_{CC2}, addresses,
7. Power down sequence: addresses, V_{CC2}, V_{CC1}.
8. F_0 (A_0) = 125 kHz (minimum).
9. F_1 (A_1) = F_0 divided by 2, F_2 = F_1 divided by 2 ... F_{12} (A_{12}) = F_{11} divided by 2.

FIGURE 4. Burn-in and operating life test circuit.



Notes:

1. All resistors labeled R1 are 3.3k ohm, .25W, 5% metal film, at every socket.
2. All resistors labeled R2 are 2.2k ohm, .25W, 5% metal film, at every socket.
3. There is a 1.0 uf decoupling capacitor between pin 28 and GND at every socket.
4. There is a 1.0 uf decoupling capacitor between VCC and GND at every socket.
5. VCC1 = 5.25V, VCC2 = 2.25V. All voltage levels are +/- 0.25V.
6. Static I SW = position 1.
7. Static II SW = position 2.

Figure 4A. Static Burnin Test Circuit

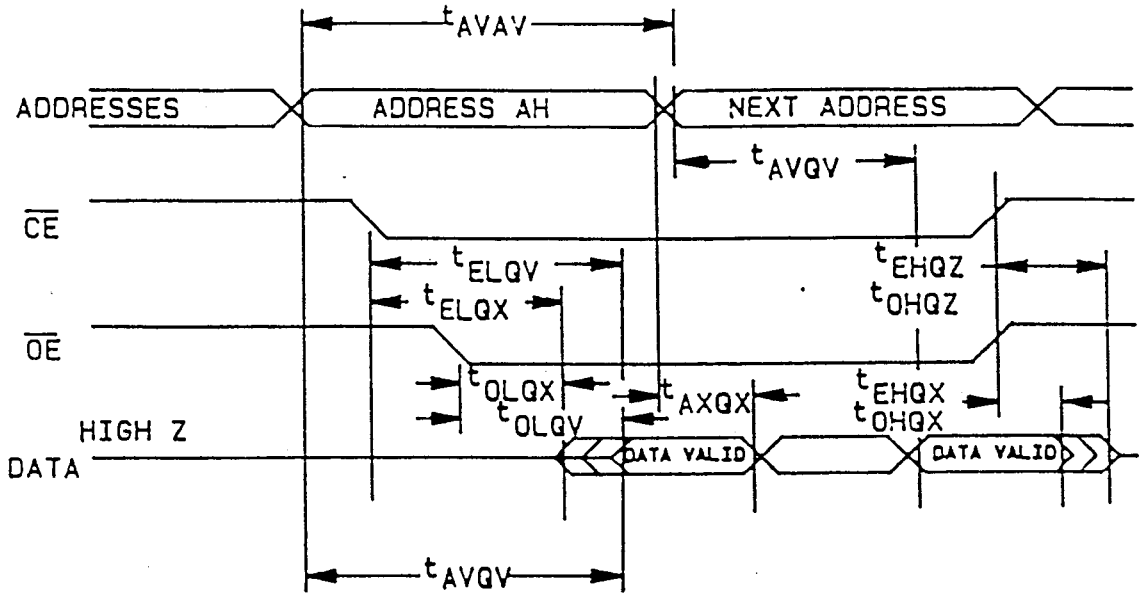
Column address (see notes)

		0	1	2	3	4	5	6 . . . 57	58	59	60	61	62	63
	0	AA	AA	AA	AA	AA	AA	AA . . . AA	AA	AA	AA	AA	AA	AA
	1	55	55	55	55	55	55	55 . . . 55	55	55	55	55	55	55
	2	AA	AA	AA	AA	AA	AA	AA . . . AA	AA	AA	AA	AA	AA	AA
	3	55	55	55	55	55	55	55 . . . 55	55	55	55	55	55	55
R	.							. . .						
O	.							. . .						
W	.							. . .						
	124	AA	AA	AA	AA	AA	AA	AA . . . AA	AA	AA	AA	AA	AA	AA
A	125	55	55	55	55	55	55	55 . . . 55	55	55	55	55	55	55
D	126	AA	AA	AA	AA	AA	AA	AA . . . AA	AA	AA	AA	AA	AA	AA
D	127	55	55	55	55	55	55	55 . . . 55	55	55	55	55	55	55
R	.							. . .						
E	.							. . .						
S	.							. . .						
S	508	AA	AA	AA	AA	AA	AA	AA . . . AA	AA	AA	AA	AA	AA	AA
	509	55	55	55	55	55	55	55 . . . 55	55	55	55	55	55	55
See note 1														
	510	AA	AA	AA	AA	AA	AA	AA . . . AA	AA	AA	AA	AA	AA	AA
See note 2														
	511	55	55	55	55	55	55	55 . . . 55	55	55	55	55	55	55

NOTES:
1. All address numbers shown in decimal.
2. Each column/row address location corresponds to one byte.
3. All data numbers shown in hexadecimal.
   AA = 10101010 55 = 01010101
4. Manufacturers at their option may employ an equivalent pattern provided it is a topologically true alternating bit pattern.

FIGURE 5. Data pattern.

Read mode

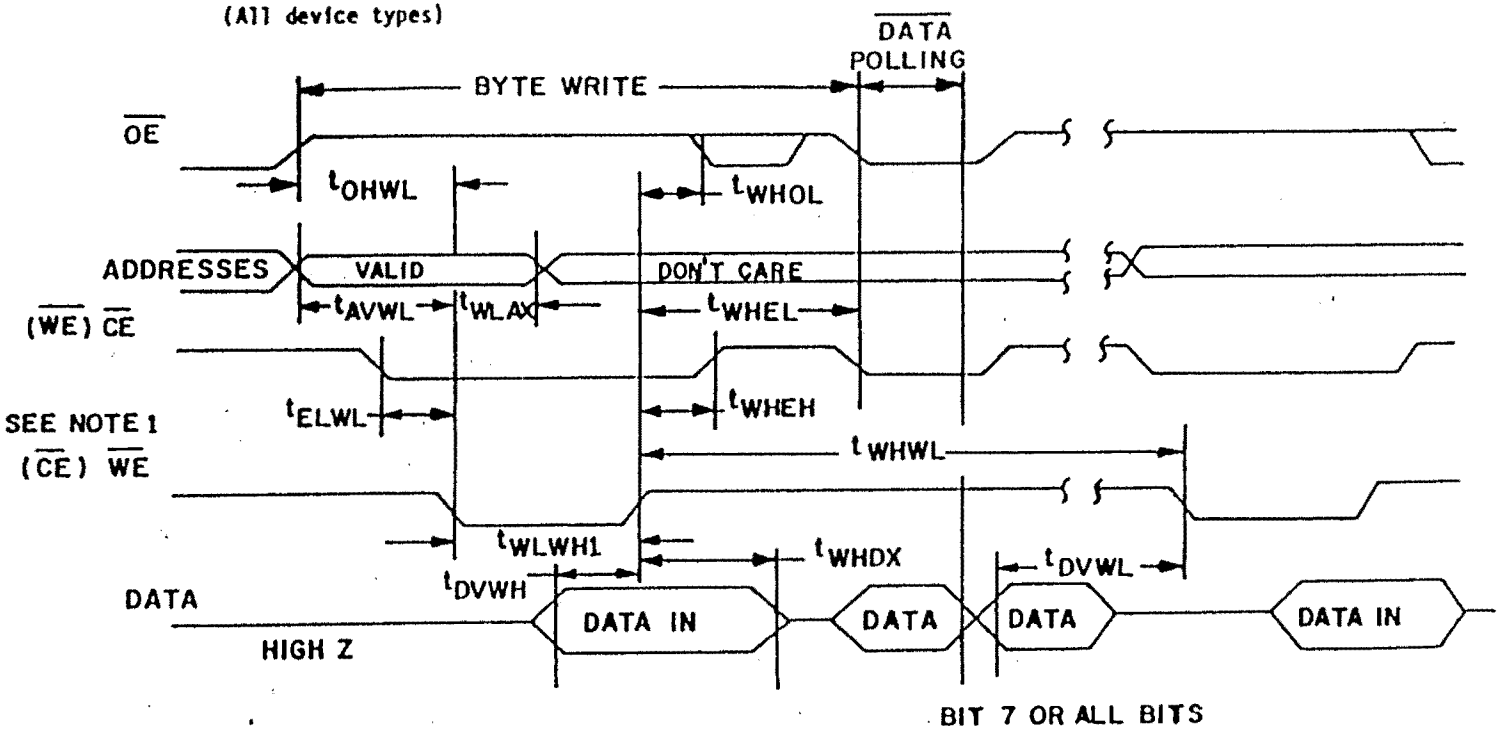


NOTES:
1. V_{CC} shall be applied simultaneously or after $\overline{WE}$ and removed simultaneously or before $\overline{WE}$.
2. Output load is a TTL gate and 100 pF including jig or probe capacitance.
3. Input rise and fall time $\leq$ 20 ns.
4. Input pulse levels of 0.4 V and 2.4 V.
5. Timing measurement reference levels:
   Inputs 1.0 V and 2.0 V.
   Outputs 0.8 V and 2.0 V.

FIGURE 6. Waveforms.

Byte write waveforms ($\overline{WE}$ and $\overline{CE}$ controlled)

(All device types)

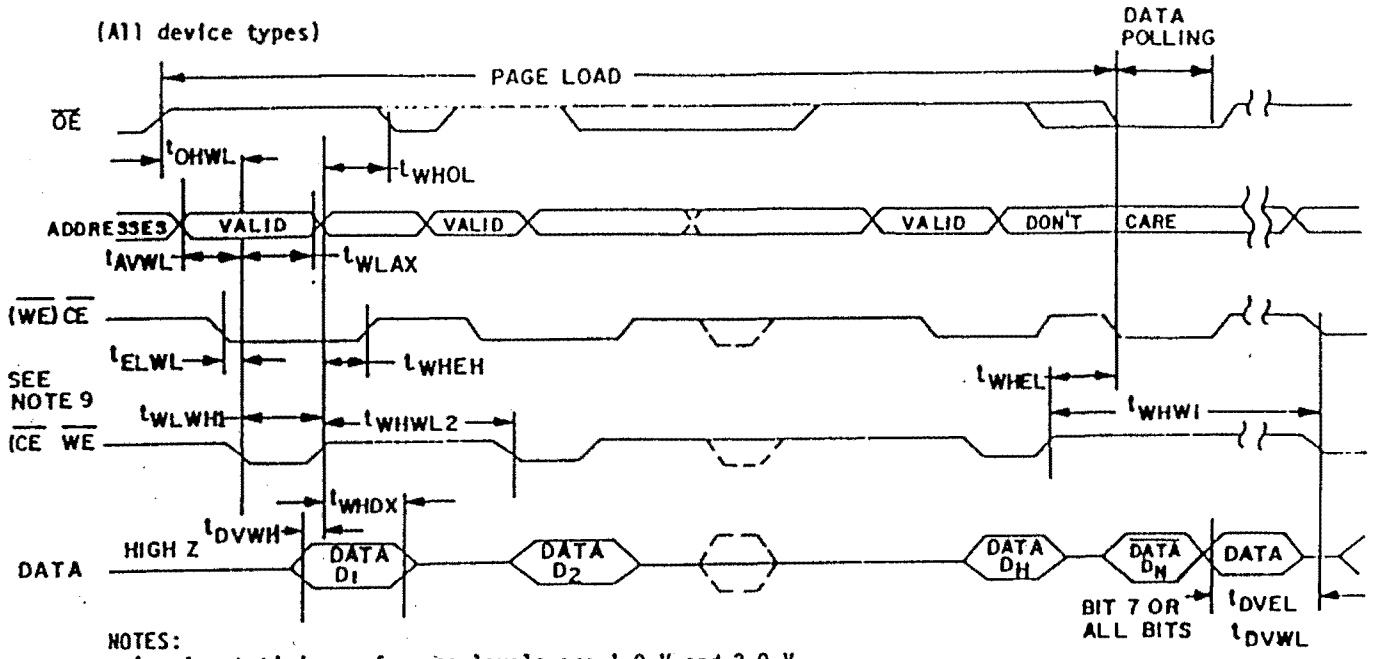


NOTES:

1. Input timing reference levels are 1.0 V and 2.0 V.
2. Output timing reference levels are 0.8 V and 2.0 V.
3. Input pulse rise and fall times (10% and 90%) $\leq$ 20 ns.
4. Input pulse levels of 0.4 V and 2.4 V.
5. Program verify equivalent to the read mode.
6. $\overline{WE}$ is noise protected. Less than a 20 ns write pulse will not activate a write cycle.
7. $\overline{WE}$ and $\overline{CE}$ both must be active to initiate a write cycle; therefore, the sequence of $\overline{WE}$ or $\overline{CE}$ (e.g., for $\overline{WE}$ or $\overline{CE}$ controlled write) is verified interchangeable without duplicate testing.

FIGURE 6. Waveforms - Continued.

Page mode write cycle waveforms



NOTES:

1. Input timing reference levels are 1.0 V and 2.0 V.
2. Output timing reference levels are 0.8 V and 2.0 V.
3. Input pulse rise and fall times (10% and 90%) $\leq$ 20 ns.
4. Input pulse levels are 0.4 V and 2.4 V.
5. Program verify equivalent to the read mode.
6. Page load is 1 to 64 bytes of data.
7. $\overline{WE}$ is noise protected. Less than a 20 ns write pulse will not activate a write cycle.
8. $\overline{WE}$ and $\overline{CE}$ both must be active to initiate a write cycle; therefore, the sequence of $\overline{WE}$ or $\overline{CE}$ (e.g., for $\overline{WE}$ or $\overline{CE}$ controlled write) is verified interchangeable without duplicate testing.
9. Page write cycle timings are referenced to the $\overline{WE}$ or $\overline{CE}$ inputs, whichever is last to go low, and $\overline{WE}$ or $\overline{CE}$ inputs, whichever is first to go high.
10. Bytes may be loaded and reloaded at random within a page load cycle. The page addresses must remain the same for each successive write operation throughout the page load cycle. Between successive byte writes within a page write operation, $\overline{OE}$ can be strobed low; e.g., this can be done for the next write; or with $\overline{WE}$ high and $\overline{CE}$ low effectively performing a polling operation.

FIGURE 6. Waveforms - Continued.

Chip erase mode waveforms

(All device types)

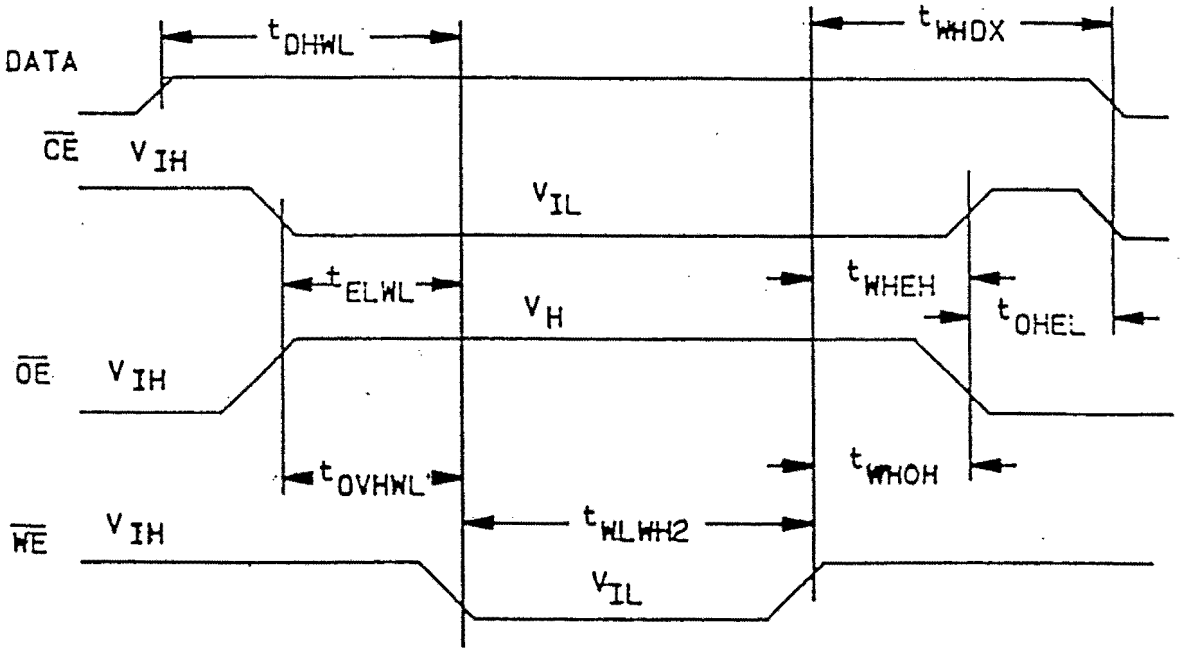
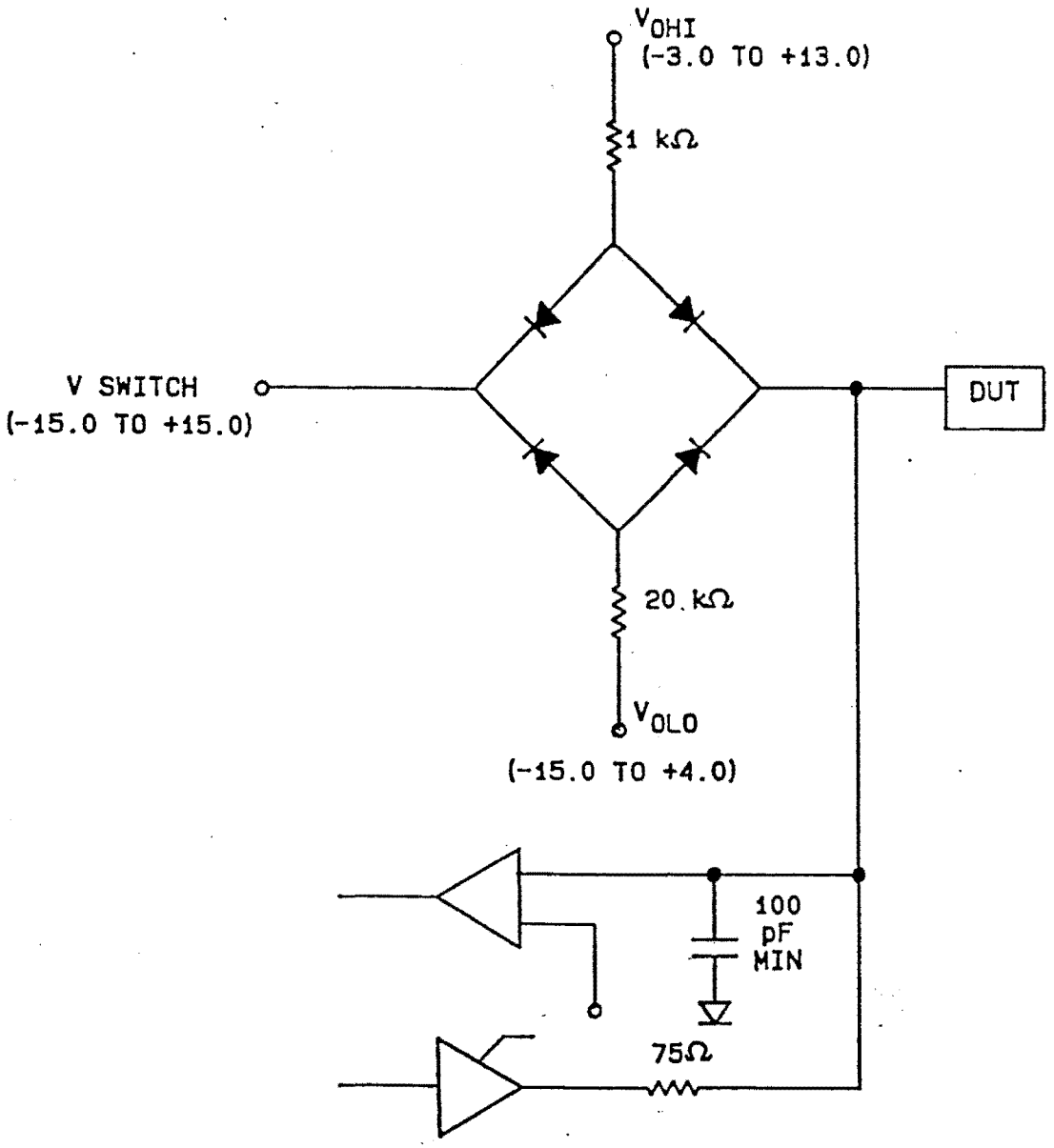


FIGURE 6. Waveforms - Continued.



NOTE: V_{OHI} and V_{OLO} will be adjusted to meet load conditions of table I.

FIGURE 7. Switching load circuit.