A Look at Failure: Weld Splatter
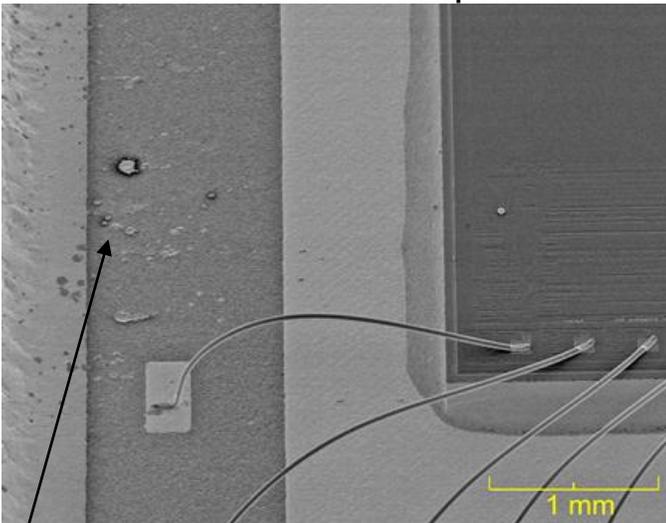
Faulty lid welding process leaves conductive splatter causing PIND test failure. JPL Failure Analysis Lab

Dynamic Burn-In Frequency

Some manufacturers of high-frequency parts are conducting burn-in testing at frequencies much lower than the maximum specified frequency of the part (several hundred MHz for memories and up to low GHz for data converters). MIL-STD-883 does not specify frequency requirements for dynamic burn-in. The burn-in equipment is typically limited to 4 MHz. This issue has been raised at the JEDEC Task Group on burn-in and delta requirements.

For further information, contact:

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Supply Chain—The Changing Landscape

When auditing your suppliers, should you be auditing your suppliers' suppliers? Your purchase order to Chip Manufacturer A provides a part that may have required careful handling from all the companies in the fictitious but typical list below:

- *Die design and fab:* Chip Manufacturer **A**
- *Package design and package manufacturing*: High Tech Part Packager **B**
- *Wafer lap and dice*: Dice Mfg. Inc. **C**
- *Assembly*: Test Lab Co. **D**
- *Column grid array (CGA) Column Attach and solder-ability*: Array Ltd. **E**
- *Screening/electrical/package tests*: Test Lab Co. **F**
- *Complete electricals per SMD*: Volts Engineering **G**
- *Internal water vapor content testing*: Moisture Inc. **H**
- *Radiation Testing*: Protons-R-Us **I**

DLA approves all entities in the supply chain for QML product.

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EEE COTS Parts and Small Spacecraft

The interest in small spacecraft (<100 kg) has continued to grow each year. Reduced launch costs are a key contributor to this increasing trend in small satellite usage. EEE commercial off-the-shelf (COTS) parts play a significant role in the ability to reduce project cost while enabling ever increasing levels of capability. Large field-programmable gate arrays (FPGAs), high density memories, and continuously improving radio frequency (RF) communication parts form the basis for communication and data analysis space platforms. Modern electronic parts continue to benefit from industry continuous improvement practices. Large wafer fabs are capable of producing defect levels in the low parts per million (ppm), and manufacturers have instituted sophisticated Design for Reliability (DfR) and Design for Testability (DfT) methods.

One of the most important possible failure mechanisms due to the use of more EEE COTS is soft errors. While historical space grade parts have always been concerned with single-event effects (SEEs), as well as total dose effects, due to the inherent radiation environment in space, commercial device users have also been concerned with soft errors. Commercial soft errors can be related to interactions with either alpha particles or neutrons. Almost all large digital integrated circuits (ICs) have significant amounts of on-board static RAM (SRAM) while requiring external dynamic RAM

(DRAM) for operation. Current transistor densities are now in the hundreds of millions of individual gates per square centimeter. These large areas of memory make ideal targets for soft error or single event upsets (SEUs). These types of errors must be managed in order to properly use EEE COTS parts in small spacecraft.

Soft error rates are usually measured in terms of hundreds of failures in time per megabyte (FIT/MB). With error rates this high, integrating even a few modern COTS chips into a design could result in small spacecraft experiencing multiple errors even for a mission duration that is only a few months long. This rate is 10 to 100X higher than historical "hard" device failures such as electromigration and hot carrier effects. While circuit designers work at the logic and layout level to minimize such effects, the end user must implement a variety of system-level mitigation schemes in order to manage and control errors. Such schemes include redundant devices operating in lock step, triple-modular architectures, and a wide variety of error-correction and detection software. All of these add significantly to power, size, and mass requirements and can possibly radically alter the overall system design. Failure to implement adequate soft-error and SEU protection will often lead to failures that are hard to diagnose and difficult to debug. Many times these failures start out as a pure software failure (such as failure to load a new version or update). Only after significant and usually expensive testing can a root cause be precisely determined to be soft error on a given logic node.

The performance benefits of modern EEE COTS for use on small spacecraft needs to be augmented with concern over soft errors.

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Current and Emerging DRAM SEEs

Dynamic Random Access Memories (DRAMs) have been used on NASA spacecraft since Cassini. They present very attractive density and power attributes. Modern spacecraft have employed more recent Synchronous DRAMs (SDRAMs), and cutting edge designs are now calling for the use of double data rate devices (DDR, DDR2, and DDR3). These devices can transfer data at rates above 1 Gb/s per data line, which is not readily available in hardened components. DRAMs are built from a cell array of storage capacitors that must be periodically refreshed. Early DRAMs combined the cell array with an address decoder for accessing bits. SDRAMs increased the complexity by adding multiple banks, support for yield-improving redundancy, and standard operations such as automatic refresh. DDR devices increase this support even more. With each generation, increased on-chip requirements and functionality have increased the complexity of single-event effects (SEEs).
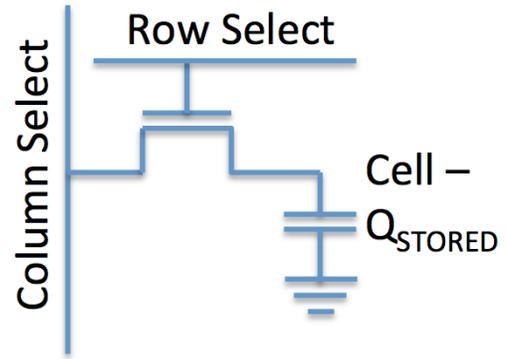

Figure 1: DRAM Data Bit Storage Cell

Early DRAMs showed sensitivity to ionizing particles by exhibiting bit upsets and row upsets (where many data bits sharing the same device row may be flipped). The bit upsets are referred to as single bit upsets (SBUs) when only one bit of a read operation is flipped, or as multiple bit upset (MBU) when more than one is flipped. Sometimes multiple bits are flipped by a single ionizing particle, but the multiple bits are spread over multiple addresses. From an operational point of view these are treated as multiple SBUs. In early devices SBUs and MBUs dominated (with the latter being more common in devices with a wide data word); row upsets were far less likely. Current SDRAMs in flight are showing more complex SEE modes that disrupt larger amounts of data. These SEE modes are often referred to as single event functionality interrupts (SEFIs). They are a byproduct of the increased complexity of the SDRAMs. Some current flight projects are experiencing these events at a rate of approximately one every two months. Although they may be less common than bit upsets, their system impact is often much greater. SEFIs occur when SEEs affect the control circuitry for the device. Next-generation systems using DDR2 or newer devices will likely have their SEE response dominated by SEFIs due to the increased complexity of the support circuitry in DDR2 devices. This increased SEFI rate will require aggressive error handling.
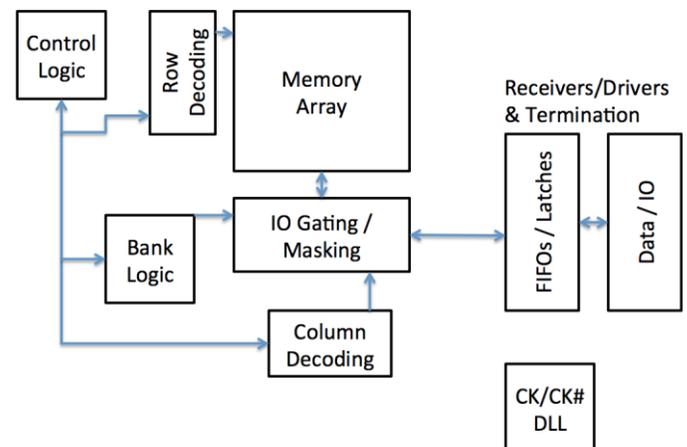

Figure 2: Block diagram of a DDR2 memory.

The impact of SEE depends on the system implementation. Error detection and correction (EDAC) systems are often used to correct SBUs before they impact a flight system, achieving very low per-bit SEE rates until they are affected by a SEFI. EDAC systems use additional bits, which encode enough information to identify an incorrect bit or determine that two bits have changed. EDAC systems with this capability are called single error correction double error detection (SECDED). SECDED requires seven check bits for a 32-bit data word, or eight check bits for a 64-bit data word. With correct implementation, these EDAC systems were sufficient for DRAM use. Recent SEFI sensitivity of SDRAMs has highlighted two scenarios where SECDED EDAC is insufficient. SEFIs in SDRAMs have occurred where thousands of addresses exhibit one or two bit errors, and they have occurred where thousands of addresses exhibit between one and four bit errors. In the former case, the number of errors encountered at any one time by the EDAC system is two or less, so the errors are contained. While in the latter case, bit counts above two have undefined EDAC response. In both cases, however, the number of errors is very large, and the data in the portion of the device with the SEFI is essentially lost. In both cases double bit errors are likely to be seen, leading to system-level response to an uncorrectable EDAC word.
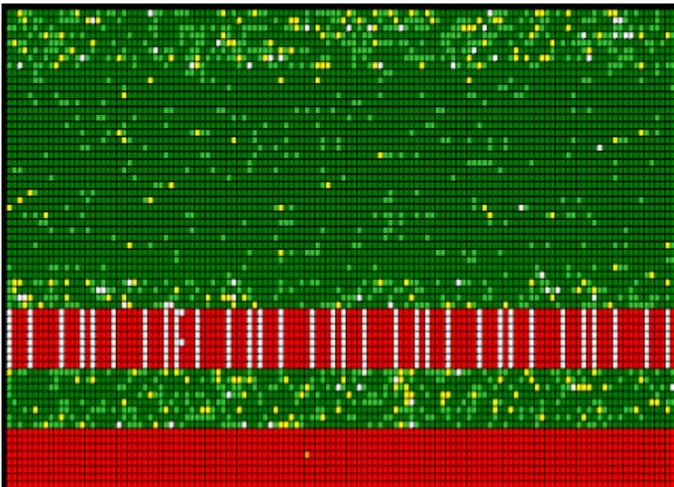

Figure 3: Example of an SDRAM bank with two SEFIs. Red dots are rows with a multi-block error (MBE) of 3 or more bits. Other colors refer to different counts of SBUs in a row.

It has been observed that many SEFIs can be mitigated by periodically reloading the mode registers of the SDRAM. Reloading the mode registers in an SDRAM acts as a soft reset. This action is recommended in DDR and later devices; however, a full reset requires resynchronizing the delay-locked loop (DLL) in addition to reloading the mode registers. The SEE response of these devices is currently being studied by several aerospace organizations, and further recommendations related to the mode register reload and DLL resynchronization are anticipated.

System-level error handling and complexity in recent devices have highlighted the need to handle the more intrusive SEFIs in a robust way. Although periodic reload of mode registers and resetting of DLLs is recommended, it cannot fully protect data. Recent data collected from one example device indicates that reloading the mode register may only result in a reduction of the SEFI rate by about a factor of ten. The only viable approach to guarantee that data is not lost is to use enough redundancy that the EDAC system can recover data in the event that an entire device worth of data is lost. There are multiple hardware schemes that can be employed, from triple-module redundancy to complex Hamming codes. In the absence of such an EDAC system, careful study of SEFI signatures and their impact on device data can be used to understand the frequency and structure of data loss events.

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Class Y Update

Class Y is about the infusion of new technology into the military and space standardization system. This new class will cover products such as Xilinx Virtex-4 / Virtex-5 and similar devices. The most recent G12 Class Y meeting was held on October 1, 2012. DLA Land and Maritime has completed their Engineering Practice (EP) study, and will update the document for distribution to the community for review.

For more information, contact

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GIDEP Alerts/Advisories

Contact your GIDEP Representative for a copy of:

Suspect Coun-terfeit	Exceeds 20. Contact GIDEP Rep.
Misc.	IB7-P-12-02A Aluminum Whisker Growth; CE9-P-12-01 Microcircuit, Digi-tal-Linear, 14 bit, 2.4 GSPS D/A Con-verter; BP6-P-12-01 Microcircuit, 3 Pad LCC Package; 6L-P-12-01 Failure traced to shorted Zener Diode; MT2-P-12-02 Microcircuit, Hybrid, DC/DC con-verter, EMI Filter; GB4-P-12-01A Micro-circuit, Memory, Digital, CMOS, Rad Hardened Low Voltage; PA3-P-12-01 Hermeticity Issue with TO-257 Metal Headers with Glass Feed Through Seals; IB7-A-12-01 Transistor, Ni Flakes in TO-18 Packages; AYE-P-12-01 Attenuator, fixed, MIL-DTL-M3933; VV-A-12-03 Connector, Electrical, Class W; UR7-P-12-01 Microcircuits, Seam Weld, Foreign Object Debris; SC7-P-12-03A Synplify Software Bug Affecting RTAX-S/SL/DSP and Axcelerator De-signs with Active Low Enable Flip Flops

NASA parts specialists recently supported DLA Land and Maritime Audits of:

ST Microelectronics, Singapore; Golden Altos, CA; Ava-go Technologies, Singapore; Triotech, Singapore; Linear Technology, WA; Honeywell Aerospace, MN; Millennium MicroTech, Thailand; Optek Technology, TX; Sawtec, TX; Micropac Industries, TX; International Rectifier, MA; Wafer Tech, WA; Spectrum Microwave, MA; Minco Technology Labs, TX; M.S. Kennedy, NY; Microsemi Corp., Ireland; Aeroflex Metelics, MA; Aeroflex, NH; e2v Aerospace & Defense, France; Infineon, Germany; Viasystems Corp., CA; Kyocera America, CA; Solitron Devices, FL; Spectrum Controls, PA; Semicoa Corp., CA; M.S. Kennedy Corp.,NY, Intersil Corp., FL; Micro-semi Lawrence, MA; Crane Electronics, WA; Cirexx In-ternational, CA; Q-Tech Corp., CA

Upcoming Meetings

- JEDEC JC-13, San Antonio, TX, Jan. 14–17, 2013 http://www.jedec.org/events-meetings/view_event/481

- European Space Components Conference (ESCCON 2013) at Noordwijk, The Netherlands, March 12–14, 2013 ESCCON 2013

- Second Annual Space Tech Conference Long Beach, CA, May 21-23, 2013 www.spacetechexpo.com

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http://atpo.jpl.nasa.gov/nepag/index.html

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