Effect of Radiation Exposure on the Retention of Commercial NAND Flash Memory

T.R. Oldham[1], D. Chen[2], M. Friendlich[3], M.A. Carts[2], C.M. Seidleck[3], and K.A. LaBel[2]

***Abstract*— We have compared the data retention of irradiated commercial NAND flash memories with that of unirradiated controls. Under some circumstances, radiation exposure has a significant effect on the retention of flash memories.**

I. Introduction

Flash memories are used in different applications in space systems, and our goal was to determine the retention characteristics of flash memories for relevant applications. Retention is defined as the ability to hold information for a specified period, without being refreshed or changed. For terrestrial applications, manufacturers normally specify ten years as the period for retention. In space, one would hope for retention for the entire mission lifetime. The question is whether or not radiation exposure will affect retention during the mission life. Relevant applications include storage of critical program codes, which is rarely, or never, written or rewritten. Mass data storage, on the other hand, may be rewritten frequently, and needs to retain information only until it is downloaded to the ground, or new data is written. Previously, we compared the endurance reliability of irradiated and unirradiated NAND flash memories, and found no significant difference [1]. An endurance failure would have required enough radiation-induced defects in the tunnel oxide to induce a significant shift in V_T. However, the unhardened commercial parts used as test samples could be irradiated only to modest doses before they failed for other reasons [2, 3]. It turned out that there would not have been enough radiation-induced defects to cause an endurance failure, until after radiation had caused other failures. There was a concern, however, that retention might be more sensitive to radiation, since a retention failure requires only a very low current leakage path. Such a leakage path requires a very small number of radiation-induced defects, if they are properly aligned. Therefore, we have compared the retention failure rates for irradiated and unirradiated samples, using two different methods to accelerate the aging of the samples. Under certain circumstances, radiation exposure can cause a significant increase in the rate of retention failures in flash memories. We note, however, that flash manufacturers typically specify the endurance and retention characteristics of their products, assuming that error correction software will be used. However, in this test, we did not use error correction, in order to to characterize the underlying technology, and not the effectiveness of the error correction. It is likely that, if we had used error correction, the parts may still have met all their reliability specifications.

II. Description of Samples

The samples used in this study are summarized in Table I. All devices employ single level cells (SLC). In Table I, the TID (total ionizing dose) failure level was determined previously, by testing to failure [4-6]. The given TID exposure level refers to this experiment, and is less than the failure level. Each device type uses a nominal 3.3 V power supply (2.7-3.6 V, full range). The Samsung parts are intended to operate over the industrial temperature range, -40 to +85º C, while the Micron parts are intended for the commercial temperature range, 0-70°C. Both the write (Programming) and Erase operations proceed through Fowler-Nordheim tunneling of electrons through the tunnel oxide [7]. Fowler-Nordheim (F-N) injection requires very high fields, and the operation of

TABLE 1. SAMPLES USED IN TID TESTS.

Mfr.	Part (NAND flash)	Part Number	LDC	Feature Size (nm)	Temp. Range (°C)	TID failure (krads (SiO_2)) [4, 5, 6]	TID exposure (krads (SiO_2))
Micron	8G	MT29F8G08AAA	948	50	0-70	75	50
Micron	16G	MT29F16G08ABABA	1006	40	0-70	100	50
Samsung	8G	K9F8G08U0M	031	60	-40-85	500	200

This work was supported in part by the NASA Electronic Parts and Packaging Program (NEPP), and the Defense Threat Reduction Agency (DTRA) under IACRO# 11-4395I.

1. Dell Services Federal Government, Inc., Seabrook, MD 20706
2. NASA Goddard Space Flight Center, Greenbelt, MD 20771
3. MEI Technologies, Inc., Seabrook, MD 20706

To be presented by Timothy R. Oldham at the International Electrical and Electronics Engineering (IEEE) Nuclear and Space Radiation Effects Conference (NSREC), July 28, 2011, Las Vegas, NV., and published on nepp.nasa.gov and radhome.gsfc.nasa.gov.

a charge pump circuit to step up the power supply voltage. F-N injection also introduces damage into the tunnel oxide, contributing to wear-out. It is for this reason, that manufacturers typically guarantee flash memory only for $1x10^5$ Program/Erase (P/E) cycles. This stress-induced damage is very similar to radiation-induced damage, because it involves similar defects [8], so it is reasonable to look for combined effects.

III. Experimental Procedure

SLC NAND flash normally has a specification to retain stored information for ten years. To accelerate the aging of the parts to simulate a ten year lifetime, we have used two different methods. The first industry standard technique for accelerating retention failures is to bake the parts at high temperature, in order to investigate retention for program code storage. We used this method, baking both the Samsung 8G parts and the Micron 16G parts at 100°C, for at least 1000 hours. Characterization of the baked test devices was performed using a commercial Triad Memory Tester system [9]. For the Samsung parts, five parts were tested in each test group—that is, five parts were irradiated to 200 krads (SiO_2), and five matching controls remained unirradiated. This radiation dose was chosen because the parts survived to 400 krads (SiO_2) when tested to failure, and half that is well above most NASA requirements. The Micron 16G parts were handled similarly, except that the radiation dose was chosen to be 50 krads (SiO_2). In a test to failure, the Micron 16G parts failed at 100 krads (SiO_2), and 50 krads (SiO_2) also matched the dose to another group of Micron parts that had been subject to P/E cycling. Both groups were prepared in the same way, with a checkerboard pattern written, and initial electrical tests performed. During baking, both groups were read out periodically, and the errors counted. The second method employed simulating Mass Storage issues, was performing (P/E) cycling on five irradiated samples and five unirradiated controls of the Micron 8G NAND (see Table I) to three different cycling levels. These levels were 10^5, 10^4, and 10^0 P/E cycles. The radiation exposure was to 50 krads (SiO_2). This level was chosen because it was the highest dose where all the parts had survived in a test to failure, which occurred at 75 krads (SiO_2). The cycled parts were characterized [10]. For parts that are cycled in normal operation, this is an obvious technique, and an industry standard, for accelerating the aging process [8, 9].

TID testing was done at a Co-60 room air source, where the pencils are raised up out of the floor, during exposures. Active dosimetry was performed, using air ionization probes. Testing was done, using a standard Pb/Al filter box. The initial tests were done in accordance with MIL-STD-TM 1019.7 [11]. Parts were under DC bias during exposure. Each test group of five devices was programmed with an all zero pattern during exposures, and biased at 3.6 V.

IV. Results and Discussion

There is an extensive literature on the reliability, including retention characteristics, of flash memory (see, for example, [7] and its bibliography). Generally, the physical mechanism that causes retention failure is leakage current through the tunnel oxide [12], which is due to trap assisted tunneling (TAT) [13]. Basically, electrons from the floating gate tunnel from trap to trap until they escape the oxide. The tunneling rate is a strong function of the distance between traps, and it has been argued that even two defects, properly aligned, can cause a retention failure [13]. The electrical stress from P/E cycling, which injects charge through the tunnel oxide at high field, causes oxide damage in the form of hole traps, and gives rise to SILC (stress-induced leakage current. Since the effect of TID exposure is also to introduce trapped holes into the oxide, one might expect radiation induced trapped holes to contribute to TAT-induced retention failures. It has been shown [14-16] that that electrons tunneling into and out of E' centers, which are just trapped holes, is an important component in the time-dependent response of MOS oxides. There is also no question that high enough radiation doses will produce measurable leakage currents in thin MOS oxides [8], even without electrical stress. In [8], Scarpa et al. reported measurable radiation-induced leakage currents (RILC), but at multi-Mrad (SiO_2) doses. In fact, Scarpa et al. also concluded that RILC and SILC originate in the same physical mechanism. At such high doses, unhardened commercial technology would be likely to fail from TID damage long before RILC could be measured. On the other hand, retention failures can be caused by leakage currents too small to measure directly.

James [17] reverse engineered flash products from several manufacturers, and reported that the Samsung 4G single level cell (SLC) memory cell was 73 nm by 90 nm, with a tunnel oxide thickness of 7.2 nm. If we assume a ΔV_T of 1V is required to produce a retention failure, which is typical, then, for this geometry, the loss of 194 electrons will cause a failure. For the typical ten year retention spec, this means leakage current has to be less than one electron every 19 days, or less than 10^{-25} A, on average. For newer chips, scaled more aggressively, the tolerable leakage current would be even less. Therefore, the question is not whether or not radiation can cause flash retention failures. The question is what dose level is required for such failures to occur. And will unhardened commercial parts suffer TID failures for other reasons before that dose is reached?

As we have described, there are two methods used to accelerate retention failures in flash memory, which are to bake the circuit at elevated temperature, or to expose the circuit to repeated P/E cycles [8, 9]. Here, we have used both methods, as have many others, some of whom treat the two methods as interchangeable. In fact, Belgal et al. [18] present a model which allows one to calculate how many P/E cycles are equivalent to a given change in the bake temperature. This model is given with supporting experimental data, but only for

the authors' company's process (Intel), and the general applicability is uncertain. It is not entirely clear what the mechanism is by which a high temperature bake accelerates charge loss from the floating gate. One possibility, suggested by Herrmann et al., [19] is a multi-phonon assisted tunneling process, by which electrons in the floating gate tunnel to oxide traps.

The aging acceleration factor (AF) that one gains by baking at 100°C, rather than 25°C, is not entirely clear. Normally, AF(T) is calculated as follows:

$$AF(T) = \exp[(E_A/k_B)\ \{(1/T_{use}) - (1/T_{stress})\}] \quad (1)$$

where E_A is the activation energy, k_B is the Boltzman constant, T_{stress} is the bake temperature, 100°C, and Tuse is taken to be room temperature. The problem here is that published values of E_A vary widely, from 0.3 eV to 1.9 eV, and that E_A appears to be temperature dependent [20]. Generally, the higher values of E_A correspond to higher temperatures than we used here. If we use Eq. 1 with E_A = 0.3 eV, then AF = 8.7, and 1000 hours at the stress temperature corresponds to about one year at room temperature. If E_A = 0.5 eV is assumed, AF = 36.8, and 1000 hours test time corresponds to about 4.2 years. If E_A = 0.7 eV is assumed, AF = 155, and 1000 hours corresponds to 17.8 years. It is not clear what the proper value of E_A is, but relatively low values are usually assumed in the literature [15, 17] for our temperature range. Therefore, 1000 hours of test time may not be enough to predict a full ten year life test. This means the error count could be higher when we do reach the test time equivalent to a ten year lifetime.

In Fig. 1, we show the results for the Samsung parts, baked at 100°C, for almost 1200 hours. This temperature was selected because we wanted to keep the temperature low enough to not anneal out the radiation-induced defects we were trying to study. In addition, in [15], the authors presented data showing that the acceleration of the aging process saturated above this temperature. The five irradiated parts have from 96 to 197 errors, while none of the unirradiated controls have more than four errors. Therefore, we conclude there is clear evidence that the radiation dose has caused an increase in the number of bits suffering retention failures.

In Fig. 2, we show similar results for the Micron 16G parts, which were also baked at 100°C. The irradiated samples all have more than 300 errors, and the unirradiated samples all have fewer than 275 errors. We will discuss the details of the statistical analysis later, but the difference is statistically significant at the p = 0.95 level. That is, for both manufacturers, there is a statistically significant effect on retention properties from radiation exposure in a high temperature bake test.

For the Micron parts, that were cycled rather than baked, the results are less clear. For example, the irradiated group cycled to 10^5 P/E cycles, the mean error count for the five parts was 41, with a standard deviation of 25. For the unirradiated controls, the mean error count was 24, with a standard deviation of 17. These results are shown in Fig. 3 (irradiated samples) and Fig. 4 (unirradiated controls). That is, there is a difference between the groups, but it is not considered to be statistically significant because the variation within the groups is greater than or equal to the difference between the groups. We also show, in Fig. 5 (with radiation) and Fig. 6 (unirradiated), similar results for samples cycled to 10^4 P/E cycles. In Fig. 7 (irradiated) and Fig. 8 (unirradiated controls), we show results for Micron 8G parts not cycled at all, except for initial checkout and storing the original test pattern (one cycle). We will not discuss in detail the results at these lower cycle counts, because they are even less significant than the results at 10^5 P/E cyles. However, we note that the mean error count for the irradiated samples is slightly higher than for the unirradiated controls at all three P/E cycle levels. The difference is not statistically significant, however, because the variation within the groups is greater than the difference between the irradiated and unirradiated groups. For the cycled Micron 8G parts, a higher radiation dose would be expected to increase the number of radiation-induced retention failures, and at some dose the difference from the controls would become statistically significant. In the Micron case, the parts would have failed for other reasons before that dose was reached.

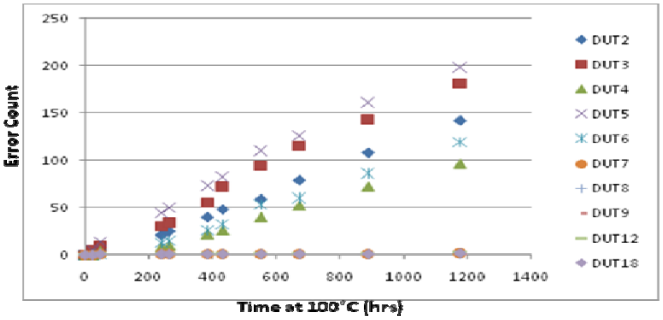

Fig 1. Error count for retention failures in Samsung 8G NAND flash, after baking at 100°C for more than 1000 hours. DUTs 2-6 wereirradiated to 200 krads (SiO_2); DUTs 7, 8, 9, 12, and 18 were unirradiated.

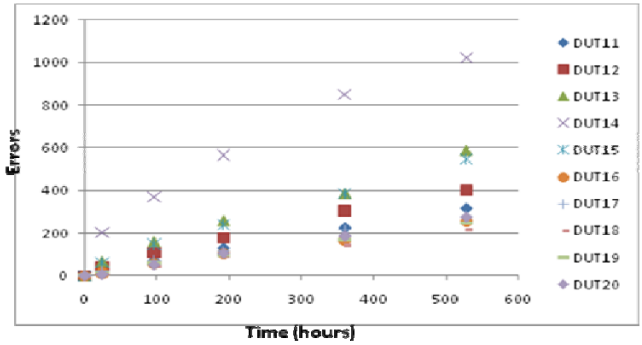

Fig. 2. Errors from retention failures for Micron 16G parts, baked at 100°C. DUTs 11-15 were irradiated to 50 krads (SiO_2); DUTs 16-20 are unirradiated controls.

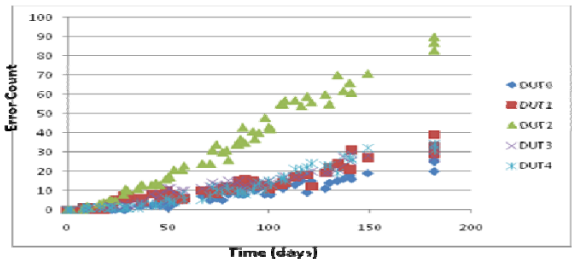

Fig. 3. Error counts for five Micron 8G samples, irradiated to 50 krads (SiO_2), then cycled to 105 P/E cycles, and monitored for at room temperature.

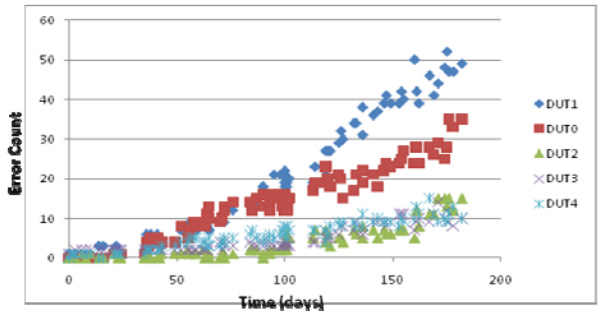

Fig. 4. Error counts for Micron 8G unirradiated controls, cycled to 105 P/E cycles.

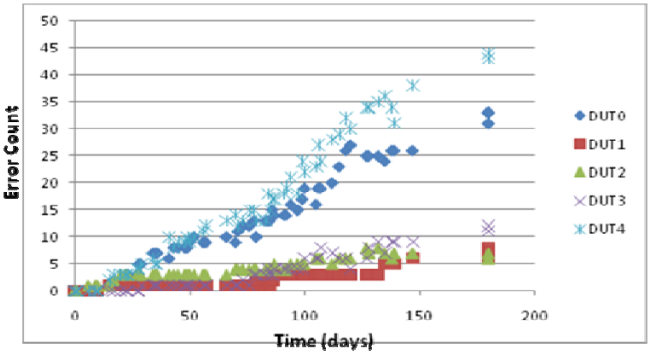

Fig. 5. Error counts for Micron 8G samples, exposed to 50 krads (SiO_2) and 104 P/E cycles.

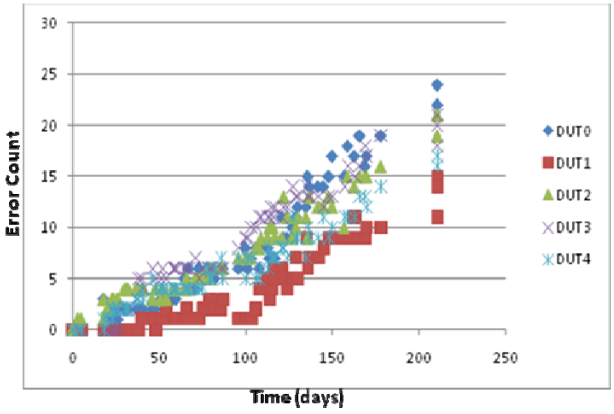

Fig. 6. Error counts for Micron 8G samples, unirradiated controls at 104 P/E cycles.

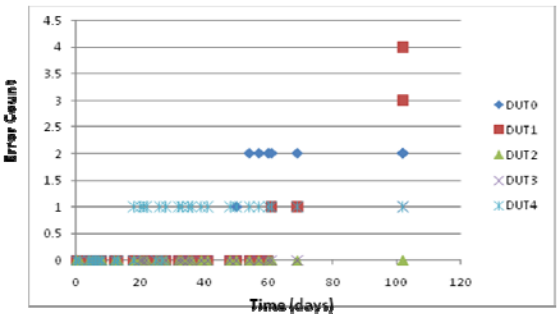

Fig. 7. Error counts for Micron 8G irradiated samples, with one P/E cycle.

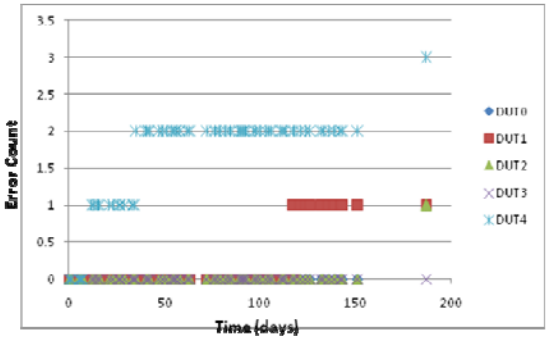

Fig. 8. Error counts for Micron 8G unirradiated controls, with one P/E cycle.

Next, we present statistical analysis, which supports the conclusion that the results for the parts baked at 100°C are statistically significant. In Table 2, we show the error counts for all the samples, along with the calculation of the mean (μ), the variance (σ^2), and the standard deviation (σ). Table 3 is similar to Table 2, but for the Micron 16G parts, which were also baked at 100°C. Table 4 is similar to Tables 2 and 3, for the Micron 8G parts cycled at to 10^5 P/E cycles.

We have applied the Student's t-test [21] to determine whether the difference between the test group (irradiated) and the control group (unirradiated) is significant, or not.

TABLE 2. DATA FOR SAMSUNG PARTS BAKED AT 100°C, WITH CALCULATIONS OF MEAN, VARIANCE (Σ2), AND STANDARD DEVIATION (Σ).

Samsung 8G, 100°C						
	No TID			200 krads (SiO_2)		
Sample	Errors	x-μ	$(x-\mu)^2$	Errors	x-μ	$(x-\mu)^2$
1	2	-0.4	.16	145	-2.6	6.8
2	1	0.6	.36	180	32.4	1050
3	1	0.6	.36	96	-51.6	2663
4	2	-0.4	.16	197	49.4	2440
5	2	-0.4	.16	120	-27.6	762
Total	8	0	1.2	738	0	6922
Mean	1.6			147.6		
σ^2	0.3			1730		
σ	0.54			41.6		

TABLE 3. DATA FOR MICRON 16G PARTS BAKED AT 100°C,WITH CALCULATIONS OF MEAN, VARIANCE, AND STANDARD DEVIATION.

Micron 16G, 100°C						
	No TID			50 krads (SiO_2)		
Sample	Errors	x-μ	$(x-\mu)^2$	Errors	x-μ	$(x-\mu)^2$
1	255	1.2	1.44	314	-260.2	67704
2	278	24.2	586	401	-173.2	29998
3	216	-37.8	1429	589	14.8	219
4	246	-7.8	61	1022	447.8	2.01E5
5	274	20.2	408	545	-29.2	853
Total	1279	0	2485	2871	0	2.99E5
Mean	253.8			574.2		
σ^2	621.2			74825		
σ	24.9			273.5		

TABLE 4. ERROR DATA FOR MICRON 8G PARTS IRRADIATED TO 50 KRADS (SiO_2), WITH CALCULATIONS OF MEAN, VARIANCE AND STANDARD DEVIATION.

Micron 8G, 10^5 P/E Cycles						
	No TID			50 krads (SiO_2)		
Sample	Errors	x-μ	$(x-\mu)^2$	Errors	x-μ	$(x-\mu)^2$
1	35	11.2	125.44	20	-21	441
2	49	25.2	635.04	38	-3	9
3	15	-8.8	77.4	85	44	1936
4	10	-13.8	190.44	32	-9	81
5	10	-13.8	190.44	30	-11	121
Total	119	0		205	0	2588
Mean	23.8			41		
σ^2	304.7			647		
σ	17.5			25.4		

The formula for the parameter, t, is shown in Fig. 9. It is the difference in the means for the test (irradiated) group and the control (unirradiated) group, divided by the standard error, which is given by the expression in the denominator of the equation in Fig. 9. That is, the variances of the two groups are divided by the number of samples in each group, and then one takes the square root of the sum. Once t is determined, it is compared to critical values of t, which can be looked up in standard tables [21], or calculated with standard software packages. For the data summarized in Tables 2-4, two groups of five samples each, t > 2.306 means there is more than 95% probability that the differences between the groups are not due to chance. As indicated in Fig. 9, the two tests where the parts were baked both have t greater than this value of tcrit. For the Micron 16G parts, t = 2.61, which exceeds tcrit at the level of p = 0.95. However the result is not significant with 99 % probability. For the Samsung 8G parts, t = 7.85, which means there is less than one chance in 10,000 the results are due to chance. For the Micron 8G parts, which were stressed by P/E cycling, none of the results met a rigorous statistical significance test, although, as we have noted, there were more errors in the irradiated samples in all cases. For the samples cycled to 105 P/E cycles, t = 1.23, which means there is less than 95% probability the differences are due to radiation. Actually, there is about one chance in four the results are simply due to chance.

Student's t-test for Statistical Significance

$$t = \frac{\mu_R - \mu_C}{\left[\frac{\sigma^2_R}{5} + \frac{\sigma^2_C}{5}\right]^{1/2}}$$

$t_{Micron\ (8G)} = (41-24) / [(647/5) + (305/5)]^{1/2} = 1.23$

$t_{Micron\ (16G)} = (574.2-253.8)/[(74825/5)+621/5)]^{1/2} = 2.61$

$t_{Samsung} = (147.6-1.6) / [(1730/5) + (0.3/5)]^{1/2} = 7.85$

t_{crit} = 2.306 at 0.95 probability
= 3.355 at 0.99 probability
= 5.041 at 0.999 probability

Fig. 9. Student's t-test: t is determined from the equation in the Figure, along with t-values for the three tests summarized in Tables 2-4, and critical t-values for selected confidence levels.

The point of the cycling experiments reported here is to determine if flash memory in, say, a solid state recorder (SSR) would start to experience radiation-induced retention problems after a certain time in orbit, which would correspond to some number of P/E cycles. For example, if the memory is read out once a day and then rewritten, it would have about 1000 P/E cycles after about three years, and it would have to retain data for about a day, until the next rewrite operation. Could there be a radiation-induced retention failure under these circumstances? From the results presented here, it seems clear the answer is "No". The results in Figures 3 and 4 are for parts cycled to a level two orders of magnitude past 1000 cycles. The interval after cycling is hundreds of days, not one day. This is also about two orders of magnitude beyond the operational requirement. Even with an over-test of two orders of magnitude in both cycle count and retention interval, there is no statistically significant effect due to radiation, at least for the parts tested.

V. CONCLUSION

There are three points to be made about the results presented here. First, any radiation effect will have a clear dependence on the dose level. For the two cases of high temperature baking, both were statistically significant, but the Samsung results were significant to a much higher confidence level than the Micron results. However, the Samsung dose was also 4X greater. One would think that, if the Micron parts could have survived 200 krads (SiO_2), the radiation effect would have been even clearer at the higher dose.

The second point concerns the difference between the high temperature baking results, and the results on P/E cycled parts. Both radiation and P/E cycling introduce trapped holes into the tunnel oxide. One would expect that the effect of radiation-induced hole traps would be harder to resolve, when another known physical process is also introducing hole traps. This is especially true when the dose is relatively low to begin with. At higher doses, the radiation effect would probably have become statistically significant in the cycling

experiments, too, eventually. As we have already pointed out, in some cases, unhardened commercial parts are likely to fail for other reasons, before the impact of radiation on retention becomes significant. We note that typical device failure is based on functional operations and not cell failure.

Third, as we have already pointed out, the retention specifications of the manufacturers assume error correction will be used. However, in this test, it was not used. It is likely that all the errors observed here would be corrected by robust error correction software. That is, the apparent retention "failures" that we are reporting might not be real system level errors. This point should be addressed through further testing. We have obtained clear evidence that radiation exposure can induce physical processes that cause measurable reliability effects, under some circumstances. However, the circumstances are complicated enough, that it is not clear whether these effects will have major system impacts, or not.

ACKNOWLEDGMENT

This work was supported in part by the NASA Electronic Parts and Packaging Program (NEPP), and the Defense Threat Reduction Agency (DTRA) under IACRO# 11-4395I. The authors wish to thank Martha O'Bryan for technical assistance in preparing both the poster and the final manuscript for this paper.

REFERENCES

[1] T.R. Oldham, M. Friendlich, M.A. Carts, C.M. Seidleck, amd K.A. LaBel, Effect of radiation exposure on the endurance of commercial NAND flash memory, IEEE Trans. Nucl. Sci., vol. 56, no. 6, pp. 3280-3284, Dec. 2009.

[2] T.R. Oldham, M.R. Friendlich, and S.R. Cox, Total Dose 4G Micron Test Report for Micron 4G NAND Flash Nonvolatile Memory, http://radhome.gsfc.nasa.gov, 2009.

[3] T.R. Oldham, M.R. Friendlich, and S.R. Cox, Total Dose Test Report for Samsung 8G NAND Flash Nonvolatile Memory, http://radhome.gsfc.nasa.gov, 2008.

[4] T.R. Oldham, M.R. Friendlich, and D. Chen, Total dose test report for Samsung 8G NAND Flash nonvolatile Memory, http://radhome.gsfc.nasa.gov, 2011.

[5] T.R. Oldham, M.R. Friendlich, and M.A. Carts, Total dose test report for the Micron 8G NAND flash memory, http://radhome.gsfc.nasa.gov, 2011.

[6] T.R. Oldham, D. Chen, and M. Friendlich, Total dose test report for the Micron 16G NAND flash memory, http://radhome.gsfc.nasa.gov, 2011.

[7] N. Mielke and J. Chen, "Reliability of Flash Nonvolatile Memories," pp. 103-134, in Oxide Reliability, ed. by D.J. Dumin, Selected Topics in Electronics and Systems, vol. 23, World Scientific Press, Singapore, 2002.

[8] A. Scarpa, A. Paccagnella, F. Montera, G. Ghibaudo, G. Pananakakis, G. Ghidini, and P.G. Fuochi, Ionizing radiation induced leakage current in ultra-thin gate oxides, IEEE Trans. Nucl. Sci., vol. 44, no. 6, pp. 1818-1825, Dec. 1997.

[9] TRIAD Spectrum, http://www.triadspectrum.com

[10] J.W. Howard, et al. "Development of a Low Cost and High Speed Single Event Effects Tester based on Reconfigurable Field Programmable Gate Arrays (FPGA)," Presented at SEE Symposium 2006, Long Beach, Apr. 2006.

[11] Department of Defense "Test Method Standard Microcircuits," MIL-STD-883 Test Method 1019.8 Ionizing radiation (total dose) test procedure, http://www.dscc.dla.mil/Downloads/ MilSpec/Docs/MIL-STD-883/std883_1000.pdf, Sept. 2010.

[12] F. Arai, T. Maruyama, and R. Shirota, Extended data retention process technology for highly reliable flash EEPROMs of 106 to 107W/E cycles, Proc. Int. Reliability Phys. Symp., pp. 378-382, 1998.

[13] D. Ielmini, A.S. Spinelli, A.L. Lacaita, A. Modelli, A statistical model for SILC in flash memories, IEEE Trans. Electron Dev., vol. 49, no. 11, pp. 1955-1961, 2002.

[14] A. J. Lelis, H. E. Boesch, T. R. Oldham, and F. B. McLean, Reversibility of trapped hole annealing, IEEE Trans. Nucl. Sci., vol. 35, no. 6, pp. 1186-1191, 1988.

[15] A. J. Lelis, T. R. Oldham, H. E. Boesch, Jr., and F. B. McLean, The nature of the trapped hole annealing process, IEEE Trans. Nucl. Sci., vol. 36, no. 6, pp. 1808-1815, 1989.

[16] A. J. Lelis, and T. R. Oldham, Time dependence of switching oxide traps, IEEE Trans. Nucl. Sci., vol. 41, no. 6, pp. 1835-1843, 1994.

[17] D. James, Nano-scale flash in the mid-decade, IEEE/SEMI Advanced Manufacturing Conference Proceedings, pp. 371-376, 2007.

[18] H.P. Belgal, N. Righos, I. Kalastirsky, J.J. Peterson, R. Shiner, and N. Mielke, A new reliability model for post-cycling charge retention of flash memories, IEEE Proceedings of the 40th International Reliability Physics Symposium, pp. 7-20, 2002.

[19] M. Herrmann and A Schenk, Field and high-temperature dependence of long term charge loss in erasable programmable read only memories: measurements and modeling, J. Appl. Phys., vol. 77, no. 9, pp. 4522-4540, 1995.

[20] B. De Salvo, G. Ghibaudo, G. Pananakakis, G. Reimbold, F. Mondond, B. Guillaumot, and P. Candelier, Experimental and theoretical investigation of nonvolatile memory data retention, IEEE Trans. Electron Dev., vol. 46, no. 7, pp. 1518-1524, 1999.

[21] R.S. Burington and D.C. May, Handbook of Probability and Statistics with Tables,2nd edition, McGraw-Hill, New York, NY, 1970.