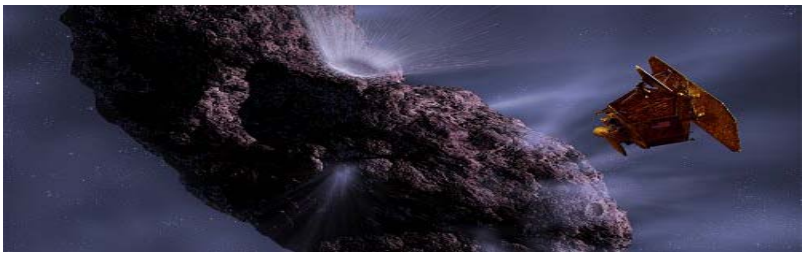
New Approaches to Single Event Effect Characterization of Parallel and Serial Analog to Digital Devices



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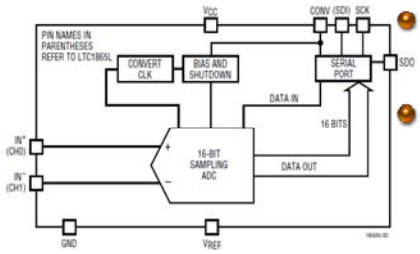
Motivation

- Single Event Effects (SEE) test methodologies of Serial Analog to Digital Converters (ADCs) and Parallel ADCs are not equivalent
  - Architectures differ:
    - Serial: Sample and hold successive approximation
    - Parallel: Flash
  - Parallel ADCs tend to be significantly faster than Serial ADCs
- SEE testing is not equivalent to manufacturer parametric testing
  - We are not characterizing ENOB
  - We are characterizing the number of upsets that will occur based on the number (and type) of particles the device is exposed to.
- The aforementioned points frame SEE test development for Serial and Parallel ADCs

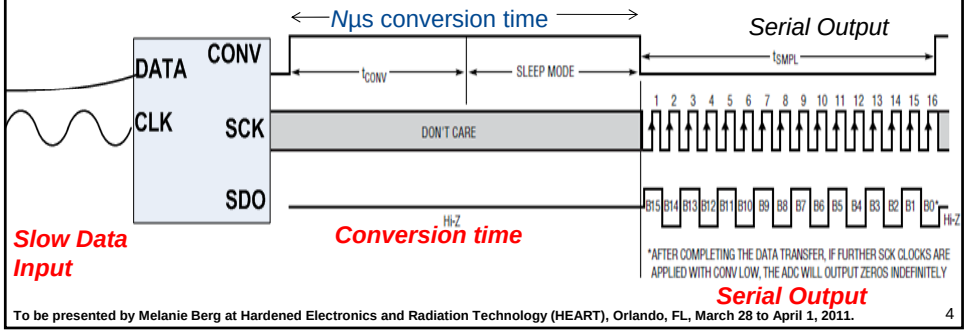
Overview

- **Serial ADCs:**
  - Architecture and operation
  - Manufacturing versus SEE testing
  - Old versus New Test Setup
  - Synopsis of Test Methodology
- **Parallel ADCs:**
  - Architecture and operation
  - Manufacturing versus SEE testing
  - Old versus New Test Setup
  - Synopsis of Test Methodology

Serial ADCs

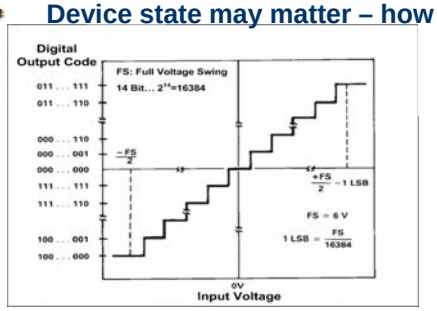


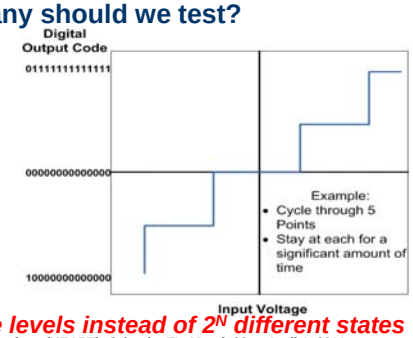
- **Input Data is in the order of KHz**
- **Generally used to measure slowly changing device outputs (e.g. current, temperature, etc…)**



Serial ADC Parametric Testing versus SEE Testing

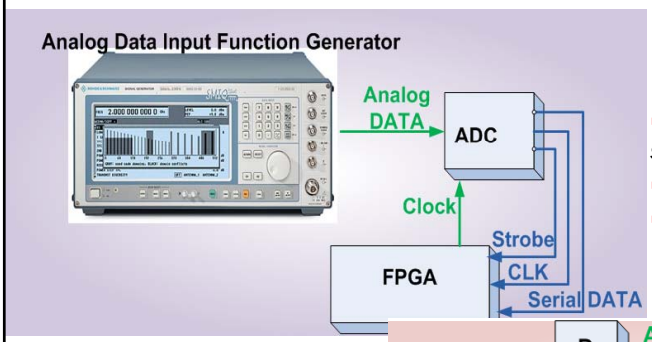
- SEE upsets occur for a limited amount of time and will not effect ENOB.
- ENOB Parametric testing requires 2^N codes to be evaluated
- SEE upsets are random & can cause multiple bits to flip due to analog transients
- Do we need to test every voltage input code (2^N states) during SEE tests?
- Device state may matter – how many should we test?





Only Test Strategic Voltage levels instead of 2^N different states

SEE Testing of Serial ADCs

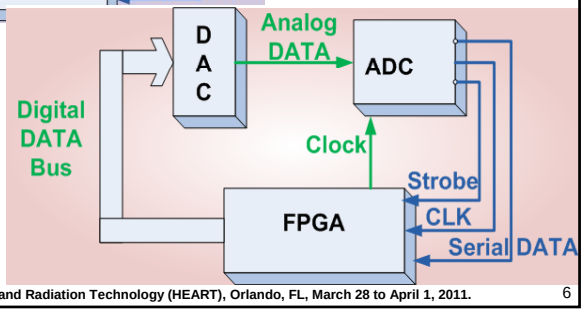


Original Test Set:

- ***Data and clock are from separate sources***
- ***Less Control***
- ***Generator can be noisy***

New Test Set:

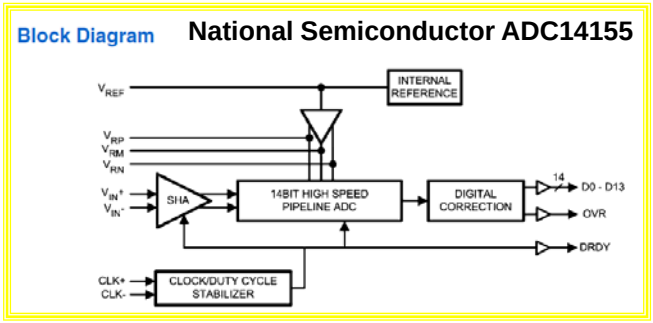
- ***Data and clock are from same source (FPGA)***
- ***Enhanced Control***
- ***Must Reduce DAC to ADC noise***

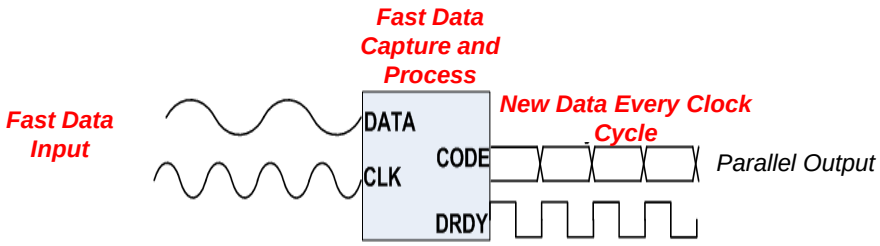


Serial ADC Test Methodology

- Determine whether test will have static or dynamic inputs
  - If all tests have static data inputs, then multiple tests are necessary at various voltage inputs
    - Helps to determine susceptibility across various ADC states
    - Stress the device during testing
  - If tests are dynamic, data variation must be slow
    - Device conversion time
    - Stay at value long enough to obtain good statistics (also based on particle flux)
- Prior to radiation exposure, calculate expected values
- During irradiation, compare digital output code-words to expected values (noise error-bound)

Parallel ADCs





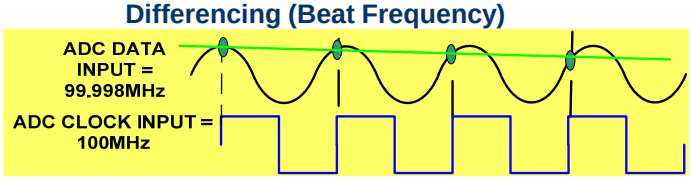
Traditional Parallel ADC Parametric Testing

- Input Data is slightly slower than clock
- Assumes noise is distributed evenly (consistently) through every clock cycle

N point FFT used for noise parameterization

$$X(k) = \sum_{n=0}^{N} x(n) \cdot e^{-j2\pi nK/N}$$

Differencing (Beat Frequency)

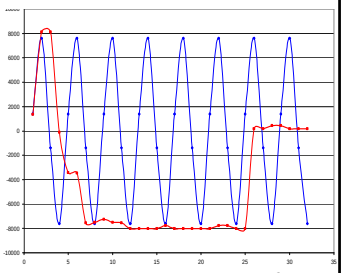


Approximately one sample point per signal period

Because noise is distributed, it is acceptable to start and stop sampling in order to process FFT

Why Parametric Parallel ADC Testing Does Not Apply to SEE Testing

- Noise due to SEEs affects only one clock cycle or a limited number clock cycles
- Hence noise is not equally distributed
- Can not start and stop sampling – SEUs are random
- Sampling only one point per cycle will not obtain error signature information
- However, generalized error rates can be obtained
- Additional noise inserted into test system to create the "beat frequency" clock data relationship

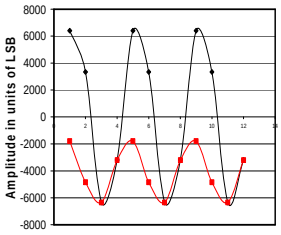


SEU error Rates can be more accurate by using an alternate method

National Semiconductor ADC14155 Error Signatures

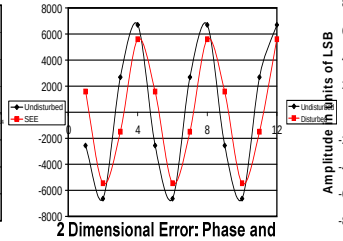
- ***At Lower LETs and proton testing jitter was dominant***
- ***Below are interesting SEEs at higher LETs***
- ***Flattening was also observed, just not shown here***

ADC14155 Burst: LET = 41.5MeV-cm^2/mg @ 100MHz



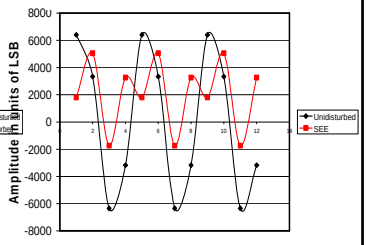
Amplitude Effects; Clock Circuitry unaffected

ADC14155 Burst: LET = 29.56MeV-cm^2/mg @ 100MHz



2 Dimensional Error: Phase and Amplitdue; Clock circuitry is affected

ADC14155 Burst: LET = 41.5MeV-cm^2/mg @ 100MHz



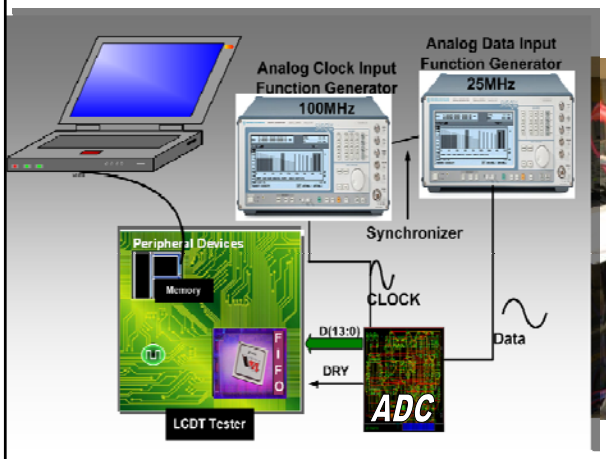
Loss of Signal Composition:

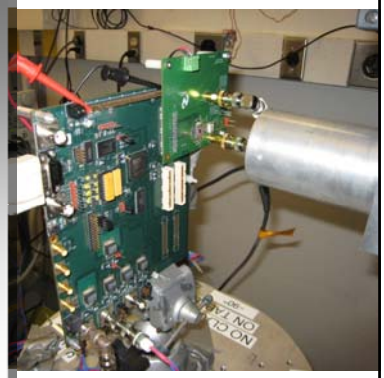
Need more than one sample point per cycle to obtain this detail of observation: Hence Development of 4-Point Method

What's Happening

- **In most cases, SEEs incur in the analog circuitry as a transient**
  - How long does the transient last
  - Is it in the data path such that it gets latched into the code
  - Is it in the clock circuitry such that the sampling is phase shifted
  - Is it in the voltage regulation such that all the codes will be shifted or noisy
  - Will last multiple cycles
- **SEUs can incur in the digital logic and are usually are single cycle**

Parallel ADC 4-Point Test Setup: Low Cost Digital Tester (LCDT) and Texas A&M Heavy Ion Setup





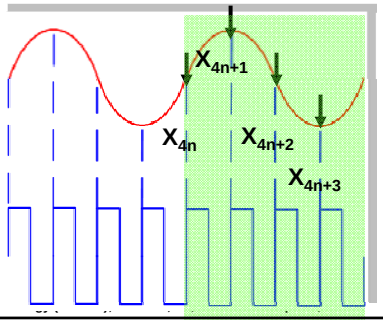
To be presented by Melanie Berg at Hardened Electronics and Radiation Technology (HEART), Orlando, FL, March 28 to April 1, 2011. 13

4-Point SEE Parallel ADC Testing

- Calculate 4 expected values (E0…E3)
- Compare incoming sample points ($X_{m \bmod k}$) to expected values (E_k) (e.g. compare X0 to E0)
- Due to noise in test setup – digital outputs will never always be exactly the same

$$(E_k - errorbound) < X_{m \bmod k} < (E_k + errorbound)$$

$$k = (0,1,2,3); m = (1..\infty)$$



More information each data cycle

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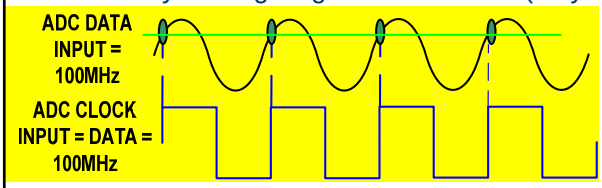
Parallel ADC Full SEE Testing

- **4-Point Methodology is used to characterize error signatures**
  - Two Signal Generators are required
    - Clock
    - Data
  - Due to the synchronization of Signal Generators noise is added into test system
- **General SEE characterization**
  - Single Point Testing is performed
  - Can not differentiate between upsets
  - Only one signal generator is used (very low noise)



Single Point: One Point of Observation per Signal Period

M. Berg et. al,"Enhancing Observability of Signal Composition and Error Signatures during Dynamic SEE Analog to Digital Device Testing" RADECS 2009

Conclusion

- **Manufacturers perform error rate testing**
  - Error rates have to do with intrinsic device noise
  - Noise is distributed throughout the data input signal
- **Manufacturing Parameterization and SEU testing must be differentiated**
  - Tests are not formed to evaluate the same noise source
  - Tests are not formed to detect the same error signatures
- **Due to architectural differences Serial ADC SEE test methodologies differ from Parallel ADCs**
- **All points in this presentation refer to SEE testing. It is best to use parametric tests for Total Ionizing Dose (TID) testing**