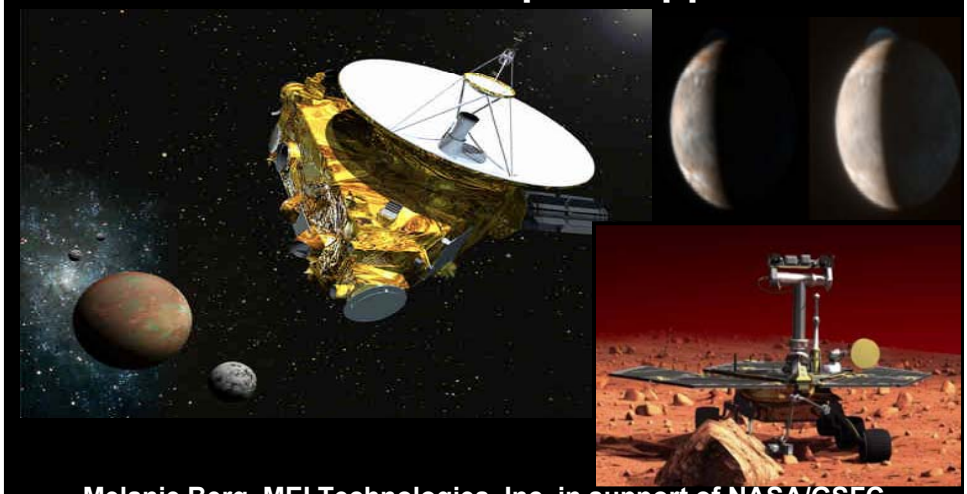
Single Event Upset (SEU) Test and Analysis of Field Programmable Gate Array (FPGA) Devices for Critical Space Applications



Melanie Berg, MEI Technologies, Inc. in support of NASA/GSFC

Acknowledgements

- ***Some of this work has been sponsored by the NASA Electronic Parts and Packaging (NEPP) Program and the Defense Threat Reduction Agency (DTRA)***
- ***Thanks is given to the NASA Goddard Radiation Effects and Analysis Group (REAG) for their technical assistance and support. REAG is led by Kenneth LaBel and Jonathan Pellish***

Abstract

- **The intent of this presentation is to:**
  - **Describe the complex nature of performing Field Programmable Gate Array (FPGA) Single Event Upset (SEU) radiation testing**
  - **Illustrate how such tests can be mapped into device characterization for critical project usage**

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Before we get started… here are some things to keep in mind during this presentation

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Single Event Effects (SEEs) and Common Terminology

- Single Event Latch Up (SEL): Device latches in high current state
- Single Event Burnout (SEB): Device draws high current and burns out
- Single Event Gate Rupture: (SEGR): Gate destroyed typically in power MOSFETs
- Single Event Transient (SET): current spike due to ionization. Dissipates through bulk
- Single Event Upset (SEU): transient is caught by a memory element. Causes an incorrect state. SETs are categorized under SEUs
- Single Event Functional Interrupt (SEFI) - upset disrupts function

SEU Radiation Testing

- Exposing a Device-Under-Test (DUT) to a radiation source and monitoring the DUT's response is the primary method for on-ground SEU evaluation
- SEU testing requires counting the number of upsets that occur while exposing a DUT to a given number of ionizing particles.
- A common test metric is the SEU cross-section (σ_{SEU}).

$$Fluence = (Number\,of\,Particles\,during\,Exposure)/cm^2$$

$$\sigma_{SEU} = \frac{Number\,of\,Upset\,Events}{(Number\,of\,Particles\,during\,Exposure)/cm^2}$$

Motivation

- A goal of SEU testing is to provide critical missions upper-bound error rate predictions for their specific FPGA design applications
- σ_{SEU}s are used to calculate bit upset rates ($dE_{bit}(f_s)/dt$)
- Upper bound Design/System error rate ($dE(f_s)/dt$) predictions for FPGA devices are calculated by using:
  - The implemented number of bits (i.e., flip-flops, D flip-flops (DFFs), or configuration bits) in a design and
  - ($dE_{bit}(f_s)/dt$)) from SEU testing

$$\frac{dE(fs)}{dt} < \frac{dE_{bit}(fs)}{dt} * (\#UsedDFFs)$$

Design Upset rate — *bit Upset rate* — *Number of bits in the design*

Bit Upset Rates and SEUs

- What is a bit upset with regard to an SEU?
  - It is not simply a storage element flipping its state
  - There's a difference between upset generation, upset capture, and operational failure
  - There are a variety of elements in a design that contribute to bit upset rates
- How do we determine bit upset rates?
  - Understand the elements that constitute the DUT-FPGA
  - Determine DUT-FPGA test structures.
  - Test and Analyze the SEU data
    - Differentiate upset types
    - Develop trends: Frequency, data pattern, design topology
    - Determine upsets with respect to number of bits implemented

FPGA Devices: Understanding the Elements that Constitute the FPGA Fabric

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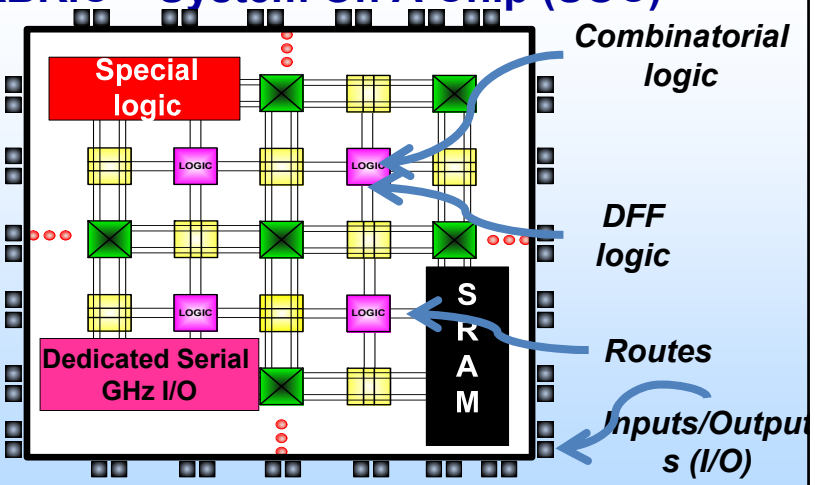
Field Programmable Gate Array (FPGA) FABRIC – System On A Chip (SOC)



User creates a design by configuring pre-existing logic blocks and routes.

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FPGA Element Definitions

Element	Definition
Configuration	A static definition of the function. It consists of elements that hold information regarding: • The identification of selected FPGA logic blocks • The mapping function of the selected logic blocks • Interconnects between logic blocks • I/O definitions
Functional logic data-path	The cells that perform the operation: Combinatorial logic blocks, routes, sequential logic blocks, and I/O blocks.
Global Routes	Clock trees, resets, and high fan-out nets

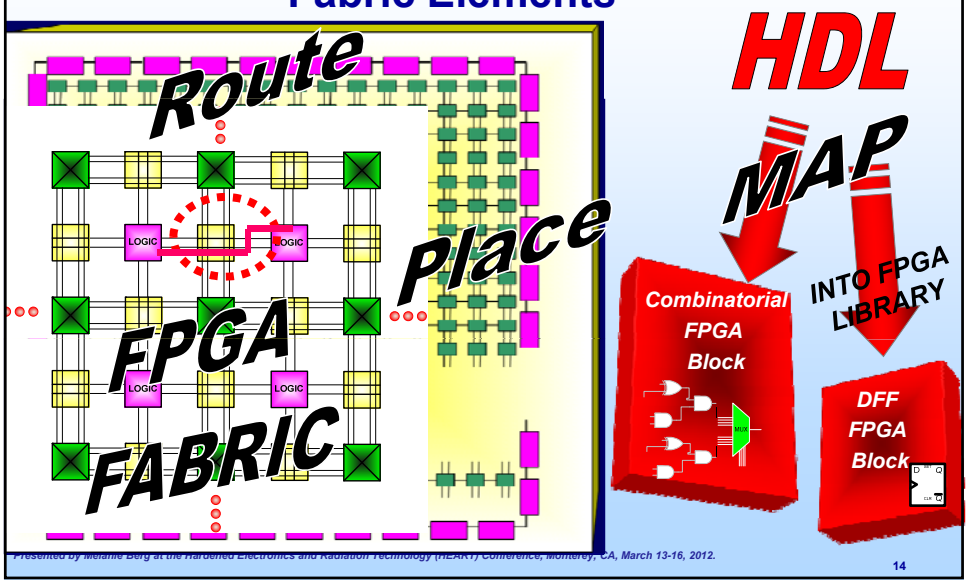
Check the FPGA Data Sheet Prior to Test Development-1

- **What types of elements exist in the DUT-FPGA to test? – e.g., types of:**
  - **DFFs, combinatorial logic structures, global routing,**
  - **configuration,**
  - **hidden logic circuits, etc,…**
- **Are any of the elements mitigated or hardened?**
- **How much power does the DUT-FPGA consume? – e.g., is cooling equipment required during testing?**
- **Are additional devices necessary to operate the DUT-FPGA such as a configuration manager or memory elements?**

Check the FPGA Data Sheet Prior to Test Development-2

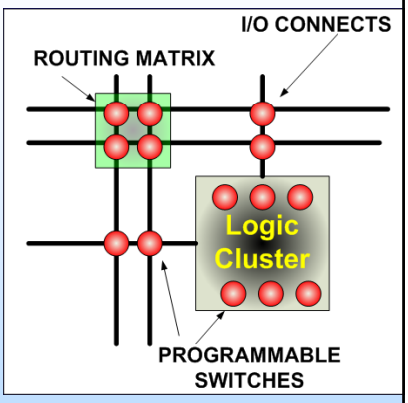
- Is special testing equipment required to operate the DUT-FPGA at its maximum speeds?
- What are the switching characteristics of the I/O:
  - will the I/O speed limitations restrict maximum frequency test-structure evaluations? Or
  - will the output switching characteristics cause signal integrity issues if not handled properly?

Creating a Design: Mapping Hardware Description Language (HDL) into FPGA Fabric Elements



Place, Route, and Gate Utilization are Stored in the FPGA Configuration

- ***Configuration Defines:***
  - ***Functionality (logic cluster)***
  - ***Connectivity (routes)***
  - ***Placement***



- ***Configuration Switch Types:***
  - ***Antifuse:*** ***One time Programmable (OTP)***
  - ***SRAM:*** ***Reprogrammable (RP)***
  - ***Flash:*** ***Reprogrammable (RP)***

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FPGA Devices: Understanding the Element SEU Susceptibility

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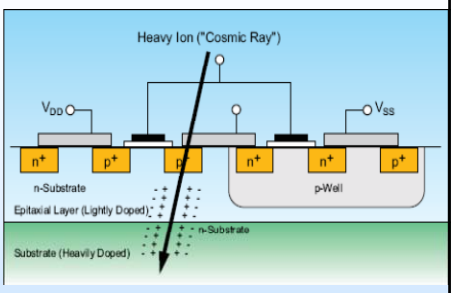
Device Penetration of Heavy Ions and Linear Energy Transfer (LET)

- LET characterizes the deposition of charged particles
- Based on Average energy loss per unit path length (stopping power)
- Mass is used to normalize LET to the target material



Average energy deposited per unit path length

$$LET = \frac{1}{\rho}\frac{dE}{dx} \; ; \; MeV\frac{cm^2}{mg}$$

Units

Density of target material

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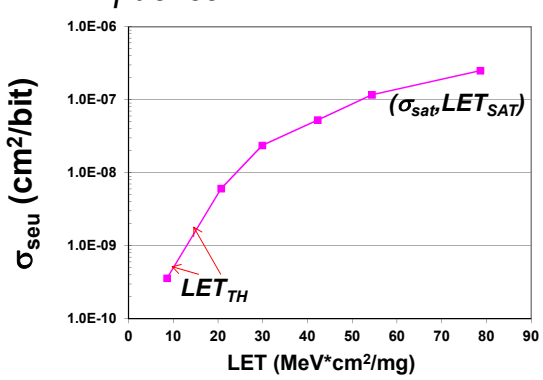
Characterizing SEUs: LET vs. Error Cross Section Graph and How They Relate to Error Rates

$$\sigma_{seu} = \frac{\#errors}{fluence}$$

dE/dt is calculated by integrating σ_{SEU} over the LET spectrum using a Weibull fit



Geostationary Earth Orbit (GEO) Upset Rate:

$$\frac{dE}{dt} \approx \frac{400 * \sigma_{sat}}{LET_{th}^{2}}$$

After Ed Petersen's figure of merit

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Differentiating FPGAs (SEU) Susceptibility

$$P(fs)_{error} \propto P_{Configuration} + P(fs)_{functionalLogic} + P_{SEFI}$$

Design Specific probability of upset

Configuration probability of upset

Functional logic probability of upset

Probability of Single Event functional Interrupt

Upsets from DFFs and Combinatorial Logic

Probabilities are proportional to σ_{SEU}

Must Clearly state which SEU type is being evaluated… Beware… sometimes difficult to differentiate

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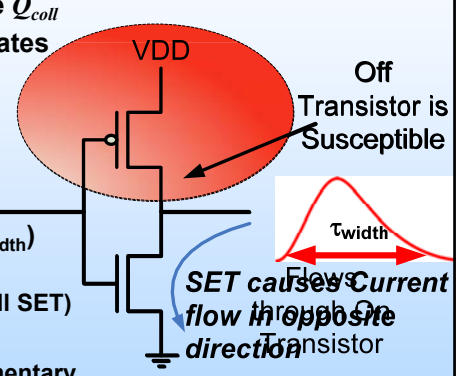
SET Generation

- **SET generation occurs due to an "off" gate turning "on".**
- **For a CMOS SET: there is a push-pull between the on gate and the off gate Q_{coll}**
- **SETs have significant metastable states**

Collected Charge ***Critical Charge***

$$Q_{coll} > Q_{crit}$$



- **SET has an amplitude and width (τ_{width}) based on:**
  - **Amount of Q_{coll} (i.e. small LET →small SET)**
  - **The capacitance of the gate's load**
  - **The strength (current) of its complimentary "ON" gate**
  - **The dissipation strength of the process.**
- **Captured SET is a SEU**

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General Concepts of FPGA SEU Susceptibility

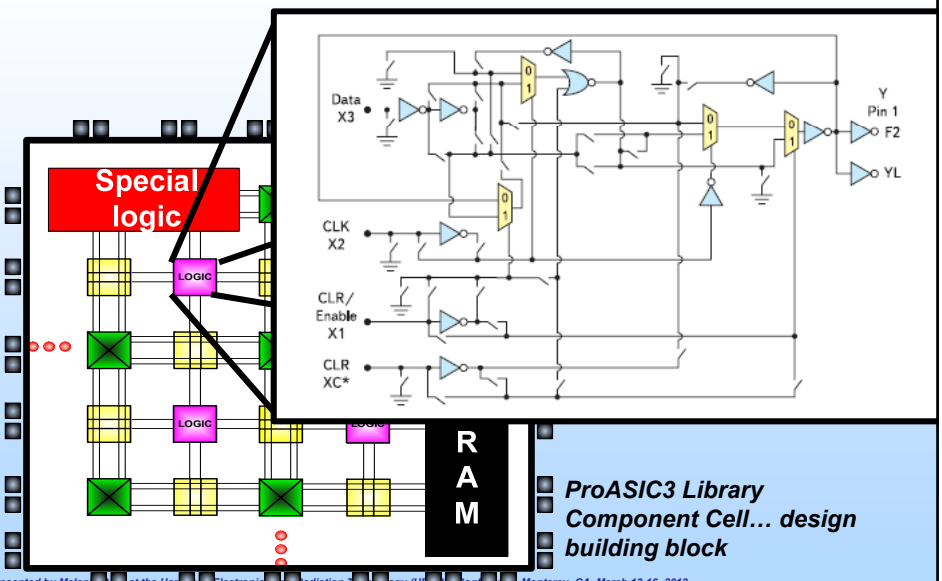
- We will only address the susceptibility of the 2 basic technology nodes of a FPGA device:
  - Configuration
  - Functional logic Blocks/routes
- Configuration and Functional logic are different technology nodes with different SEE upset rates
- Functional blocks can vary in susceptibility:
  - Fanout
  - Unused (don't care) logic
  - Highly capacitive routing matrices
  - Frequency of operation
  - Data pattern
  - Levels of functional blocks between flip flops (DFFs

Variation of technology, functional logic blocks, and complexity of design topology make it no longer valid to simply count upsets during SEU testing

Configuration

$$P(fs)_{error} \propto P_{Configuration} + P(fs)_{functionalLogic} + P_{SEFI}$$

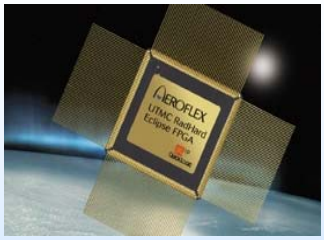
A Closer Look at an FPGA Logic Cell: Microsemi ProASIC3



ProASIC3 Library Component Cell… design building block

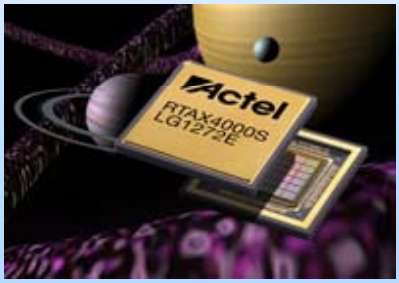
FPGA Categorized by Configuration Types

Antifuse



SRAM

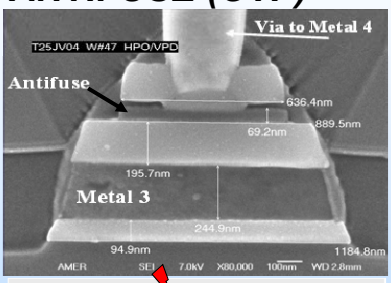
Antifuse



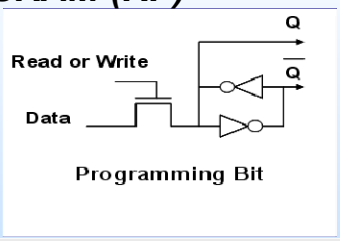
Flash

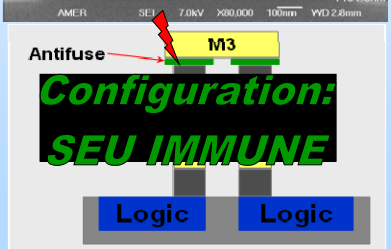
Programmable Switch Implementation and SEU Susceptibility

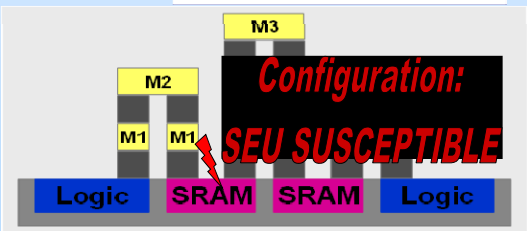
ANTIFUSE (OTP)



SRAM (RP)







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Configuration SEU Test Results and the REAG FPGA SEU Model

$$P(fs)_{error} \propto P_{Configurat\ \ ion} + P(fs)_{functional\ \ Logic} + P_{SEFI}$$

Configuration	REAG Model
Antifuse	$P(fs)_{error} \propto P(fs)_{functionalLogic} + P_{SEFI}$
SRAM **(non-mitigated)**	$P(fs)_{error} \propto P_{Configuration}$
Flash	$P(fs)_{error} \propto P(fs)_{functionalLogic} + P_{SEFI}$
Hardened SRAM	$P(fs)_{error} \propto \cancel{P_{Configuration}} + P(fs)_{functionalLogic} + P_{SEFI}$

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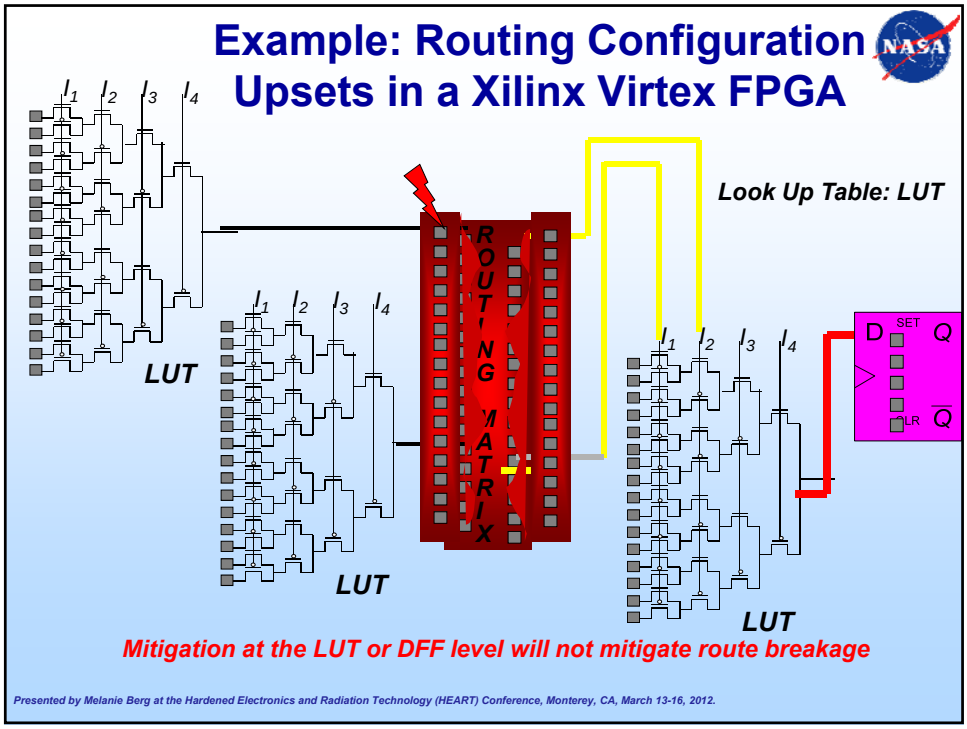
Example: Routing Configuration Upsets in a Xilinx Virtex FPGA
Look Up Table: LUT
LUT
LUT
LUT
ROUTING MATRIX
D
SET
Q
LR
Q
Mitigation at the LUT or DFF level will not mitigate route breakage
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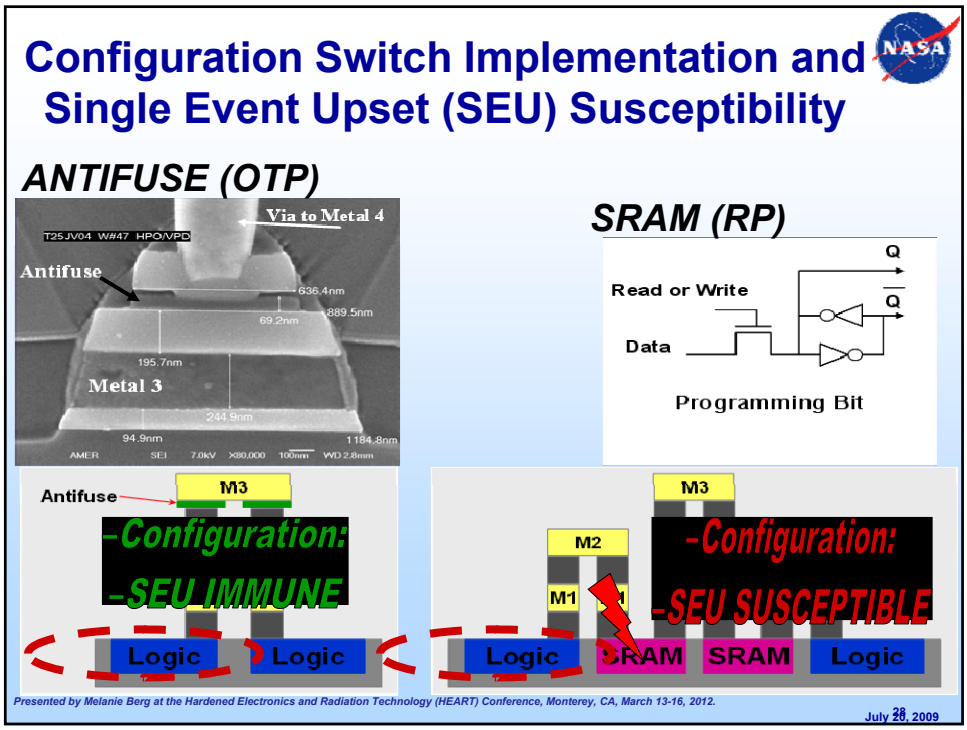
Configuration Switch Implementation and Single Event Upset (SEU) Susceptibility
ANTIFUSE (OTP)
Via to Metal 4
Antifuse
Metal 3
SRAM (RP)
Read or Write
Data
Q
Programming Bit
Antifuse
M3
-Configuration:
-SEU IMMUNE
Logic
Logic
M3
M2
M1
-Configuration:
-SEU SUSCEPTIBLE
Logic
SRAM
SRAM
Logic
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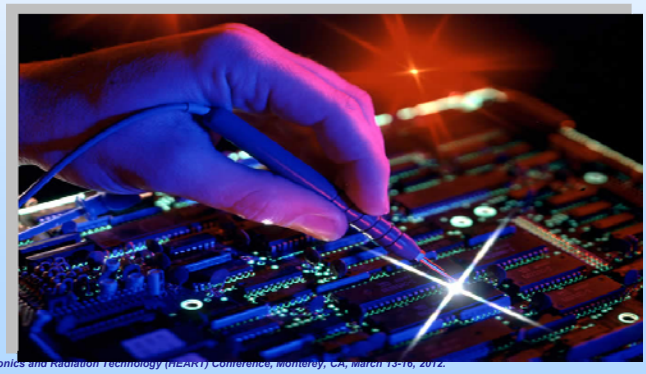
July 28, 2009

Functional Data Path SEU Modeling

$$P(fs)_{error} \propto P_{Configurat\ ion} + P(fs)_{functional\ Logic} + P_{SEFI}$$



Goal of this Section

- **Differentiate SET/SEU generation from capture**
- **Model how design topology affects SET/SEU capture**
- **Information is used to**
  - **Develop test structures**
  - **Analyze SEU data**

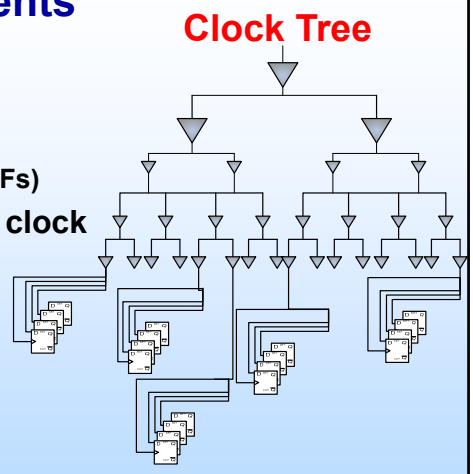
Synchronous Design Methodology and SEU Modeling

- Design topology dictates SEU susceptibility
  - Edge triggered Flip flops (DFFs) versus latches
  - Logic cells: Sea of gates versus look up tables (LUTs)
  - High capacitive routing
  - Large fan-out or large fan-in or feedback paths
- Synchronous design has proven to be the most reliable means of design and is the most common design strategy used world wide
  - Makes state transitioning deterministic
  - Provides distinct boundary points – relates state to clock cycle
  - Easiest method to verify
  - Automated design tools are geared for synchronous methodology

This presentation pertains to synchronous designs

Synchronous Design Data Path Components

- Designs are comprised of:
  - Combinatorial Logic (CL)
  - Edge Triggered Flip-Flops (DFFs)
- All DFFs are connected to a clock
- Clock period: τ_{clk}
- Clock frequency: f_s



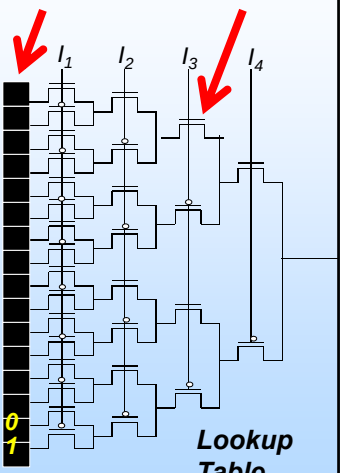
$$\tau_{clk} = \frac{1}{fs}$$

The premise of synchronous design is to compute and hold in a deterministic manor

Combinatorial Logic: Data Path Computation

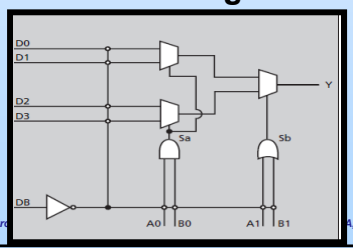
- Output is affected by inputs after gate delay
- Used for computing or routing
- FPGAs provide blocks of combinatorial logic (library components)… blocks vary per manufacturer
- Combinatorial Loops are not allowed in synchronous design

Xilinx Virtex LUT uses SRAM + Combinatorial



Lookup Table LUT

RTAXs C-CELL: Does not require SRAM



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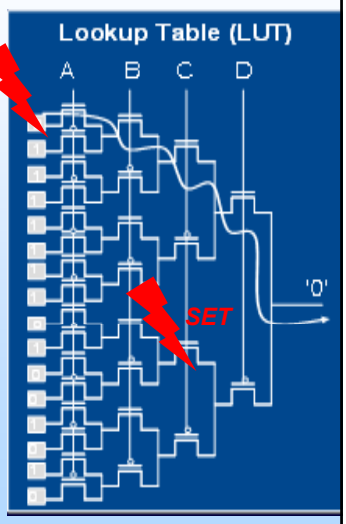
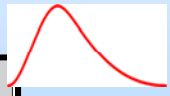
SETs and Combinatorial Logic

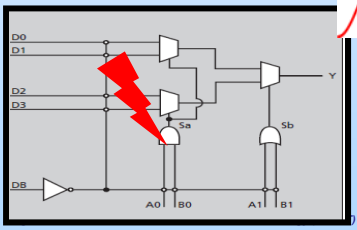
- SETs are double sided functions
- Because there are no combinatorial logic loops, SETs are not captured by the combinatorial path
- In SRAM based FPGAs:
  - SET in combinatorial logic path
  - SEU in configuration

SEU



SET





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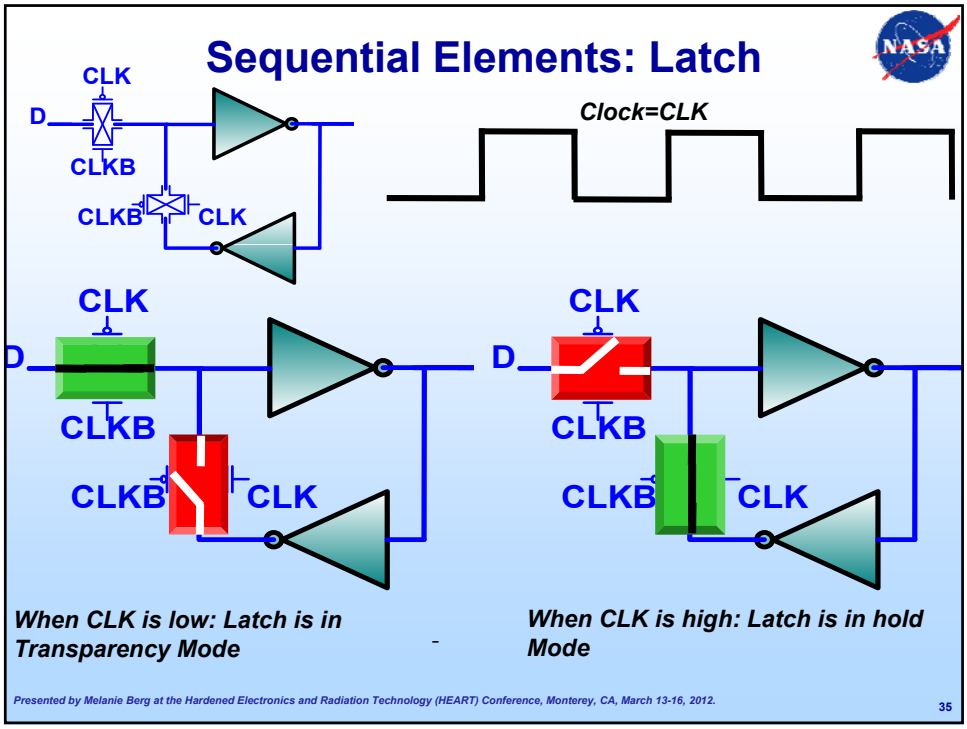
Sequential Elements: Latch
CLK
D
CLKB
CLKB
CLK
Clock=CLK
CLK
D
CLKB
CLKB
CLK
CLK
D
CLKB
CLKB
CLK
When CLK is low: Latch is in Transparency Mode
When CLK is high: Latch is in hold Mode
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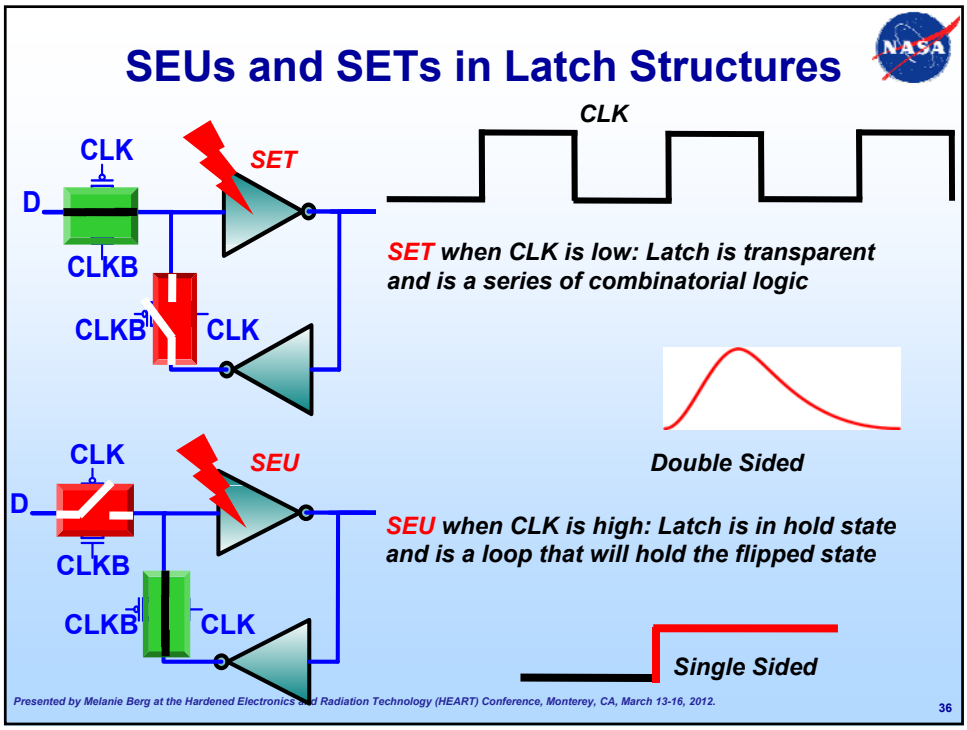
SEUs and SETs in Latch Structures
CLK
SET
D
CLK
CLKB
CLKB
CLK
SET when CLK is low: Latch is transparent and is a series of combinatorial logic
Double Sided
CLK
SEU
D
CLKB
CLKB
CLK
SEU when CLK is high: Latch is in hold state and is a loop that will hold the flipped state
Single Sided
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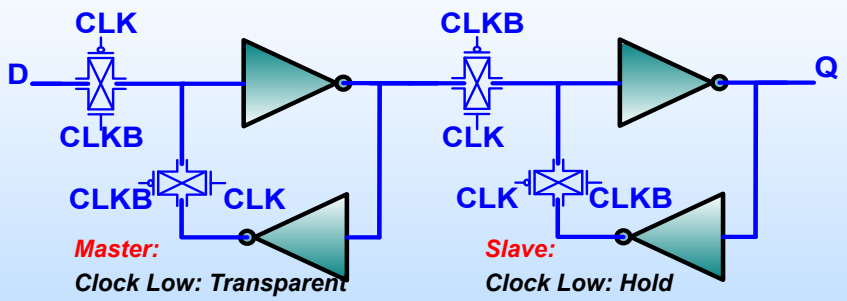
Edge Triggered Flip Flops... Creating Deterministic Boundary Points

D input must be settled by rising edge of clock

Output will only change at rising edge of clock



Master:
Clock Low: Transparent
Clock High: Hold

Slave:
Clock Low: Hold
Clock High: Transparent

In order to create precise boundary points of state capture, Latches are NOT allowed in Synchronous designs

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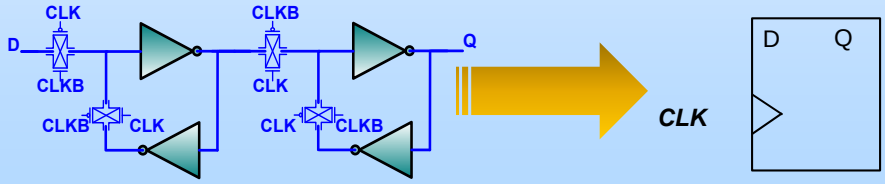
DFF SEU Generation (P_{DFFSEU})

- **DFF output is what affects the system circuit/behavior**
- **We will characterize DFF upset generation (P_{DFFSEU}) based on DFF output**
- **P_{DFFSEU} can affect the system differently depending on when and where the upset is actually generated**



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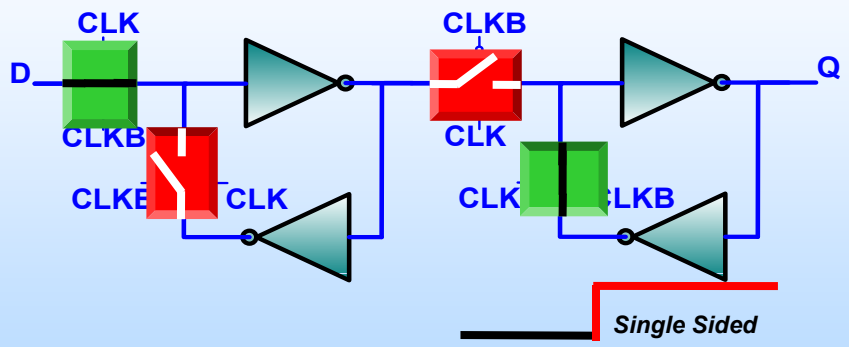
How is the DFF's Output Affected?... Clock Low

Clock low: Master is cut off from slave and an SEU can occur in the slave. Single sided upset at output



Output SEU occurs during the low portion of the clock period (intermediate state) – may not affect the system state because it needs to be captured into the next state

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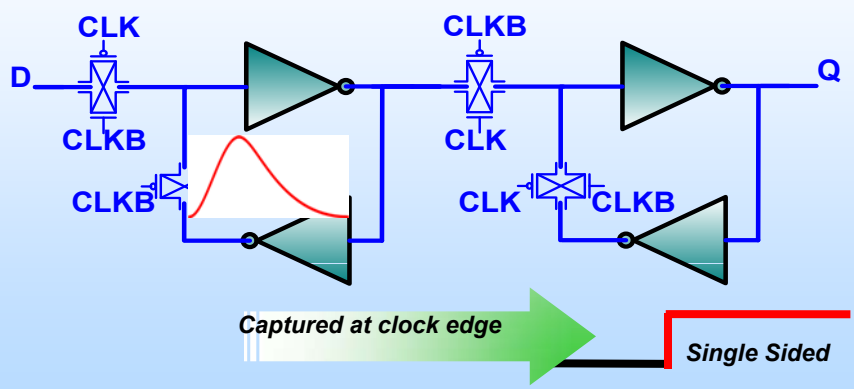
How is the DFF's Output Affected? Edge… Clock Low ➔ Clock High

Slave can capture an SET from Master. Single sided upset at output. Depends on the frequency, SET width, and the amount of circuitry in Master



Output changes at clock edge, hence it will affect the system state

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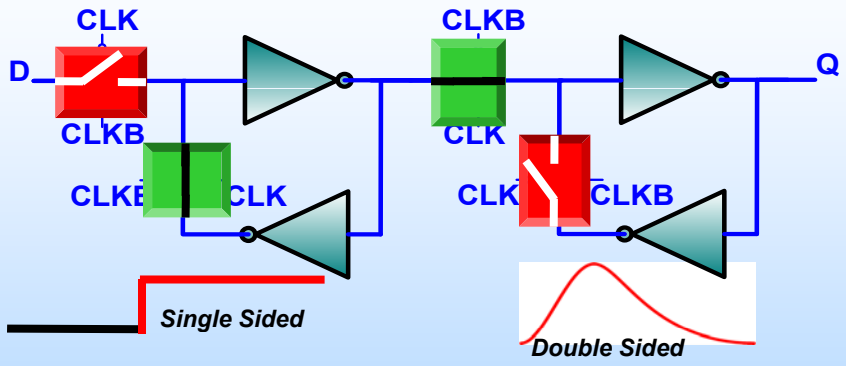
How is the DFF's Output Affected? Clock High

Master is cut off from slave and an SEU can occur in the slave. Single sided upset at output



One of the two can occur… both may not cause a system upset (intermediate state) …will need to be captured into the next state

- ***Output SEU occurs during the high portion of the clock period***
- ***Output SET occurs during the high portion of the clock period***

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DFF SEU Susceptibility

- **For simplicity, the traditional assumption that DFF upset generation is frequency independent will be used in this presentation**
- **However, it is apparent that DFF SEU susceptibility does have some frequency components:**
  - **Clock edge capture of Master SET.**
    - **Depends of the relation of SET width to clock frequency**
    - **higher frequency – higher probability for slave to capture SET from master**
  - **SET generation in the Slave… higher frequency – lower probability that the Slave will be in a state to generate an SET**

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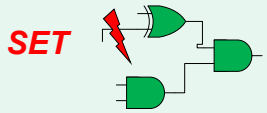
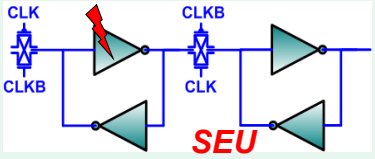
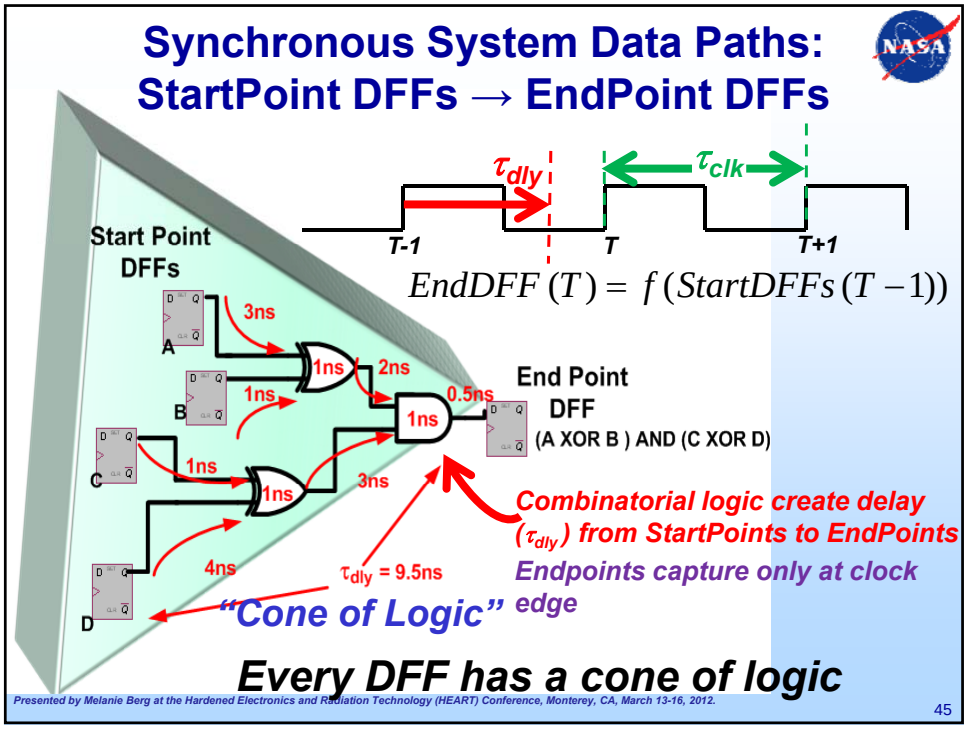
SEUs and SETs in a Data Path (Synchronous Designs)

Combinatorial (CL)	Sequential (DFF)
Logic function generation (computation)	Captures and holds state of data input at rising edge of clock
	
Glitch in the CL:	SET Capture in DFF loop

SEUs in Synchronous Systems

- We discussed SET generation and SEU generation
- For a synchronous system (design), the generation of an SET or SEU will not create an upset unless it is captured into the next state of the design
- We have discussed single sided versus double sided functions.
  - They propagate differently through a system
  - Their have opposing frequency responses with respect to system upsets
- We differentiate between SEU generation and system upsets

The question becomes, will the upset be missed or will it manifest… depends on design topology


Synchronous System Data Paths:
StartPoint DFFs → EndPoint DFFs
τ_{dly}
τ_{clk}
T-1
T
T+1
$EndDFF(T) = f(StartDFFs(T-1))$
Start Point DFFs
A
B
C
D
3ns
1ns
2ns
0.5ns
4ns
End Point DFF
(A XOR B) AND (C XOR D)
Combinatorial logic create delay (τ_{dly}) from StartPoints to EndPoints
Endpoints capture only at clock edge
τ_{dly} = 9.5ns
"Cone of Logic"
Every DFF has a cone of logic
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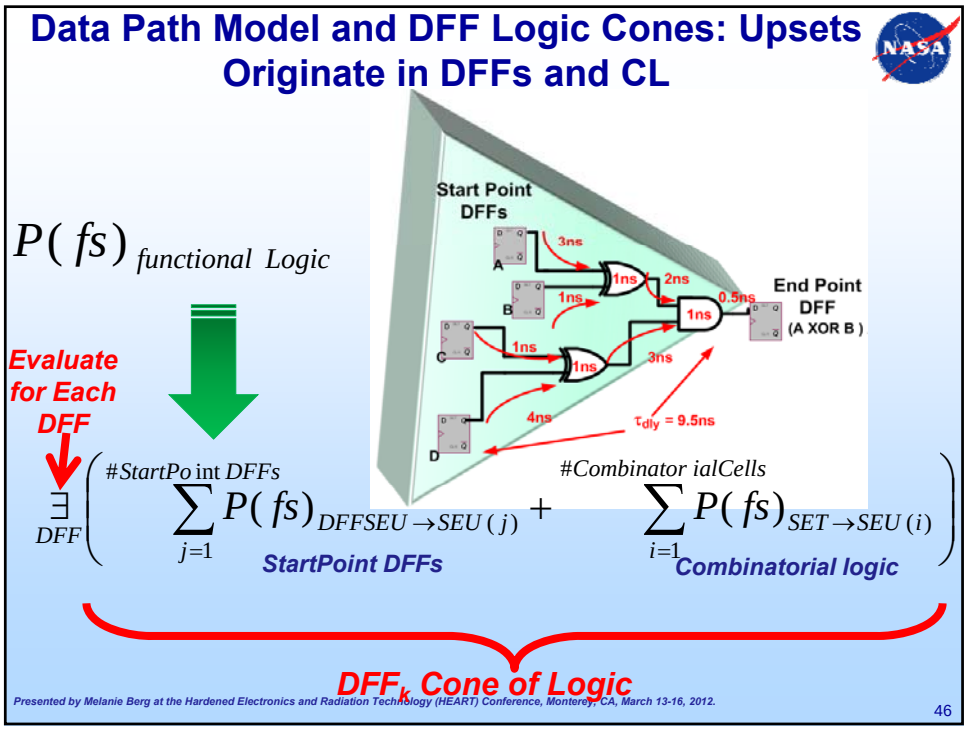
Data Path Model and DFF Logic Cones: Upsets Originate in DFFs and CL
$P(fs)_{functional\ Logic}$
Evaluate for Each DFF
$\exists_{DFF}\left(\sum_{j=1}^{\#StartPoint\ DFFs} P(fs)_{DFFSEU \to SEU(j)} + \sum_{i=1}^{\#Combinatorial\ Cells} P(fs)_{SET \to SEU(i)}\right)$
StartPoint DFFs
Combinatorial logic
DFF_k Cone of Logic
Start Point DFFs
End Point DFF
(A XOR B)
τ_{dly} = 9.5ns
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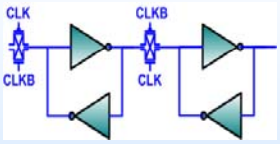
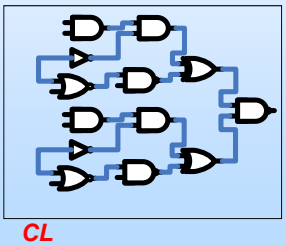
NASA REAG FPGA SEU Model Data Path Components

- **StartPoint DFF SEU Capture $P(fs)_{DFFSEU \rightarrow SEU}$:**
  - **SEU Generation in DFF (P_{DFFSEU})**
  - **Logic Masking (P_{logic})**
  - **Capture: $(1-\tau_{dly}/\tau_{clk}) = (1-\tau_{dly} fs)$**



- **CL SET Capture $P(fs)_{SET \rightarrow SEU}$:**
  - **SET Generation (P_{gen})**
  - **SET Propagation strength (P_{prop})**
  - **Logic Masking (P_{logic})**
  - **Capture is proportional to the SET width (τ_{width}) and the clock period (τ_{clk}): $\tau_{width}/\tau_{clk} = \tau_{width} fs$**



CL

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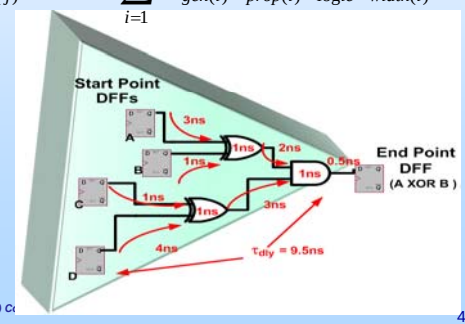
Putting it All Together: NASA REAG FPGA Data Path Susceptibility Model

$$P(fs)_{functionalLogic}$$

$$\exists_{DFF} \left(P(fs)_{DFFSEU \rightarrow SEU} + P(fs)_{SET \rightarrow SEU} \right)$$

$$\exists_{DFF} \left(\left(\sum_{j=1}^{\#StartPoint\,DFFs} P_{DFFSEU(j)} (1-\tau_{dly(j)} fs) P_{logic(j)} \right) + \sum_{i=1}^{\#CombinatorialCells} (P_{gen(i)} P_{prop(i)} P_{logic} \tau_{width(i)} fs) \right)$$



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Combinatorial Logic Susceptibility Formulation

$$\exists_{DFF}\left(\sum_{i=1}^{\#Combinator\,ialCells}(P_{gen(i)}P_{prop(i)}P_{logic}\tau_{width(i)}fs)\right)$$

Generation

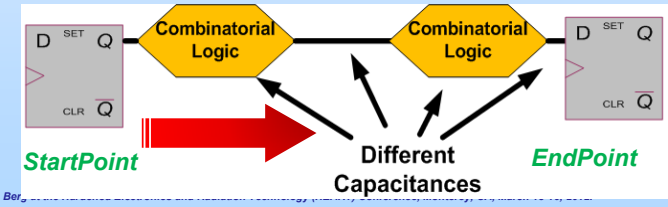
Propagation

Logic Masking

Capture

SET Propagation to an EndPoint DFF: P_{prop}

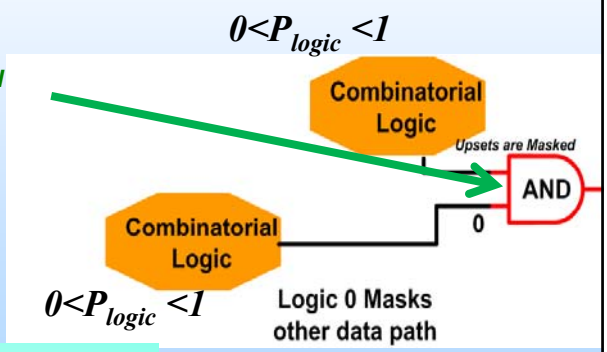
- In order for the data path SET to become an upset, it must propagate and be captured by its Endpoint DFF
- P_{prop} only pertains to electrical medium (capacitance of path… combinatorial logic and routing)
  - Capacitive SET amplitude reshaping
  - Capacitive SET width reshaping
- Small SETs or paths with high capacitance have low P_{prop}
- P_{prop} contributes to the non-linearity of $P(fs)_{SET \rightarrow SEU}$ because of the variation in path capacitance



SET Logic Masking: P_{logic}

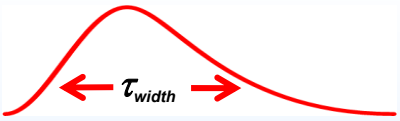
- P_{logic}: Probability that a SET can logically propagate through a cone of logic. Based on state of the combinatorial logic gates and their potential masking.

"AND" gate reduces probability that SET will logically propagate



Determining P_{logic} for a complex system can be very difficult

SET Capture at Destination DFF



The transient width (τ_{width}) will be a fraction of the clock period (τ_{clk}) for a synchronous design in a CMOS process.

$$P(\tau_{clk})_{SET \to SEU} \propto \frac{\tau_{width}}{\tau_{clk}}$$

$$P(fs)_{SET \to SEU} \propto \tau_{width} fs$$

Probability of capture is proportional to the width of the transient as seen from the destination DFF

Data Path Model and Combinatorial Logic SETs

$$\sum_{i=1}^{\#CombinatorialCells} P(fs)_{SET \to SEU(i)} \propto \sum_{i=1}^{\#CombinatorialCells} P_{gen(i)} P_{prop(i)} P_{logic(i)} \tau_{width(i)} fs$$

$$< \sum_{i=1}^{\#CombinatorialCells} P_{gen(i)} P_{prop(i)} \tau_{width(i)} fs$$

Upper Bound SET P_{logic}=1

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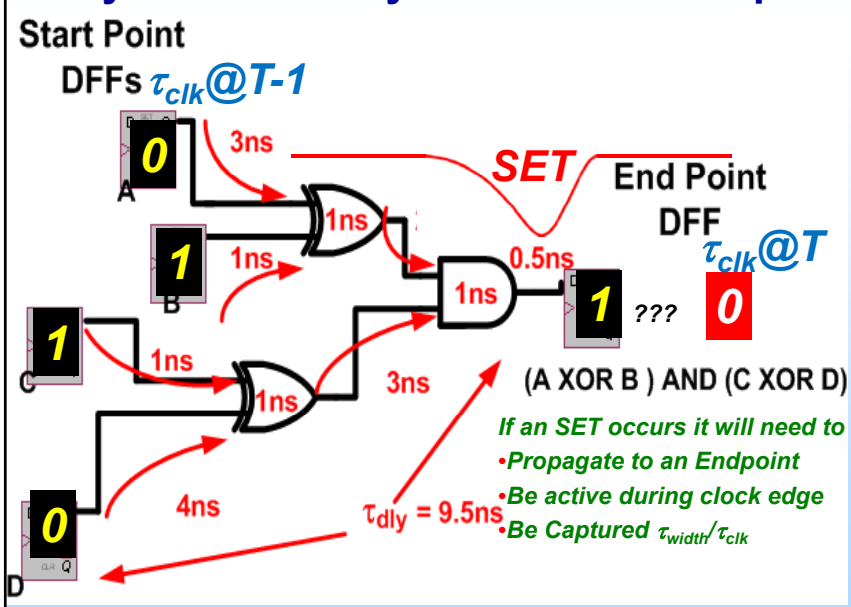
Synchronous System: CL SET Capture



If an SET occurs it will need to
- *Propagate to an Endpoint*
- *Be active during clock edge*
- *Be Captured τ_{width}/τ_{clk}*

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DFF Susceptibility Formulation

$$\exists_{DFF}\left(\left(\sum_{j=1}^{\#StartPoint\,DFFs} P_{DFFSEU(j)}(1-\tau_{dly(j)}fs)P_{logic(j)}\right)\right)$$

Generation

Capture

Logic Masking

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Generation P_{DFFSEU} versus Capture $P(fs)_{DFFSEU \rightarrow SEU}$

P_{DFFSEU}	$P(fs)_{DFFSEU \rightarrow SEU}$
Probability a StartPoint DFF becomes upset	Probability that the StartPoint upset is captured by the endpoint DFF
Occurs at some point in time within a clock period	Occurs at a clock edge (capture)
Not frequency dependent	Frequency dependent

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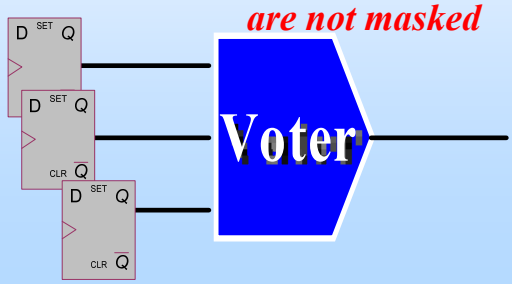
Logic Masking DFFs… P_{logic}

- Logic masking for DFF StartPoints is similar to logic masking of combinatorial logic.
- DFF logic masking is generally the point where Triple Modular Redundancy (TMR) is inserted

P_{logic}>0 for Voter… its upsets are not masked

P_{logic}=0 for DFFs… their upsets are masked



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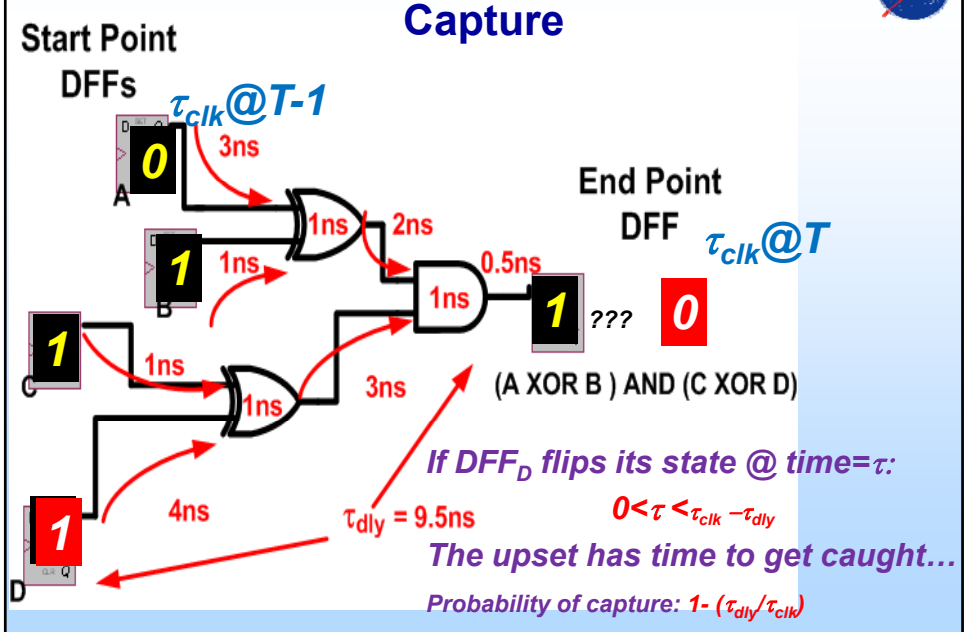
Synchronous System: StartPoint SEU Capture



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Percentage of Clock Cycle for SEU Capture:

$$\tau < \tau_{clk} - \tau_{dly}$$

Upset is caught within this timeframe

$$\frac{\tau}{\tau_{clk}} < \frac{\tau_{clk} - \tau_{dly}}{\tau_{clk}} = 1 - \frac{\tau_{dly}}{\tau_{clk}}$$

Fraction of clock period for upset capture

$$\tau \ fs < 1 - \tau_{dly} \ fs$$

upset capture with respect to to frequency

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Comparison of $P(fs)_{funtionalLogic}$ Components

$$\exists_{DFF}\left(\left(\sum_{j=1}^{\#StartPointDFFs} P_{DFFSEU(j)}(1-\tau_{dly(j)} fs) P_{\log ic(j)} \right) + \sum_{i=1}^{\#CombinatorialCells} (P_{gen(i)} P_{prop(i)} P_{\log ic} \tau_{width(i)} fs) \right)$$

	$P(fs)_{DFFSEU \to SEU}$	$P(fs)_{SET \to SEU}$
Logic	**StartPoint DFF Capture by EndPoint DFF**	**CL SET Capture by EndPoint DFF**
Capture percentage of τ_{clk}	$(1-\frac{\tau_{dly}}{\tau_{clk}}) = (1-\tau_{dly} fs)$	$\frac{\tau_{width}}{\tau_{clk}} = \tau_{width} fs$
Frequency Dependency	**As frequency increases, $P(fs)_{DFFSEU \to SEU}$ decreases**	**As frequency increases, $P(fs)_{SET \to SEU}$ Increases**
CL Effects	**Increase CL increases τ_{dly} and decreases $P(fs)_{DFFSEU \to SEU}$**	**Increase in CL increases P_{gen} and increases $P(fs)_{SET \to SEU}$**

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Test Structure Development

Test Structure Development Considerations-1

Best Practice Consideration	Description of how complex real-design test structures violate best-practice considerations
Create a DUT design that has a large number of replicated logic structures in order to increase statistics.	Statistics are poor because there usually is not a significant amount of replication. In addition, trends for specific elements are not able to be clearly identified/established.

Test Structure Development Considerations-2

Best Practice Consideration	Description of how complex real-design test structures violate best-practice considerations
Create a DUT design that has a traversable state space that can be completed within one radiation test run	The state space of a complex design cannot be traversed within one radiation test run. Hence, a significant amount of circuitry and system states are not tested. The result is σ_{SEU}s that are uncharacteristic of the design.

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Test Structure Development Considerations-3

Best Practice Consideration	Description of how complex real-design test structures violate best-practice considerations
Create a DUT design such that logic masking is minimized or is controllable.	Unintentional logic masking can hide upsets that would normally cause system malfunction.

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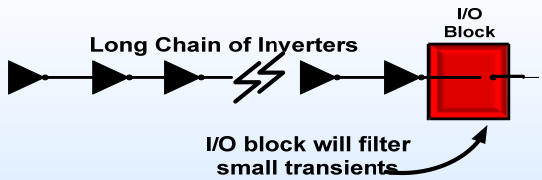
Test Structure Development Considerations-4

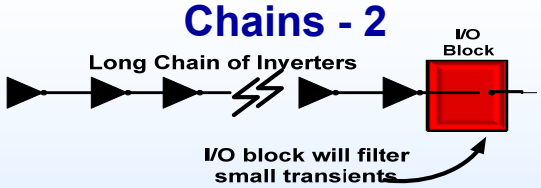
Best Practice Consideration	Description of how complex real-design test structures violate best-practice considerations
Create a DUT design such that all (or a significant percentage of) potential upsets are observable	A significant number of upsets in a complex design are generally not observable during radiation testing. This is true mostly because of logic masking, limitations in state space traversal, limitations in I/O count, or time of upset propagation to observable node.

Original Test Structures: SET Measurement with Long Inverter Chains - 1



- Small SETs can be attenuated as they propagate through the combinatorial logic chain.
- SET Attenuation will reduce visibility and hence result in inaccurate characterization.
- Topology matters: the test structure is not indicative of a synchronous design. Synchronous designs must include DFFs, combinatorial logic and clocks.

Original Test Structures: SET Measurement with Long Inverter Chains - 2



- SET error response is non-linear.
  - Determining the SET cross section for one inverter will not be1/N the SET cross section for N inverters.
  - The topology of the design will change capacitance, causes non-linear effects, and cannot be extrapolated from a long chain of inverters.
- I/O Block is slower than internal circuitry. Its cutoff frequency is lower and will filter small transients. Hence small SETs will be unobservable.

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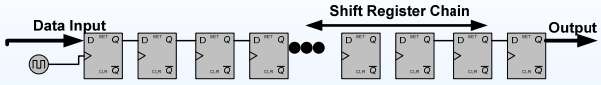
Original Test Structures: SEU Measurement with Long Shift Register (SR) Chains - Pros



- SRs are a reasonable method for measuring the susceptibility of DFFs because there is no logic masking.
- Simple architecture – state space is traversable
- Meets synchronous design requirements if each DFF is connected to a balance clock tree

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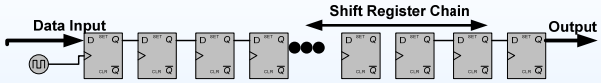
Original Test Structures: SEU Measurement with Long Shift Register (SR) Chains - Cons



- The architectural topology on an SR is too simple as compared to a real design.
- High frequency testing is complicated because the output will switch at high speeds. This can cause signal integrity issues on the
- Testing SRs with DFFs only at low frequencies can provide a fairly accurate characterization of the susceptibility of the DFFs. However, low frequency testing, alone, will not be efficient to characterize the susceptibility of the system.

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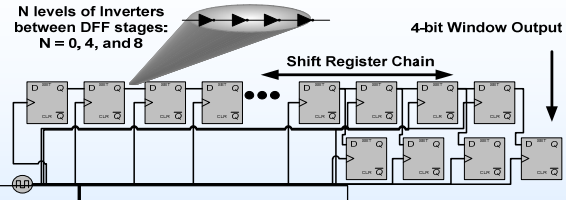
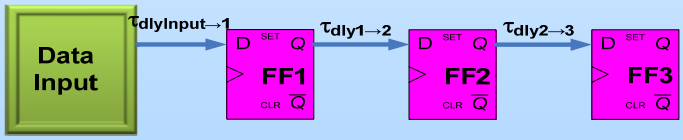
Evolution from Original Test Structures: Windowed Shift Registers (WSRs)

WSR_N:

N = levels of logic between DFFs



End-Point	Start-Point	Data Path Delays
FF3	FF2	$\tau_{dly2\rightarrow3}$
FF2	FF1	$\tau_{dly1\rightarrow2}$
FF1	Input	$\tau_{dlyInput\rightarrow1}$



Linear Cone of Logic

Maximum frequency of operation depends on the maximum τ_{dly}

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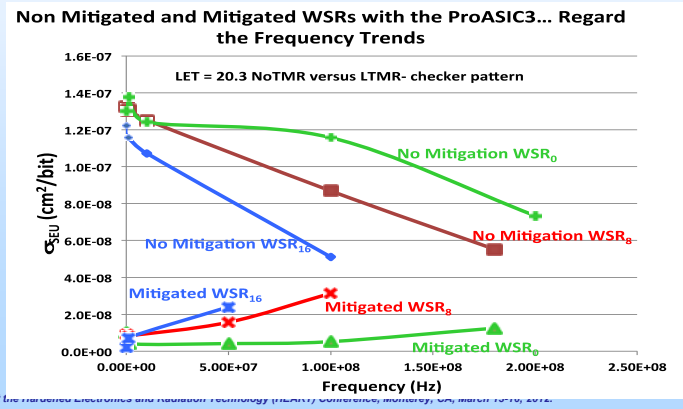
Impact of Frequency and τ_{dly} on System Level SEU Susceptibility - 1

- Depending on the FPGA's logic block structures, σ_{SEU}s may be frequency dependent. Subsequently, it is essential to evaluate σ_{SEU}s at a variety of frequencies to analyze trends.



Impact of Frequency and τ_{dly} on System Level SEU Susceptibility - 2

Based on the previous σ_{SEU}s Graph:

- Designs with well mitigated DFFs will produce σ_{SEU}s that are directly proportional to frequency
- Designs with poorly mitigated DFFs will produce σ_{SEU}s that are indirectly proportional to frequency
- σ_{SEU}s can differ by decades based on the frequency of operation during testing. Hence, for error rate calculations, it is essential to use σ_{SEU} data that was obtained using a similar frequency as the target design.

WSR Pros

- SRs with and without combinatorial logic between DFF stages are a reasonable method for measuring the susceptibility of DFFs because there is no logic masking.
- Simple architecture – state space is traversable
- Meets synchronous design requirements if each DFF is connected to a balance clock tree
- Because of windowing, high frequency testing can be performed without the SR causing signal integrity issues.
- All nodes are observable by the tester
- The inclusion of strings with combinatorial logic facilitates evaluation of combinatorial logic effects, i.e., SET capture
- Meets synchronous design requirements if each DFF is connected to a balanced clock tree

WSR Cons

- The WSRs with combinatorial logic between DFF stages have more complexity than purely sequential SR's, due to the addition of combinatorial logic. However, the cones-of-logic are still very simple compared to actual designs. Test structures with fan-in and fan-out should also be evaluated.

Considerations when Developing a Complex Design Test Methodology

- Design should contain Repeatability … increase statistics
- Stress building blocks…
  - Test Design should be stressed at highest frequency
  - Full state space traversal should be accomplished within one test run
- Fault Isolation…Create test designs that will facilitate error detection and differentiation
- Test design should have the characteristics of a complex design with:
  - Fan-Out and Fan-In > 1
  - contains a mixture of sequential and combinatorial logic.

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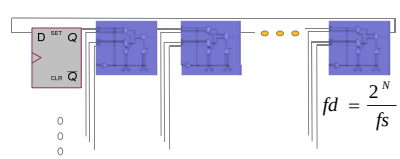
Evolution from Original Test Structures: Counters

- Has characteristics of a complex design with:
  - fan-out and fan-in > 1
  - contains a mixture of sequential and combinatorial logic.
- Variety of data pattern frequencies (f_d)
- State space Traversal = $2^N/f_s$
  - 24 bit counter takes 1.6777216×10^7 clock cycles
  - Less than 1 second state space traversal for 17MHz and above

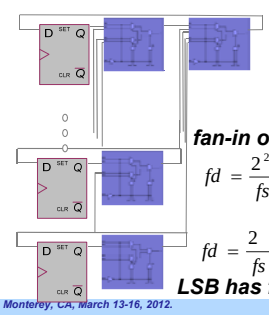
2 Bit Counter State Space Example:

0 0 → 0 1 → 1 0 → 1 1

MSB depends on all other bits: Largest fan-in



$$fd = \frac{2^N}{fs}$$



fan-in of two

$$fd = \frac{2^2}{fs}$$

$$fd = \frac{2}{fs}$$

LSB has fan-in of one

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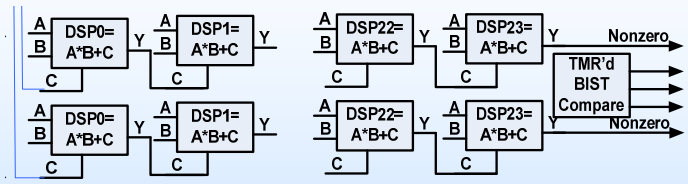
Evolution from Original Test Structures: Chains of Digital Signal Processing (DSP)



- **Example DSPs:**
  - **Multiply Accumulate Blocks**
  - **Blocks are Cascaded**
  - **Outputs are compared internally to the FPGA (BIST). BIST circuit is mitigated using Triple Modular Redundancy (TMR)**

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SEU test structures should include various levels of complexity with traversable state spaces: e.g., WSRs, Counters, DSPs, etc…

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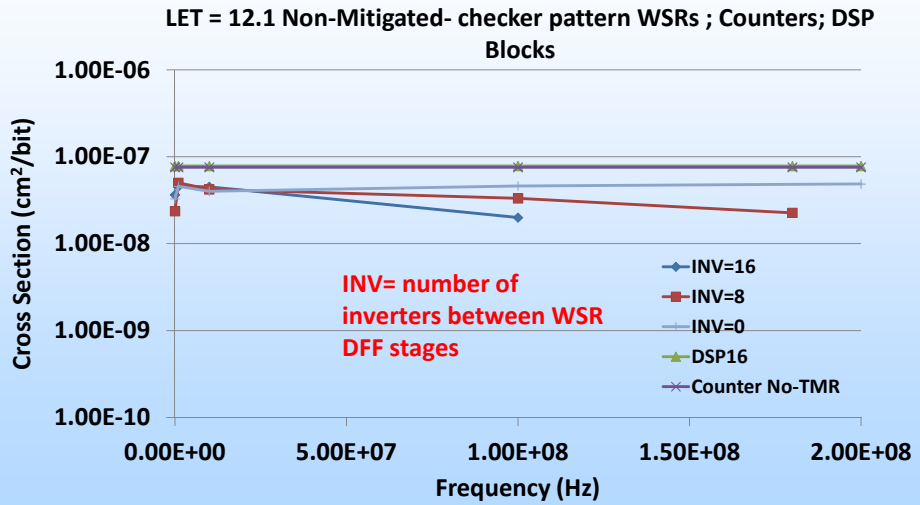
Benefits of Evaluating a Variety of Test Structures: Trend Analysis across Frequency



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Test and Analysis

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General SEU Testing Techniques

SEU Test Strategy

Different Technology

Configuration

- Static
- NOT performed for Anti-fuse FPGA
- Read Back SRAM or Flash

Functional Logic

- Generally dynamic testing is required
  - DFFs and Combinatorial
  - SEFIs: Global Routes (clocks and resets)
  - SEFIs: Custom internal circuitry
- Vary test structures and operational parameters for trend analysis

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Functional Data Path Heavy-Ion Testing

- Determine LET_{TH}: This is the lowest LET value where upsets are first observed. This is the most difficult goal to achieve. It will depend on:
  - Test structure: is there enough complexity of the test structure to observe upsets are small LETs? Or, is there too much complexity in the test structure where upsets are being masked and are unobservable?
  - Frequency: Regarding SETs, is the testing frequency fast enough to capture upsets? Regarding FF SEUs, is the frequency slow enough to observe upsets.
  - Data pattern: It has been shown that data paths that switch state every clock cycle are the most susceptible. Is the data pattern significantly switching states?
  - Test Vehicle: Does the test vehicle have enough granularity to capture all upsets?

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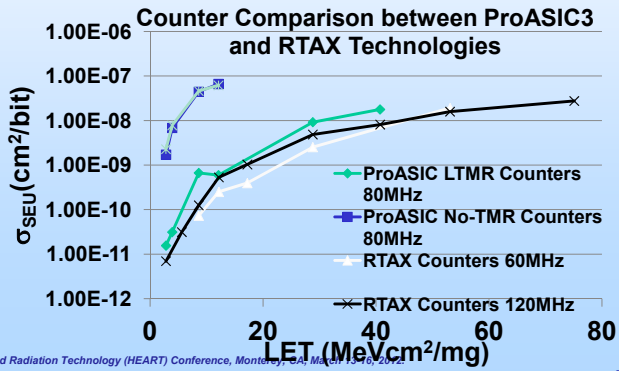
Functional Data Path Heavy-Ion Testing - 2

- Calculate σ_{SEU}s for at least 5 LET points. For a proper Weibull fit, it is best to have as many σ_{SEU}-LET data points as test time permits
- Determine the LET saturation (LET_{sat}) point. As technology shrinks, LET_{sat} is not observable.



Evaluating Trends: σ_{SEU}s are Dominated by DFF Upsets

- $P(fs)_{DFFSEU \rightarrow SEU}$ Dominance – Most SEUs stem from Captured Start-point DFFs. If there is an increase in the number of combinatorial logic blocks or τ_{dly} and the σ_{SEU} decreases in response
  - If there is an increase in frequency and the σ_{SEU} decreases in response
  - If there is an increase in frequency and the σ_{SEU} decreases in response
- Evaluate σ_{SEU}s across frequency and vary complexity

Evaluating Trends: σ_{SEU}s are Dominated by Combinatorial Logic Upsets

- ***P(fs)***$_{SET \rightarrow SEU}$ **Dominance – Most SEUs stem from Captured Combinatorial Logic SETs:**
  - **If there is an increase in frequency and σ_{SEU}s (increases in response**
  - **If there is an increase in combinatorial logic and σ_{SEU}s increases in response**
- **Evaluate σ_{SEU}s across frequency and vary complexity**
-

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Data Analysis

- **Differentiate upsets:**
  - **Configuration**
  - **Functional logic data-path**
    - **Determine dominant upsets (e.g. DFFs, combinatorial logic, or global routes)**
    - **Evaluate data trends per complexity, frequency, and data pattern**
  - **SEFIs**
- **Calculate σ_{SEU}s depending on upset type**
- **Calculate associated upset rates (i.e. integrate across LET)**

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Summary

- NASA Goddard Radiation Effects and Analysis Group has developed a new test methodology to enhance FPGA SEU characterization
- From this testing:
  - Lower LET thresholds have been observed
  - Fault isolation has been achieved
  - Enhanced SEU predication rates have been established
- Benefit of new test schemes include versatility – they can be implemented in all FPGAs and serve as effective test bench comparison points

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