NASA Electronic Parts and Packaging Program

Part II: Evaluation of Multilayer Ceramic Capacitors with C0G Dielectric and Base-Metal Electrodes

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Abstract

A commercial multilayer ceramic capacitor with base-metal electrode (BME) and a $CaZrO_3$-based C0G dielectric was evaluated for potential space-level applications. The product showed superior microstructure and reliability performance when tested under the MIL-PRF-123 requirements for space-level capacitors.

When examined with a scanning electron microscope (SEM), all BME capacitors with a $CaZrO_3$-based C0G dielectric in this study revealed a near-perfect microstructure for ceramic material, i.e., a dense and uniform grain structure with straight grain boundaries. No structural defects such as cracks, delamination, or voids were observed, indicating an excellent processing compatibility between the $CaZrO_3$ dielectric material and the base metal nickel electrodes.

No dielectric wearout failures were generated when the capacitors were tested under highly accelerating stress conditions of temperature and applied voltage as high as 200°C and 600V for a group of 50V C0G BME capacitors. A 4000-hour life test at 125°C and twice the rated voltage did not result in any failures. The insulating resistance measurement for all capacitor units under life test was more than 10 times greater than the MIL-PRF-123 requirements, both at room temperature and at 125°C.

Surge step stress testing (SSST) has resulted in failures of all parts. However, the lowest measured SSST breakdown voltage is at least 20 times higher than the rated voltage.

This ceramic capacitor is an excellent example for revealing the importance of structure-property relations and for showing that superior performance is always attributed to ideal microstructures.

The low-cost, commercially available BME capacitor with a $CaZrO_3$-based C0G dielectric is one of a few existing commercial products that can significantly exceed the NASA requirements for high-reliability space applications and can be directly recommended for use in NASA flight projects.

Acknowledgements

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1. Introduction

Many electronic circuit applications require capacitance to be precisely stable over a wide temperature range, with low dielectric losses or low acoustic noise. These applications include digital tuning and high-fidelity audio devices. The high-capacitance multilayer ceramic capacitors (MLCCs) with a C0G dielectric and base-metal electrode (BME is typically nickel) are good candidates for these applications.

The Electronic Industries Alliance (EIA) specification for C0G dielectrics, also known as NP0 ("negative-positive-zero"), is that the capacitance variation from room temperature (25°C) should be within 0 ±30 ppm/°C (or $\Delta C_{Max}/C \leq 0.3\%$) over the temperature range of -55°C to 125°C. The C0G dielectrics are usually non-ferroelectric materials that exhibit a linear response to voltage and temperature. Compared with Class-II dielectrics, typically X7R/X5R materials, C0G dielectrics have the advantages of high stability of capacitance over temperature, frequency, and voltage, and they have no aging, no "Piezo effort," as well as a low dielectric loss.

Traditionally, the maximum capacitance values of many ceramic capacitors with C0G dielectrics have been limited due to thick dielectric layers and to high costs due to the use of precious-metal electrodes (PMEs are typically Pd or Ag/Pd). The industrial efforts to replace expensive PMEs with cheap BMEs and the use of thinner dielectric layers allow ceramic C0G dielectric capacitors to exhibit capacitances that are competitive with PME capacitors that have high dielectric constant X7R dielectrics over a range of case sizes and voltages [1].

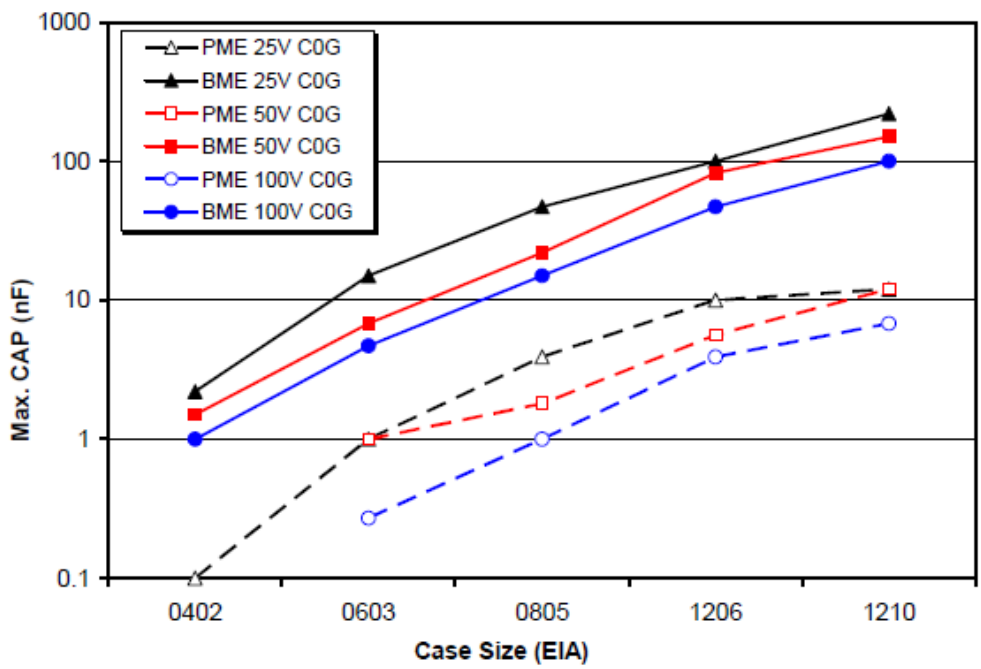


Figure 1. PME C0G vs. BME C0G: maximum capacitance offering.

A comparison of the maximum capacitance offering for BME C0Gs with PME C0Gs by case size is shown in Figure 1. Three voltage ratings (25V, 50V, and 100V) are compared. It is clear that a BME C0G can offer at least an order of magnitude higher capacitance than a PME C0G in the same case size and same voltage rating. For example, for the $25V_{DC}$-rated 1206 case size, the maximum capacitance offering of a BME C0G is 100 nF, while a PME C0G can only offer 10 nF capacitance. This plot also indicates that at the same capacitance and same voltage rating, a BME C0G MLCC has a much smaller case size than a PME C0G MLCC.

2. Microstructure Characterization of C0G BME Capacitors

A group of commercial BME capacitors with C0G dielectrics from manufacturer K were selected for this evaluation.

Table I summarizes the capacitor information on four chip sizes with the same rated voltage. The parts were cross-section processed and examined with SEM for microstructure characterizations.

Table I. Part Information for BME Capacitors with C0G Dielectrics

EIA SIZE CODE	Part Number	Capacitance (pF)	Rated Voltage (V)
0402	K04C10210	1,000	10.0
0603	K06C56210	5,600	10.0
0805	K08C10310	10,000	10.0
1206	K12C27310	27,000	10.0

Figure 2 shows cross-section SEM images of all four BME capacitor samples listed in Table I. The typical dielectric thickness of each part number was also labeled. Unlike most BME capacitors with a $BaTiO_3$-based X7R dielectric, the dielectric thickness of the BME capacitors with C0G dielectrics did not change much with increasing capacitor chip size. A discussion with the manufacturer revealed that this C0G dielectric material is non-ferroelectric and is not formed with a high insulating grain surface region. Indeed, the formulation is highly insulating, and the dielectric properties did not change much with dielectric thickness. As a result of that, the proper dielectric thickness was determined with the largest chip size in the group, i.e., 2022. When the product was qualified to meet all requirements, similar dielectric thickness casting tapes were used with all other smaller chip sizes. For commercial product development, this is clearly a cost-effective approach for manufacturers [7].

Traditionally, C0G dielectric materials for precious-metal electrodes are based on barium neodymium titanate (BNT). However, with the conversion from PMEs to BMEs in the MLCC industry in order to remain cost competitive, the BME C0G dielectrics used today are mainly $CaZrO_3$-based materials. Compared with PME C0G dielectrics, these BME C0G dielectric systems have the additional benefit of offering much higher insulation resistance and better

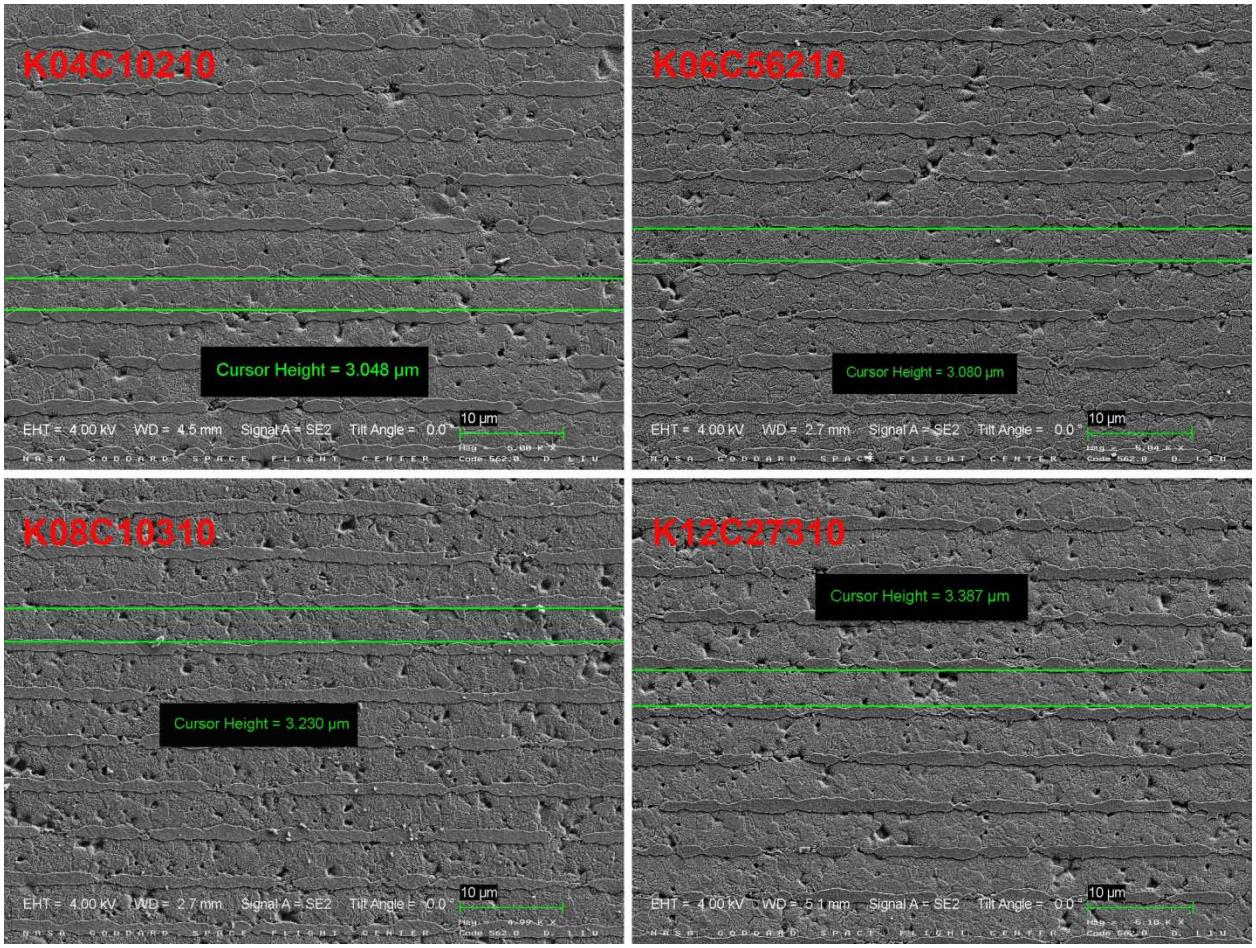


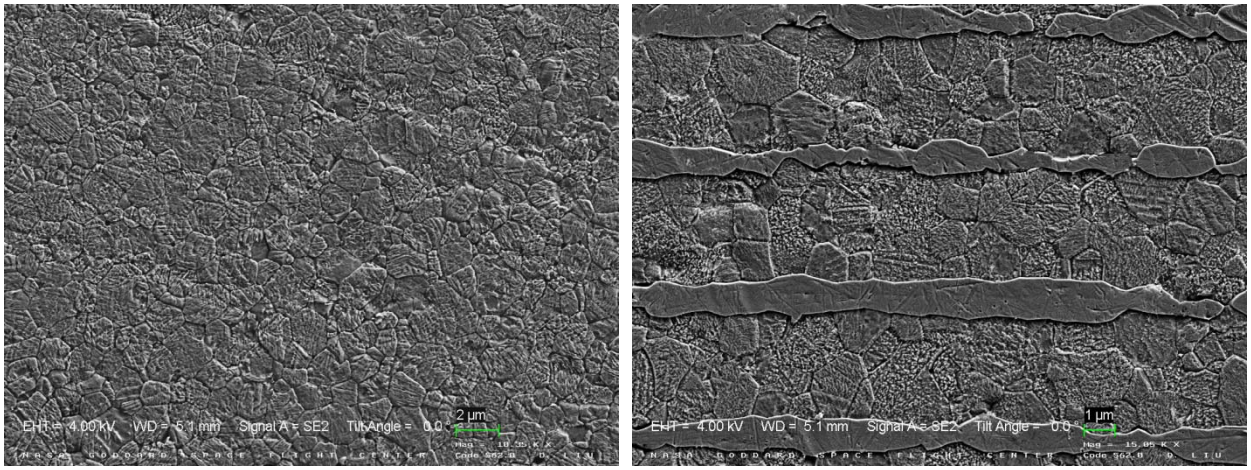
Figure 2. Cross-section SEM images of BME capacitors with C0G dielectrics reveal uniform electric layers and show that the average dielectric thickness did not change much with respect to the capacitor chip size.

reliability (HALT and life test bases), and higher quality factor (Q) even with much thinner dielectric layers [2].

All BME capacitors with C0G dielectric material were processed for the fabrication of BME capacitors as following: High purity powders of nominal formulation $(Ca_{0.7}Sr_{0.3})$ $(Zr_{0.97}Ti_{0.03})O_3$ were used with an average particle size of 0.7µm. The dielectric slips were prepared for tape-casting by milling the above powders in water for 16 hours. The slips were tape-cast into green sheets of equal thickness, which were used to build MLCCs with Ni electrodes. After burning out the organics with a manufacturer's proprietary profile, the samples were sintered at 1350°C for 3 hours with oxygen partially pressure controlled within the range of 10^{-9} to 10^{-12} atm, followed by re-oxidization in a weakly oxidizing atmosphere.

Figure 3 shows an SEM image of the microstructure for a BME capacitor with a C0G dielectric. This microstructure is typical for most $CaZrO_3$-based C0G dielectric materials studied in this report. The average sintered grain size is ~1.5-1.8 µm, which is significantly less than that in

traditional PME capacitors. There are 2-4 grains per dielectric layer. The microstructure shown in Figure 2 is dense and uniform, with typical straight grain boundaries.



(a) (b)

Figure 3. Typical microstructures of BME capacitors with $CaZrO_3$-based C0G dielectric materials: (a) Planar view of a dielectric area, and (b) a cross-section view of the electrode stacking area.

All of these features meet the criteria for excellent microstructure characteristics of a sintered ceramic material [3]. This clearly indicates that the $CaZrO_3$-based C0G dielectric material is more processing-compatible for the fabrication of MLCCs using BME technology.

Table II summarizes the construction and microstructure characteristics of BME capacitors. All of the parameters listed in Table II are according to the definitions in EIA-469.

Table II. Construction and Microstructure Characteristics of BME Capacitors

Part Number	Dielectric Thickness (μm)	Number of Dielectric Layers	Cover Plate (μm)	Side Margin (μm)	End Margin (μm)
K04C10210	3.05	70	70	155	80
K06C56210	3.08	102	170	130	130
K08C10310	3.23	98	150	150	150
K12C27310	3.39	112	103	185	210

3. Highly Accelerating Life Testing of C0G BME Capacitors

When evaluating the reliability of ceramic capacitors, highly accelerating life testing (HALT) has been a common method to choose. HALT tests electrical parts under stresses normally higher than those of use-level. By determining the time-to-failure data from HALT, the reliability life of the devices can be determined [4-5].

For capacitors, the applied stresses are usually the voltage and temperature, and they are normally held constant during the testing. For a wide class of failure modes, the failure rate at one temperature T_1 is related to the failure rate at a second temperature T_2 by an Arrhenius relation:

$$A_T = \frac{Rate(T_1)}{Rate(T_2)} = e^{-\left(E_S/k_B\right)\left(\frac{1}{T_1}-\frac{1}{T_2}\right)} \tag{1}$$

where A_T is the temperature acceleration factor, E_S is an activation energy, $k_B$is the Boltzman constant, and the temperatures are measured on an absolute scale.

Empirical work has often found that the applied voltage changes the failure rate following an inverse power law:

$$A_V = \frac{Rate(V_1)}{Rate(V_2)} = \left(\frac{V_2}{V_1}\right)^n \tag{2}$$

where A_V is the voltage acceleration factor and *n* is an empirical parameter. Prokopowicz and Vaskas have proposed that the rate of failure caused by a single failure mode when both *V* and *T* are changed is the product of the separate acceleration factors:

$$A_{VT} = \frac{Rate(T_1)}{Rate(T_2)} \cdot \frac{Rate(V_1)}{Rate(V_2)} = \left(\frac{V_2}{V_1}\right)^n \cdot e^{-(E_S/K_B)\left(\frac{1}{T_1}-\frac{1}{T_2}\right)}. \tag{3}$$

This is called a Prokopowicz and Vaskas equation (P-V equation) [8]. The P-V equation has proven useful in the capacitor industry for testing MLCCs at various test conditions. An average of n ~3 has generally been found for the voltage acceleration factor, and an average value of $1 < E_S < 2$ eV is typical for the temperature acceleration factor of ceramic capacitors.

When a *2*-parameter Weibull model is applied, the cumulative distribution function (CDF) that provides the probability of failure at time *t* is given by:

$$F(t) = 1 - e^{-\left(\frac{t}{\eta}\right)^{\beta}} \tag{4}$$

where *t* the failure time, slope β is the dimensionless shape parameter whose value is often characteristic of the particular failure mode under study, and η is the scale parameter that represents the point at which 63.2% of the population has failed and that is related to all other characteristic times, such as mean time-to-failure (MTTF):

$$MTTF = \eta\Gamma(1 + 1/\beta), \tag{5}$$

where $\Gamma(x)$ is the gamma function of x. (Note, for example, that $\Gamma(1+1/\beta)$ ranges from 0.887 to 0.900 as β ranges from 2.5 to 3.5.)

When both A_V and A_T are combined for HALT, the Weibull distribution scale parameter η can be expressed as:

$$\eta(V,T) = \frac{C}{V^n} \cdot e^{\left(\frac{B}{T}\right)} \tag{6}$$

where C and $B = E_S/k_B$ are constants. When Eqs. (4), (5), and (6) are combined, the cumulative distribution function $F(t)$ and $MTTF$ can be expressed as:

$$F(t) = 1 - e^{-\left(\frac{t \cdot V^n e^{-\left(\frac{B}{T}\right)}}{C}\right)^{\beta}} \tag{7}$$

and

$$MTTF = \frac{C}{V^n} \cdot e^{(B/T)} \Gamma(1 + 1/\beta). \tag{8}$$

By taking advantage of the maximum likelihood estimation method, reliability and accelerating parameters B, β, C, and n in Eq. (7) can all be determined.

In order to realize the proposed HALT scenario described above, the testing system shown in Figure 4 was constructed using the National Instrument PXI approach. The system has a potential testing capability of 200 channels (200 capacitors can be tested at the same time). Among them, 60 channels have been wired up and programmed for in-situ monitoring and recording of the leakage current as a function of stress time. The system can be operated at stress levels as high as 200°C for temperature and 600V for applied voltage.

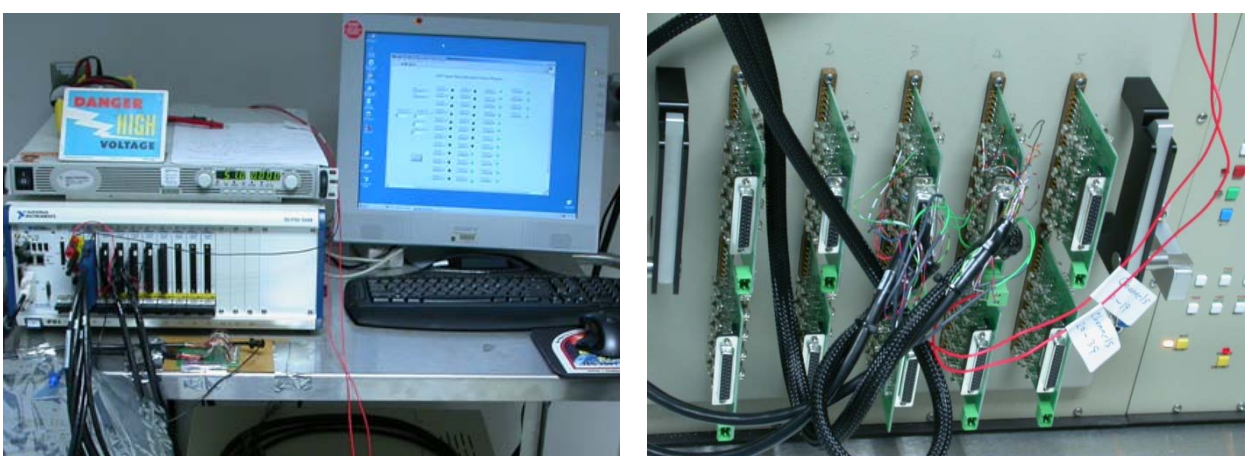


Figure 4. Illustration of testing setup for highly accelerated life test of BME capacitors.

Two groups of C0G BME capacitors, as shown in Table I (K08C10310, K12C27310), were used for HALT. However, no failures were generated at 165°C and 300V for 48 hours. That voltage is 30 times the rated voltage of BME capacitors. There is no need to further increase the accelerating stress levels since it is too high to reveal the failure modes that could exist at use-level (room temperature, rated voltage, i.e., 10V). As an alternative, another group of C0G BME capacitors with a 50V rating was stress accelerated to 200°C and 600V. No failures were generated.

These HALT results clearly indicate that the BME capacitors with $CaZrO_3$-based C0G dielectric material are so robust that no failures could be generated under regular HALT conditions. Alternative testing approaches are to be explored.

4. Life Testing of C0G BME Capacitors

Selected BME C0G capacitors were also evaluated per MIL-PRF-123 for life testing at 125°C and twice the rated voltage for 4000 hours. Two groups of BME capacitors in Table I (K08C10310 and K12C27310) were mounted and life tested. All capacitor samples passed the 4000-hour life test without a single failure. In addition, no observable capacitance or insulating resistance (IR) degradation was revealed. Figure 5 shows the IR measurement at both 125°C and 25°C. The measured IR data are at least one magnitude higher than that specified in MIL-PRF-123, paragraph 3.23. Both capacitance and dielectric loss met the requirements as well.

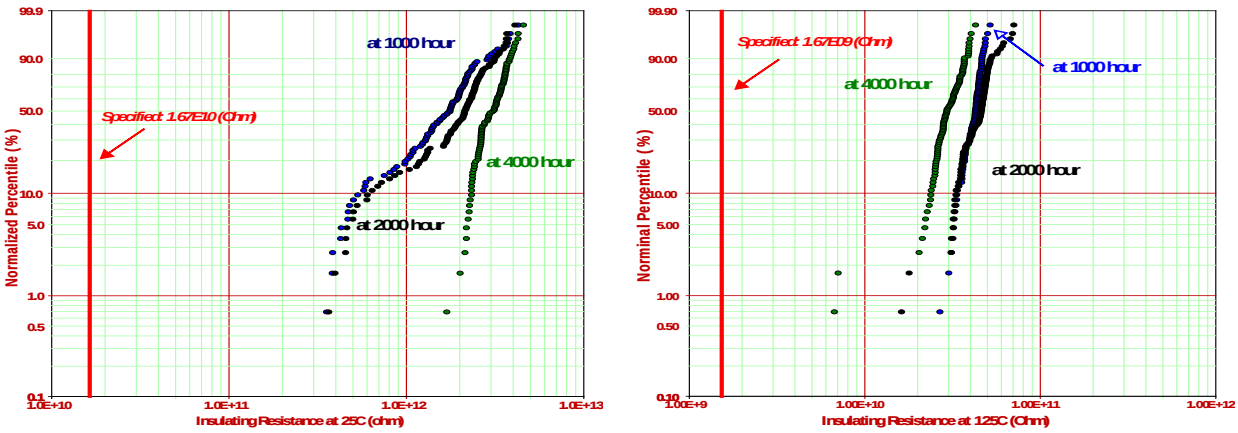


Figure 5. Measured insulating resistance (IR) at both 125°C (left) and 25°C (right) were at least 10 times greater than that specified in MIL-PRF-123, paragraph 3.23.

5. Surge Step Stress Testing of C0G BME capacitors

Ceramic capacitors with a $CaZrO_3$-based C0G dielectric have thus far revealed excellent performance under voltage and temperature stresses. In a highly accelerating life test, with the accelerating voltage as high as 30 times the rated voltage, the temperature at 165°C, and with 48 hours of testing, no failures due to dielectric wearout were revealed. Since these accelerating

parameters are way above use-level stress, the capacitors usually do not have dielectric wearout failures.

As an alternative, it is interesting to reveal the failures under an overstressed condition. Surge step stress testing (SSST) is one of the overstress tests that may generate an adequate number of failures at reasonably low stress levels. A detail description of SSST testing of various capacitors has been given previously [6].

The initial SSST of 10V ceramic capacitors with C0G dielectrics did not reveal any failures; SSST voltage was around $290V_{DC}$. Modifications of SSST for these C0G capacitors are proposed in order to generate overstress failures.

1. Test Samples: 4 groups of test samples were assembled, with 60 pieces per group. The BME capacitors used for SSST are listed in Table I. They are all rated at 10V.
2. Modification of Capacitor Bank: The SSST setup uses a number of 6800µF capacitors with a 250V rating. In order to increase the voltage rating, 3 capacitors can be connected in SERIES so that the rated voltage will be increased from 250V to 750V. Since most of the ceramic capacitors under test are very small in capacitance, the series connection of the bank capacitors will still have more than 20-50 times the capacitance of the DUTs.
3. Modification of DC Power Supply: Two DC power supplies were connected in SERIES in order to increase the surge voltage capability. An Agilent N5771A (300V/5A) was pre-set at 200V to begin as the initial voltage. The second DC power supply, the Sorenson XFR 300-9 (300V/9A), will be programmed to ramp up from 0V to 290V.

According to the circuit setup described above, all BME capacitors underwent SSST under "underdamped" conditions. Figure 6 shows a typical surge voltage profile during the SSST; it confirms the underdamped testing conditions.

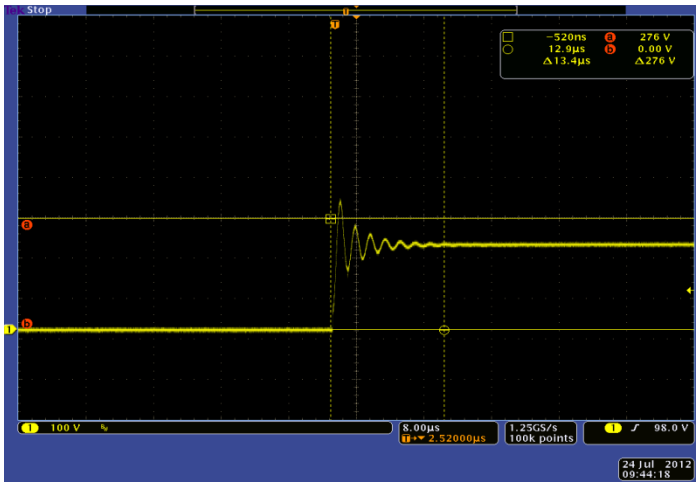


Figure 6. A typical transient voltage waveform under an underdamped test condition. The transient time is typically in the microsecond range.

Figure 7 demonstrates how the SSST breakdown voltage (V_{br}) was determined when testing under ramp-up SSST voltages. In general, the SSST voltage of a BME capacitor will increase linearly with the increase of applied SSST voltage. After a peak voltage value is reached, the SSST voltage on a capacitor will drop quickly. The V_{br} was the peak SSST voltage observed during the SSST voltage ramp-up.

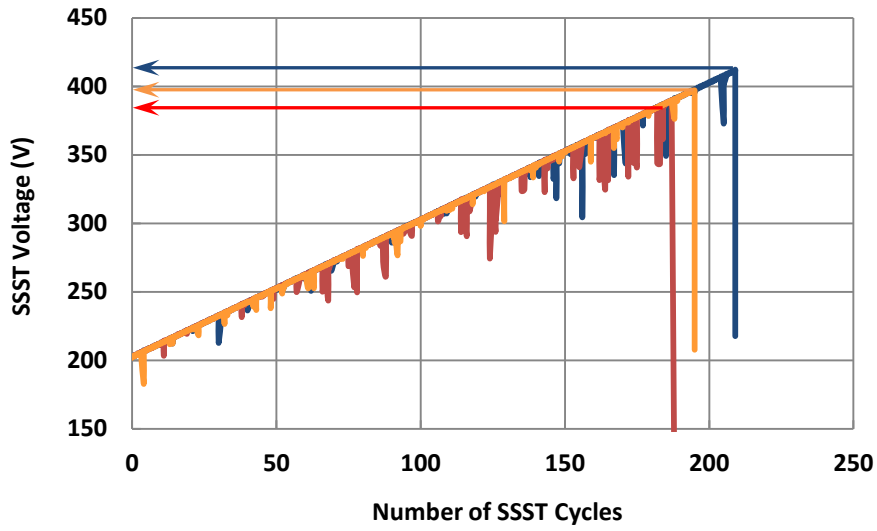


Figure 7. Illustration of the determination of SSST breakdown voltage (V_{br}) as a function of SSST voltage. The SSST voltage for three BME capacitor samples is plotted.

A Weibull plot of cumulative failure percentiles as a function of SSST breakdown voltage is shown in Figure 8. The majority of V_{br} is above 400V for these 10V-rated capacitors. A number of outliers with lower V_{br} were also revealed.

These low breakdown data points are attributed to the quality of the testing circuit boards on which all of the BME capacitors were mounted. Due to funding limitations, only the existing PCB cards that were designed for regular life testing up to 300V were used for the SSST since it was not expected that more than 400V would need to be used in order to break these BME capacitors. The author believes that with better-designed and fabricated high-voltage boards, the SSST breakdown voltage results would be more consistent. However, even with the existence of the low breakdown voltage outliers, the minimum V_{br} is still more than 200V, which is 20 times the rated voltage of these BME capacitors.

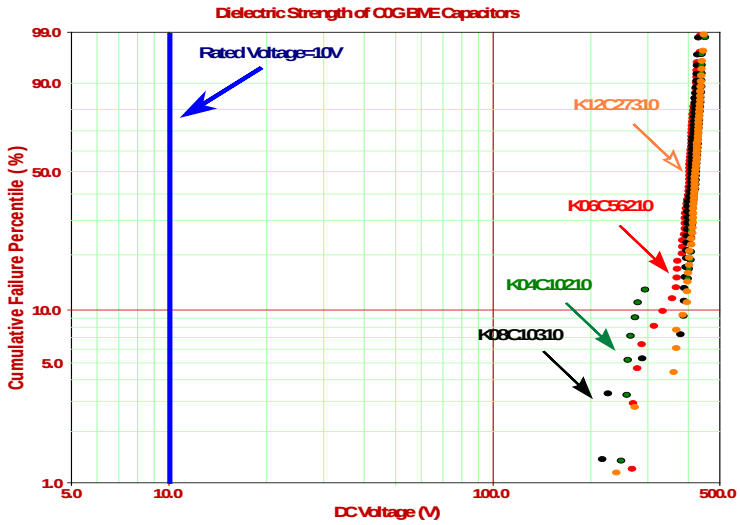


Figure 8. Weibull plot of SSST data of breakdown voltage V_{br} for all 4 groups of BME capacitors with C0G dielectric.

Weibull probability distribution function (PDF) plots of the four groups of BME capacitors are shown in Figure 9. All four groups of capacitors had similar distributions, and their PDF peaks are close to each other. Since the average dielectric thicknesses shown in Figure 2 did not change much with respect to chip size, a combination of dielectric thickness and PDF peaks can be used to approximate the dielectric strength of the $CaZrO_3$-based C0G dielectric. Taking an average dielectric layer thickness of 3.2 μm for all four groups, and using the average SSST breakdown voltage of 415V (estimated from Figure 9), the average electrical strength for BME capacitors with C0G dielectrics is ~ 415/3.2 ≈130MV/m.

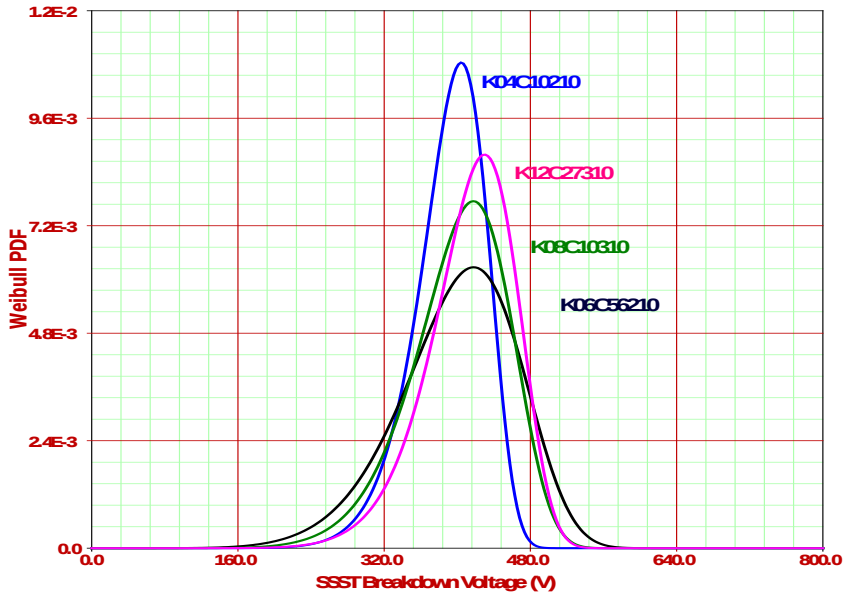


Figure 9. Weibull probability distribution function (PDF) plots of BME capacitors.

From the Weibull plot of SSST data shown in Figure 8, the SSST breakdown voltage at a failure rate of 100 parts per million (ppm), V_{br} *(100ppm)*, can be calculated and used to estimate the rated voltage de-rating. In general, if the calculated V_{br} *(100ppm)* is greater than the rated voltage V_{rated}, the capacitor operation voltage de-rating will not be required. If the value of V_{br} *(100ppm)* is less than the rated voltage, the capacitor operating voltage of a BME capacitor will be de-rated accordingly [1].

The calculated results of V_{br} *(100ppm)* for all of the BME capacitors listed in Table I are summarized in Table III. The results clearly show that the V_{br} *(100ppm)* for all BME capacitors was at least 10 times greater than the rated voltage, indicating an excellent surge voltage robustness!

Table III. Breakdown Voltage at 100 ppm Failure Rate [V_{br} *(100ppm)*]

Part Number	V_{br} *(100 ppm)*	V_{br} *(100 ppm)*/V_{rated}
K04C10210	188.64	18.86
K06C56210	118.76	11.88
K08C10310	149.66	14.97
K12C27310	177.84	17.78

6. Summary and Recommendations

A commercial MLCC with BME and a $CaZrO_3$-based C0G dielectric was evaluated for potential space-level applications. The product showed excellent performance when tested under the MIL-PRF-123 requirements for space-level capacitors:

1. All BME capacitors with $CaZrO_3$-based C0G dielectrics reveal a near-perfect microstructure characterized by a dense, uniform grain structure with straight grain boundaries. No structural defects such as cracks, delamination, or voids were observed, indicating an excellent processing compatibility between $CaZrO_3$ dielectric materials and nickel electrodes;
2. A 4000-hour life test did not reveal any failures. The insulating resistance measurement for all capacitor units under life test was more than 10 times greater than the MIL-PRF-123 requirement , both at room temperature and at 125°C;
3. No dielectric wearout failures were found when the capacitors were HALT tested under stress conditions as high as 200°C and 600V for a group of 50 C0G BME capacitors;
4. Testing under a SSST approach resulted in failure of all parts. However, the lowest measured DC breakdown voltage is at least 20 times greater than the rated voltage;
5. Due to the implementation of cheap base-metal electrode materials, BME capacitors are more than 50 times lower in cost than capacitors made with precious-metal electrodes.

This low-cost, commercially available BME capacitor with a $CaZrO_3$-based C0G dielectric is one of a few existing commercial products that can significantly exceed the NASA requirements

for high-reliability space applications and that can be directly recommended for use in NASA flight projects.

References

[1] P. Pinceloup, et al., 12th US-Japan Seminar on Dielectric and Piezoelectric Ceramics, Nov. 6-9, 2005, Annapolis, MD, p293-296.

[2] P. Pinceloup, M. Randall and A. Gurav, Proc. of CARTS USA 2006, April 3-6, 2006 Orlando, FL, p249-257.

[3] W. D. Kingery, Introduction to Ceramics, Wiley, 1960.

[4] D. Liu and M. Sampson, CARTS proceedings, New Orleans, LA, March 26-28, 2011, pp. 45-63.

[5] D. Liu and M. Sampson, CARTS proceedings, Jacksonville, FL, March 28-31, 2012, pp. 59-71.

[6] D. Liu, CARTS Proceedings, Jacksonville, FL, March 28-31, 2011, pp. 210-223.

[7] This information on the dielectric thickness against chip size was learned from a phone conversation with a processing engineer at KEMET in November, 2012.

[8] T. I. Prokopowicz and A. R. Vaskas, Final Report ECOM-90705-F, NTIS AD-864068, (Oct. 1969)