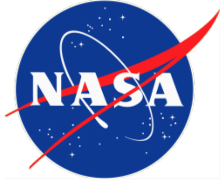

NASA Electronic Parts and Packaging Program

Selection, Qualification, Inspection, and Derating of Multilayer Ceramic Capacitors with Base-Metal Electrodes

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Selection, Qualification, Inspection, and Derating of Multilayer Ceramic Capacitors with Base-Metal Electrodes

1. Introduction

A multilayer ceramic capacitor (MLCC) is a high-temperature (1350°C typical) co-fired ceramic monolithic that is composed of many layers of alternately stacked oxide-based dielectric and internal metal electrodes. The internal electrodes are connected in parallel to form end terminations for the electrical contacts (Figure 1-1).

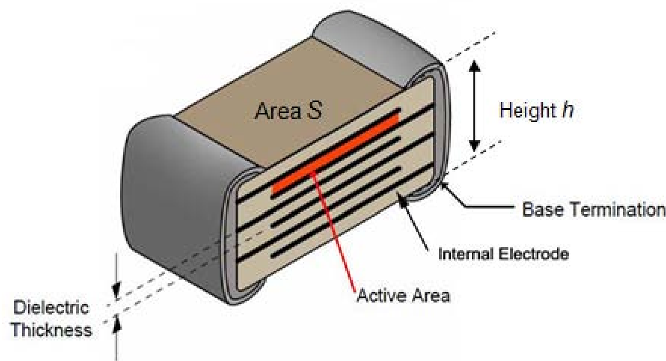

Figure 1-1. A typical structure of an MLCC device.

The capacitance C_t of an MLCC can be represented by:

$$C = \varepsilon_r \cdot \varepsilon_0 \cdot n \cdot \frac{S}{d}, \qquad (1\text{-}1)$$

where *S* is the overlap area of internal electrodes, *N* is the number of individual dielectric layers, ε_r is the relative dielectric constant of the ceramic dielectric, *d* is the thickness of the dielectric layer, and ε_0 is the dielectric constant of free space.

In order to make the dielectric layers insulating and the metal electrode layers conducting, only highly oxidation-resistant precious metals such as platinum, palladium, and silver can be used for the co-firing of insulating MLCCs in a regular air atmosphere. MLCCs made with precious metals as internal electrodes and terminations are called PME (precious-metal electrode) capacitors. To date, MIL-PRF-123 requires all MLCCs for high-reliability and space projects to be PME capacitors [1].

In the early 1990s, the high cost of precious metal materials, coupled with uncertainty about their availability, forced an industry shift from PME to base-metal electrode (Ni, Cu) technology (BME) for most commercial MLCCs. The switch from PMEs to BMEs required a change in the manner in which the ceramic is fired in a reducing atmosphere to prevent the oxidation of internal nickel electrodes. This creates a significant amount of oxygen vacancies in the dielectric that will migrate under DC bias and degrade the dielectric's insulating resistance. After more

than two decades of development, the insulating resistance degradation in BME MLCCs has been significantly reduced by two primary approaches [2-9]:

(1). A subsequent low-temperature firing in an oxygen-rich environment to re-oxidize the dielectric by occupying the oxygen vacancies.
(2). Rare-earth element doping to pin or slowdown the migration of still-existing oxygen vacancies.

Although there are always some issues and concerns with respect to the reliability life of MLCCs manufactured using BME technology, substantial progress has been made in the last 20 years. The performance and the reliability of some commercial BME capacitors have met the majority of the requirements for high-reliability space and military applications. The investigation of BME capacitors for possible high-reliability NASA space-level applications becomes urgent and inevitable due to the following considerations:

(1). Almost 99% of MLCCs fabricated today use BME technology, it is just a matter of time until high-reliability MLCCs users like NASA will face the transition from PME to BME, not only due to the smaller number of PME parts available and longer lead time, but also to the fact that some high-reliability modules and hybrid circuits are already fabricated with BME capacitors inside [10].
(2). Although the driving force to switch to BME capacitors is mainly the fabrication cost, the development of BME technology has resulted in significant progress in the performance and reliability of the capacitors, particularly the recently developed C0G BME capacitors with non-ferroelectric materials [11]. Since most R&D resources today are applied toward BME technology, continued progress is being made in improving the BME capacitor reliability and performance.

Another important parameter for measuring the degree of miniaturization of a capacitor is *volumetric efficiency*, which is the capacitance per volume and which can be expressed as:

$$\frac{C_t}{V} \approx \varepsilon_0 \frac{\varepsilon_r}{d^2} \approx 8.854 \times 10^{-8} \frac{\varepsilon_r}{d^2} \left(\frac{\mu F}{cm^3}\right) \tag{1-2}$$

where ε_r is the dielectric constant and d the dielectric thickness. MLCCs with high volumetric efficiency can be achieved by increasing the dielectric constant and reducing the dielectric thickness. Due to its improved voltage robustness and its capability for making more layers of internal electrodes, a BME capacitor can achieve equal or better lifetime reliability than PME capacitors, with much higher capacitance per volume and a much lower cost. This is another advantage to using BME capacitors for high-reliability, space-level applications.

However, the pursuit of high volumetric efficiency in commercial applications has pushed the technology envelope to its limit. Many commercial BME capacitors made today have dielectric layers less than 1 micrometer thick and have more than 500 layers of stacked internal electrodes. As a result, the lifetime reliability of these BME capacitors is reduced dramatically [12, 13]. Many ceramic capacitor manufacturers have to continuously reduce their qualification criteria in order to meet customers' demands for BME products with ever-higher levels of volumetric efficiency. This trend is clearly not desirable for high-reliability applications, and BME products made under such circumstances should be completely removed from consideration for space projects.

The purposes of this guideline document can be summarized as follows:

(1). To understand the reliability as a function of acceleration factors against applied voltage and ambient temperature, and of the macro- and micro-structure parameters.
(2). To develop viable and realistic production and qualification criteria in which all of the BME capacitors manufactured will meet the minimum high-reliability, space-level requirements and those produced only for high volumetric efficiency commercial applications will be eliminated.
(3). To provide specifications uniquely applicable to BME capacitors. General specifications for ceramic capacitors can be found in MIL-PRF-123.
(4). To follow the general vendor production flow for high-reliability ceramic capacitors.
(5). To understand voltage rating and derating in BME capacitors.

2. The Reliability of BME Capacitors

The reliability of a ceramic capacitor is generally determined by its microstructures. BME capacitors can't be qualified for high reliability; they have to be made for it. MIL-PRF-123, paragraph 3.4.1 provides a minimum dielectric thickness for high reliability PME capacitors. This minimum dielectric thickness requirement has ensured that most PME capacitors have been able to be used for high-reliability space-level applications for many years without major issues.

BME capacitors, however, have a different manufacturing process. For example, nickel electrodes have been found to be more compatible with and more adhesive to the dielectric layers, and the existence of oxygen vacancies has facilitated the sintering and densification of the dielectric materials. As a result, most BME capacitors have been shown to have more desirable microstructures than PME capacitors, with denser and more uniform ceramic grains, and smaller grain sizes. This means that most BME capacitors have greater voltage robustness than traditional PME capacitors. This also makes it possible for BME capacitors with much thinner dielectric layers to have a longer lifetime than PME capacitors. In addition, the improved processing technique in dielectric layer stacking allows the fabrication of BME capacitors with more than 1000 layers of internal electrodes (as compared with the typical 50 layers for PME capacitors) [14].

Unlike PME capacitors, a simple minimum dielectric layer thickness requirement is not sufficient for ensuring the high-reliability performance of BME capacitors. Fabrication requirements and a qualification plan must be developed for BME capacitors to help ensure that they will be suitable for high-reliability applications. This requires an in-depth look into the factors and parameters that will determine the reliability of BME capacitors.

2-1. Reliability of Multilayer Ceramic Capacitors

The reliability of an MLCC is the ability of the dielectric material to retain its insulating properties under stated environmental and operational conditions for a specified period of time *t*. A general expression of reliability consists of three parts and can be expressed as:

$$R(t) = \varphi(N, d, \bar{r}, S) \times AF(V, T) \times \gamma(t) \tag{2-1}$$

Where $\gamma(t)$ is a statistical distribution that describes the individual variation of properties in a testing group of samples (Weibull, log normal, normal, etc.).

$AF(V, T)$ is an acceleration function that describes how a capacitor's reliability responds to the external stresses such as applied voltage *V* and temperature *T*. All units in the testing group should follow the same acceleration function if they share the same failure mode (independent of individual units).

$\varphi(N, d, \bar{r}, S)$ describes the impacts on the reliability due to the structural and constructional characteristics of a capacitor device. For example, the dielectric thickness of BME MLCCs can vary from submicrons to more than 10 microns; the number of dielectric layers varies from less than 50 up to 1000! Such a broad variation in the structure of a BME capacitor may have a significant impact on the reliability of the capacitor and needs to be evaluated.

In general, a *2*-parameter Weibull statistical distribution model is often used in the description of a BME capacitor's reliability as a function of time:

$$\gamma(t) = e^{-(\frac{t}{\eta})^{\beta}} \qquad (2\text{-}2)$$

where e is the base for natural logarithms, β is the dimensionless *slope* parameter whose value is often characteristic of the particular failure mode under study, and η is the *scale* parameter that represents a characteristic time at which 63.2% of the population has failed and that is related to all other characteristic times, such as mean time to failure (MTTF):

$$MTTF = \eta\Gamma(1 + 1/\beta), \qquad (2\text{-}3)$$

where $\Gamma(x)$ is the gamma function of x (Note: $\Gamma(1+1/\beta) \approx 0.9$ when $\beta > 3.0$).

Eq. (2-2) provides a simple and clear understanding on the meaning of reliability:

(1). Reliability is a monotonic function of time and always decreases with time, which indicates that the loss of reliability is a common behavior for all devices.
(2). Since η and β always exceed zero, the value of $\gamma(t)$ is always between 0 and 1, indicating that reliability can also be viewed as the probability of a failure to occur.
(3). Reliability typically defines the durability of a system that can function normally. When $\beta > 3$ and $t < \eta$, $\gamma(t) \sim 1$, suggesting a reliable life span before η. When $t > \eta$, $\gamma(t)$ decreases rapidly to 0. The lifetime of a device to sustain its function can be characterized by η, as shown in Eq. (2-3).

2-2. Acceleration Function and Highly Accelerated Life Stress Testing (HALST) of BME Capacitors

$AF(V,T)$ in Eq. (2-1) represents the impacts of external stresses (applied voltage and temperature are commonly used) on the reliability of a BME capacitor. It is widely known that the failure rate for MLCCs that is caused by a single failure mode when both V and T are changed from V_1 to V_2 and T_1 to T_2 is the product of the separate acceleration factors:

$$A_{VT} = \frac{t_1}{t_2} = \left(\frac{V_2}{V_1}\right)^n exp\left[\frac{E_a}{k}\left(\frac{1}{T_1} - \frac{1}{T_2}\right)\right]. \qquad (2\text{-}4)$$

where n is an empirical parameter that represents the voltage acceleration factors, E_a is an activation energy that represents the temperature acceleration factor, and k is the Boltzmann constant.

This well known Prokopowicz and Vaskas equation (*P-V* equation) [15] has proven to be useful in the capacitor industry for testing PME MLCCs at various highly accelerated testing conditions. An average of $n \approx 3$ has been found for the voltage acceleration factor, and an average value of $1 < E_a < 2$ eV is typical for the temperature acceleration factor [16-18].

Since only a single failure mode is assumed, the value of β in Eq. (2-2) should not change over applied stresses. Only the Weibull distribution scale parameter η will change with external stresses. This can be expressed, according to Eq. (2-4), as

$$\eta(V,T) = \frac{C}{V^n} \cdot e^{(\frac{B}{T})}, \qquad (2\text{-}5)$$

where C and $B = E_a/k$ are constants.

Due to the relatively high concentration of oxygen vacancies $[V_O^{\bullet\bullet}]$ in BME capacitors and the impact of electromigration of $[V_O^{\bullet\bullet}]$ on the reliability of BME capacitors, the acceleration function $AF(V,T)$ of BME capacitors has been found not always follow the power law with respect to applied voltage as specified in Eq. (2-4). The failure mechanisms of BME capacitors is also found more complicated than those in PME capacitors; at least two failure modes have been reported for BME capacitors [19,20]. The measurement of time-to-failure (TTF) under various acceleration conditions is not enough to model the reliability of BME capacitors with mixed failure modes.

An attempt that combines the measurement of both TTF and the capacitor leakage current as a function of stress has been developed and practiced to describe the reliability of BME capacitors [21]. Figure 2-1 shows the measured leakage current as a function of stress time for a 4.7 μF, 16V BME capacitor that was tested at 165°C and 72V. All capacitor units revealed a gradual, near-linear increase in leakage current. For some of them, this was followed by a catastrophic dielectric breakdown, characterized by a rapid and accelerated increase of leakage against time.

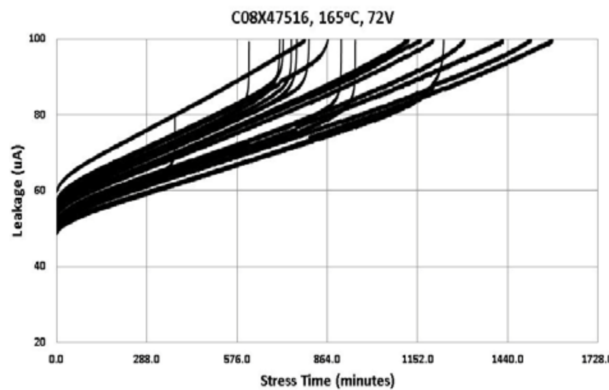

Figure 2-1. Leakage current of 20 BME capacitors as a function of stress time for a 4.7 μF, 16V BME capacitor from manufacturer C, tested at 165°C and 72V.

Two failure modes can be distinguished in Figure 2-1: catastrophic and slow degradation. Catastrophic failures are characterized by a time-accelerated increase of leakage current that may cause catastrophic damage to the capacitor (either avalanche or thermal runaway). Slow degradation failures are characterized by a gradual, near-linear increase of leakage current against stress time until the failure criterion (100μA) is reached. This slow degradation failure has been attributed to the electromigration of $[V_O^{\bullet\bullet}]$ that gradually reduced the barrier height at the grain boundary regime and caused a gradual leakage current increase, a failure mechanism that is dominant and unique for BME capacitors.

Based on the testing results showing in Figure 2-1, the failure mechanism in $BaTiO_3$ dielectric might be better described by a two-stage dielectric wearout process that initiated with a slow dielectric degradation, followed by a thermally dominated catastrophic breakdown (Figure 2-2). When the failure criterion is set with respect to a leakage current level, some BME capacitors will reach the failure level with a catastrophic failure, and some will fail prior to the occurrence of a catastrophic dielectric breakdown.

This two-stage dielectric wearout failure mechanism showing in Figure 2-2 for BME capacitors has been supported by failure analyses on BME capacitors that failed during accelerated life testing [22].

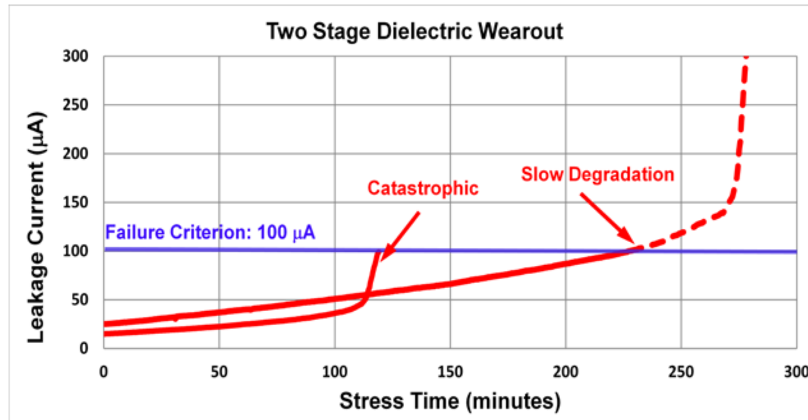

Figure 2-2. A two-stage dielectric wearout failure mode is proposed for describing the dielectric breakdown behaviors in BME capacitors [22].

Table 2-1 summarizes the TTF data measured under a given testing condition and how the data set has been divided into two groups by the leakage current characteristics. Accordingly, in Table 2-1, “F” and “S” stands for “failures” and “suspensions”. The Weibull modeling of the data set can also be processed in three different ways:

(1). Use all TTF data and fit them into a single Weibull distribution [Eq. (2-2)]. This is a common approach that has been practiced for many years by many users.

Table 2-1: Leakage Current Data showing in Figure 2-1 can be divided into two different failures

TTF (minutes)	Failure Mode	Complete Set	Slow Degradation	Catastrophic
377.26	Catastrophic	F	S	F
614.70	Catastrophic	F	S	F
712.00	Catastrophic	F	S	F
723.40	Catastrophic	F	S	F
749.30	Catastrophic	F	S	F
766.34	Catastrophic	F	S	F
793.25	Slow Degradation	F	F	S
805.29	Catastrophic	F	S	F
866.30	Catastrophic	F	S	F
908.27	Catastrophic	F	S	F
953.18	Catastrophic	F	S	F
1112.39	Slow Degradation	F	F	S
1124.51	Slow Degradation	F	F	S
1163.47	Slow Degradation	F	F	S
1203.19	Slow Degradation	F	F	S
1235.54	Catastrophic	F	S	F
1302.47	Slow Degradation	F	F	S
1425.38	Slow Degradation	F	F	S
1515.23	Slow Degradation	F	F	S
1583.30	Slow Degradation	F	F	S

(2). Only the data points that are designated as “slow degradation” failures will be used as failures; all the other data points will be considered as “suspensions” when the Eq. (2-2) is used to calculate Weibull distribution.

(3). The points designated “catastrophic” will be used as failures and the remaining data points will be labeled as “suspensions”.

This method of processing TTF data with mixed failure modes is called “failure/suspension” method.

Figure 2-3 shows the Weibull probability plot of the TTF data from Table 2-1 for a “complete set” (all time-to-failure data points are used as “failures” for Weibull modeling). Arrows are used to indicate the data points that failed “catastrophically.” It is interesting to point out that all data points appear to fit a SINGLE Weibull distribution function well. One would normally not consider the curve-fitting shown in Figure 2-3 being a result of mixed failure modes if the leakage current data was not used for the modeling. However, when the “failure/suspension” method as described here is used to model the TTF data with two different failure modes, the results clearly reveal the evidence of two failure modes. As shown in Figure 2-4(a), When the TTF data points were processed separately with different failure modes, the

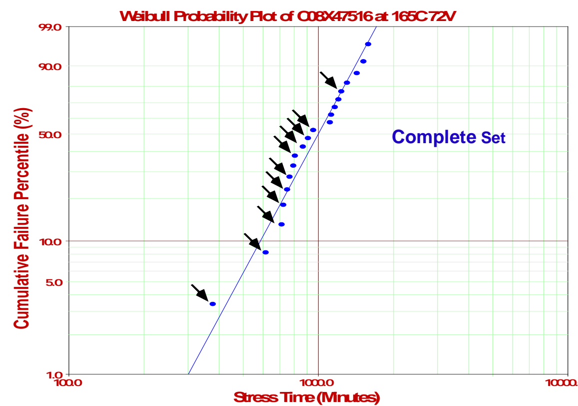

Figure 2-3. Weibull modeling results of TTF data from Table 2-1 for a BME capacitor, life tested at 165°C and 72V. The data points appear to fit a single Weibull distribution well, with arrows indicating all catastrophic failures.

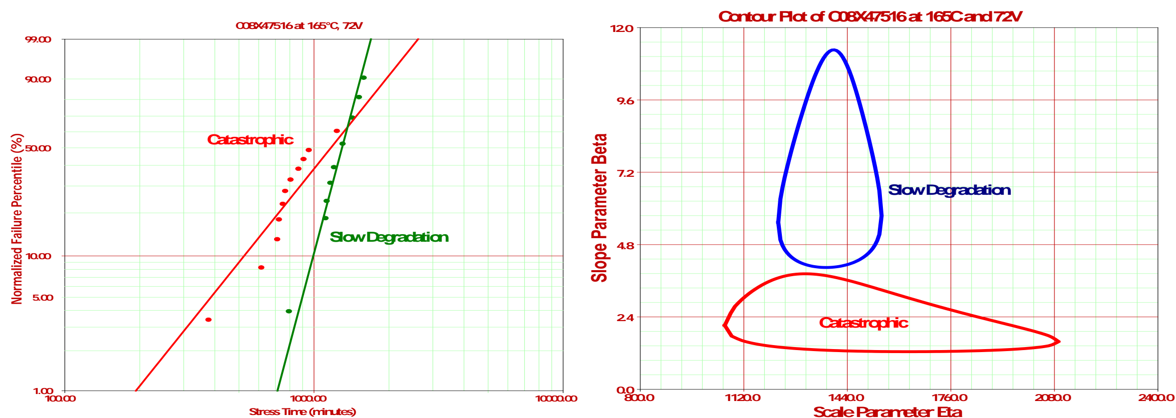

Figure 2-4. Weibull modeling results of TTF data from Table 2-1 for BME capacitor, life tested at 165°C and 72V. (a) Weibull plots of catastrophic and slow degradation failures with the same data set showing in Figure 2-3 being used. (b) Contour plot reveals the two slope parameters β for the two different failure modes, but the two subgroups share a similar scale parameter η.

distinguishable β and η values can be observed. Figure 2-4(b) shows the corresponding contour plots of the two subsets. It is clear that the two sub-data sets are completely separated in contour plots and must be *statistically* considered as two independent failure modes.

Based on the described "failure/suspension" modeling method, the total of three different sets of Weibull parameters can be calculated: i.e. complete set, catastrophic, and slow degradation. The approach can be repeated for the TTF data sets that were measured under other accelerated life testing conditions and corresponding MTTF life can be obtained per Eq. (2-3) for each testing condition.

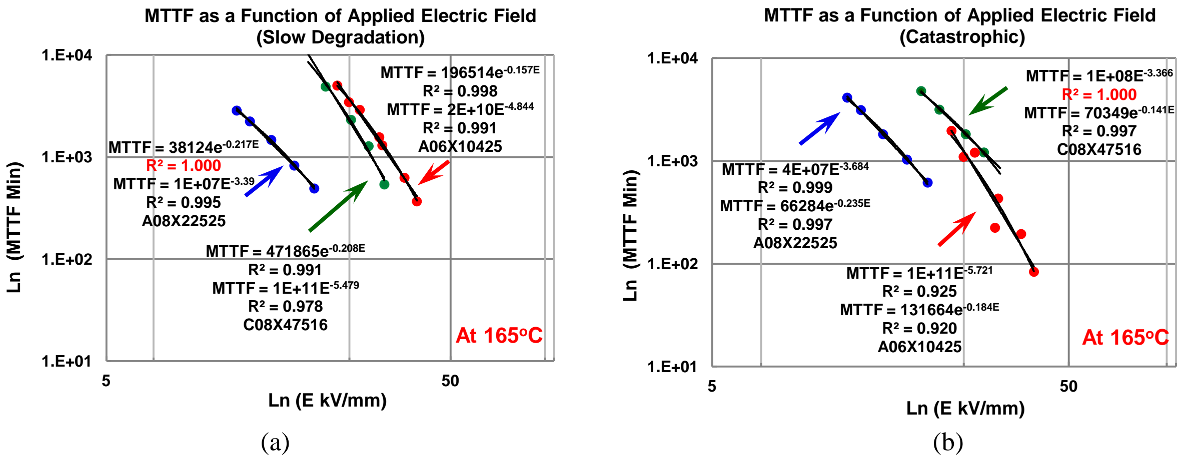

Figure 2-5. MTTF data as a function of applied electric field at 165°C for BME capacitors with slow degradation failures (a), and with catastrophic failures (b).

In order to better understand the acceleration functions of BME capacitors, the MTTF data as a function of electric field were re-plotted with respect to the failure modes. Figure 2-5 shows the MTTF data against electric field at a constant temperature (165°C). The MTTF data showing in Figure 2-5(a) include only the Weibull modeling results from units with slow degradation failures, as distinguished by leakage current measurement. The remaining units were modeled as suspensions. The MTTF data in Figure 2-5(b) are the opposite of the results showing in Figure 2-5(a). For slow degradation failures, exponential curve-fitting always gives rise to higher R^2 values [Figure 2-5(a)], and for catastrophic failures, power-law always results in higher R^2 values [Figure 2-5(b)]. The difference in R^2 is fairly small, but there are no exceptions! It is expected that the difference in R^2 for the two failure modes will become more distinct when more MTTF data points are available, particularly at lower electrical fields, although this may take years of testing to prove [23].

Table 2-2 summarizes the two voltage acceleration functions that may be applied to model the BME capacitors' reliability as showing in Figure 2-5, with respect to different levels of E and T, where $E \approx V/d$ is the electrical field per dielectric layer [21].

Table 2-2. Summary of Acceleration Functions for BME MLCCs

Type of acceleration factors	Expression to scale parameter η	Expression to time-to-failure (TTF)
E-Model (Low Field)	$\eta(E,T) = Ce^{-bE} \cdot e^{(\frac{E_a}{kT})}$	$\frac{t_1}{t_2} = exp[-b(E_1 - E_2)]exp\left[\frac{E_a}{k}\left(\frac{1}{T_1} - \frac{1}{T_2}\right)\right]$
Inverse Power-Law (P-V equation)	$\eta(V,T) = \frac{C}{V^n} \cdot e^{(\frac{E_a}{kT})}$	$\frac{t_1}{t_2} = \left(\frac{V_2}{V_1}\right)^n exp\left[\frac{E_a}{k}\left(\frac{1}{T_1} - \frac{1}{T_2}\right)\right]$

Finally, when mixed failure modes are present and each mode follows a different acceleration function, the Weibull reliability life of a BME capacitor Eq. (2-1) can be re-written as:

$$R(t) = \varphi(N, d, \bar{r}, S) \times AF(V,T) \times \gamma(t)$$

$$= \varphi(N, d, \bar{r}, S) \times \{ e^{-\left[\frac{t}{\frac{A}{V^n} \cdot e^{\left(\frac{E_{a1}}{kT}\right)}}\right]^{\beta_1}} + e^{-\left[\frac{t}{Ce^{-bE} \cdot e^{\left(\frac{E_{a2}}{kT}\right)}}\right]^{\beta_2}} \}. \qquad \text{(For BMEs)} \quad (2\text{-}6)$$

2-3. The Impacts of Capacitor Structure on Reliability of BME Capacitors

As defined in Eq. (2-1), the term $\varphi(N, d, \bar{r}, S \ldots)$ is attributed to the impacts of construction and microstructure parameters on the reliability of a BME MLCC. These parameters include average grain size $\bar{r}$ of the $BaTiO_3$ dielectric material, the measured average dielectric thickness *d*, the number of total dielectric layers *N*, and the chip size of a BME MLCC. They will be discussed separately below.

2-3-1. The Impact of Number of Dielectric Layers

As shown in Figure 2-6, a monolithic MLCC can be converted both constructively and electrically to a number of single layer ceramic capacitors connected in parallel. Assuming C_i is the *i*-th layer capacitor, the MLCC can be viewed as a parallel connection among C_1, C_2, C_3,… C_i,…, and C_N, where ***N*** is the number of dielectric layers inside an MLCC device. Since every single-layer capacitor C_i shares the same electrode area *S*, the same dielectric thickness *d*, and the same processing history, it is reasonable to assume that $C_1 = C_2 = C_3 = \cdots = C_i \ldots = C_N$.

So the sum of the capacitance C_t of an MLCC can be expressed as

$$C_t = C_1 + C_2 + C_3 \ldots + C_i \ldots + C_N = N \cdot C_i \qquad (2\text{-}7)$$

Similarly, the reliability of an MLCC with ***N*** dielectric layers that are connected in parallel can be expressed as

$$R_t = R_1 \times R_2 \times R_3 \ldots \times R_i \ldots \times R_N = R_i^N, \qquad (2\text{-}8)$$

where R_i is the reliability of an *i*-th single-layer capacitor, and R_t the overall reliability of a MLCC.

The reliability relationship shown in Eq. (2-8) indicates that the overall reliability R_t of an MLCC device is dependent highly on the reliability R_i of a single-layer capacitor inside a monolithic MLCC body. Since dielectric degradation is the primary cause of the long-term reliability failure of a single-layer capacitor, it is reasonable to assume that the reliability R_i is mainly determined by the reliability of ceramic $BaTiO_3$ dielectric material.

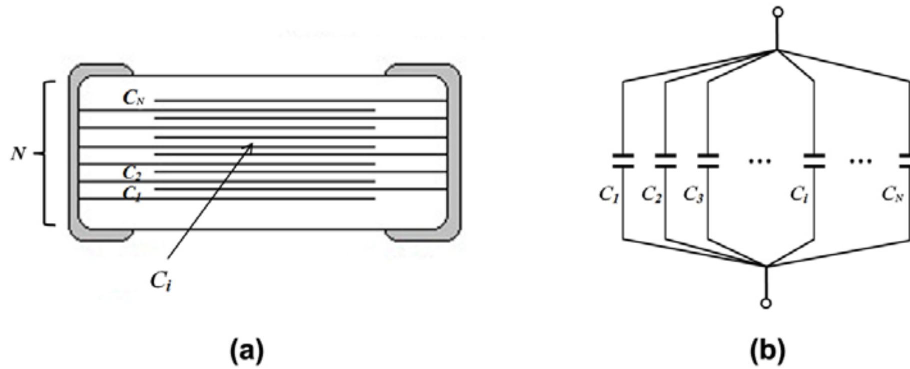

Figure 2-6. A cross-section view of a monolithic MLCC shows a stack of ***N*** layers of single-layer capacitors (a); this construction can be equivalently converted to the same number of single-layer capacitors connected in parallel.

From the structure of an MLCC unit shown in Figure 2-6, capacitor reliability can be expressed as:

$$R_t(t) = R_i(t)^N \tag{2-9}$$

where N is the number of individual dielectric layers and $R_i(t)$ is the reliability of a dielectric layer. The capacitor reliability $R_t(t)$ as a function of $R_i(t)$ and N is shown in Figure 8. In general, when dielectric reliability $R_i(t)$ is very close to unity, N does not have a significant impact on MLCC reliability $R_t(t)$. If $R_i(t)$ is reduced slightly, the overall reliability $R_t(t)$ of an

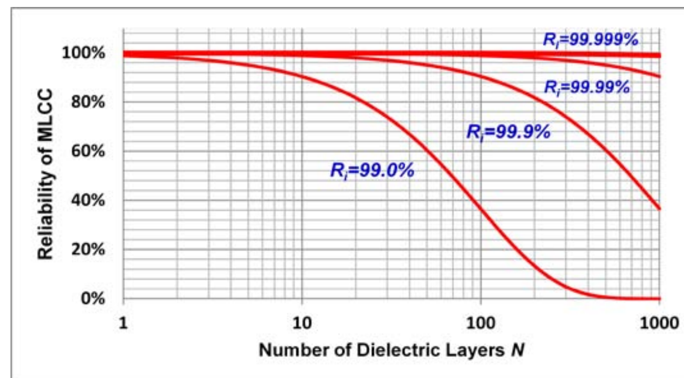

Figure 2-7. MLCC reliability $R_t(t)$ as a function of dielectric reliability $R_i(t)$ and number of dielectric layers N

MLCC can be degraded rapidly due to the amplifying effect of the number of dielectric layers *N*. Since most commercial BME capacitors are made with a large number of dielectric layers (typically N >250), the impact of *N* on BME capacitor reliability is critical.

<u>**2-3-2.** The Impact of Number of Grains per Dielectric Layer</u>

As shown in Eq. (2-9), the reliability of a MLCC unit can be determined by that of a single-layer capacitor $R_i(t)$. Once the number of dielectric layers (equivalent to number of single-layer capacitance C_i) N and $R_i(t)$ are both known, the reliability of a MLCC will also be known.

In this section the reliability of $R_i(t)$ will be discussed in detail. As shown in Figure 2-8, if a single-layer capacitor C_i has an average grain size of $\bar{r}$ and an average dielectric thickness d, the number of grains per dielectric layer can be easily determined as $\left(\frac{d}{\bar{r}}\right)$.

The MTTF of BME capacitors as a function of parameter $\left(\frac{d}{\bar{r}}\right)$ has been reported recently [24]. As shown in Figure 2-9, the measured MTTF data is proportional to the number of grains $\left(\frac{d}{\bar{r}}\right)$. On the other hand, if the voltage per grain boundary is adjusted to a similar value (1.85V here), all four MLCCs with different $\left(\frac{d}{\bar{r}}\right)$ values have similar MTTF values. According to Eq. (2-5), the MTTF of a BME capacitor at a given temperature can be written as:

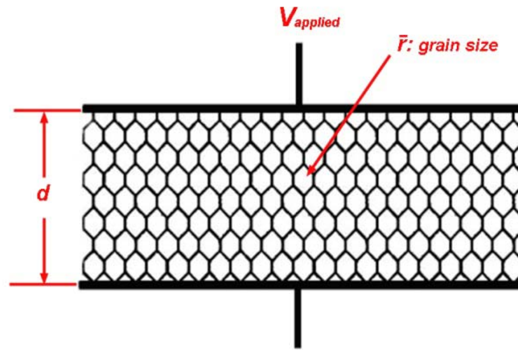

Figure 2-8. Estimate of number of grains in a dielectric layer: with an average dielectric thickness of d, and the average grain size of $\bar{r}$, the number of grains per dielectric layer can be obtained as $\left(\frac{d}{\bar{r}}\right)$.

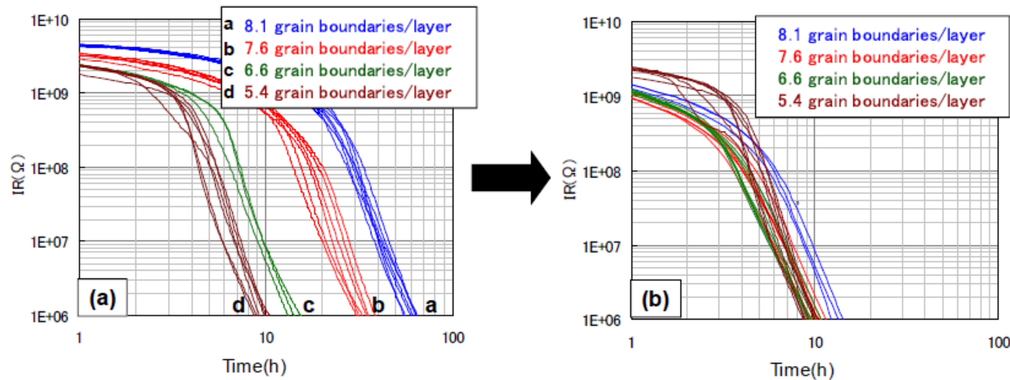

Figure 2-9. MTTF of BME capacitors as a function of grain boundaries per dielectric layer $\left(\frac{d}{\bar{r}}\right)$. Longer MTTF will be obtained for MLCCs with higher $\left(\frac{d}{\bar{r}}\right)$ values (left); when the applied voltage is adjusted to 1.85V per grain boundary, MTTF values become identical.

$$MTTF = \frac{1}{V_{grain}{}^{n}} = \frac{1}{\left[\frac{V_{applied}}{\left(\frac{d}{\bar{r}}\right)}\right]^{n}} = \frac{1}{V_{applied}{}^{n}} \times \left(\frac{d}{\bar{r}}\right)^{n}. \qquad (2\text{-}10)$$

This indicates that MTTF of BME capacitor follows a power-law relationship to the dielectric thickness d when applied voltage and average grain size are both given.

In order to implement the microstructure parameter $\left(\frac{d}{\bar{r}}\right)$ into the reliability of a single-layer capacitor, a structural model based on the dielectric thickness and the feature size of a defect can be developed and be briefly described below:

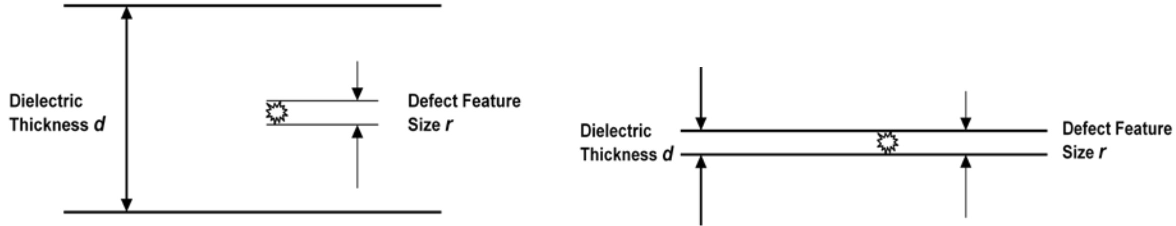

Figure 2-10. An illustration of dielectric thickness *d* with respect to the feature size *r* of an extrinsic defect inside the dielectric layer.
The dielectric layer reliability is dependent on the ratio *r/d*, (a), $d >> r$ (b), $d \approx r$.

As shown in Figure 2-10, assuming that the feature size of a defect that causes a catastrophic failure is *r*, *d* is the dielectric thickness, and the reliability of the defect is 0, then the reliability of a single dielectric layer $R_i(t)$ with thickness d will be determined by the value of d with respect to *r*. When *d* is far greater than the defect feature size *r*, the defect is non-harmful and may not cause any failures for many years, or even during a capacitor's lifetime. However, as d approaches the feature size of the defect *r*, the defect will cause dielectric failure instantly. In other words, the survival probability of the dielectric layer R_i can be written as $R_i(t) \to 1$ when $d >> r$ and as $R_i(t) \to 0$ when $d \approx r$. According to Eq. (2-10), the Weibull reliability of a dielectric layer with respect to its thickness d and the feature size of a defect *r* can thus be expressed as:

$$R_i(t) = e^{-\left(\frac{t}{\eta}\right)^{\beta}} \cdot \left[1 - \left(\frac{r}{d}\right)^{\xi}\right].$$

For simplicity, the defect size *r* can be directly related to the average grain size $\bar{r}$ as: $r \approx c \times \bar{r}$, where c is a constant. The equation above can be further expressed with respect to average grain size $\bar{r}$ as:

$$P = \left[1 - \left(\frac{r}{d}\right)^{\xi}\right] = \left[1 - \left(\frac{\bar{r}}{d}\right)^{\alpha}\right], \quad (\alpha \geq 5) \tag{2-11}$$

where P is a geometric factor that determines the dielectric layer reliability $R_i(t)$ with respect to the microstructure of an MLCC. α is a constant that was determined by the formulation, processing conditions, and microstructure of a BME capacitor. α was determined experimentally such that $\alpha \approx 6$ for V ≤ 50V and $\alpha \approx 5$ for V > 50V.

The Weibull reliability of a BME capacitor equals to unity when $t < \eta$, so that the reliability of a single dielectric layer inside a MLCC can be expressed as:

$$R_i(t < \eta) = e^{-\left(\frac{t}{\eta}\right)^{\beta}} \cdot \left[1 - \left(\frac{\bar{r}}{d}\right)^{\alpha}\right] = 1 \cdot \left[1 - \left(\frac{\bar{r}}{d}\right)^{\alpha}\right] = \left[1 - \left(\frac{\bar{r}}{d}\right)^{\alpha}\right]. \quad (2\text{-}12)$$

Combining Equations (2-9) and (2-12) yields the time-independent, simplified reliability of a BME MLCC:

$$R_t(t < \eta) = R_i(t < \eta)^N = \left[1 - \left(\frac{\bar{r}}{d}\right)^{\alpha}\right]^N, \quad (\alpha \geq 5). \quad (2\text{-}13)$$

Eq. (2-13) has been applied to evaluate the reliability of a BME MLCC as a function of its microstructure. Most BME capacitors were found to pass a life testing at 125°C, twice rated voltage for 4000 hours (as described in MIL-PRF-123) if:

$$R_t(t < \eta) = \left[1 - \left(\frac{\bar{r}}{d}\right)^{\alpha}\right]^N = 1.00000 \quad (2\text{-}14)$$

The number of zeroes in Eq. (2-14) can be related to the reliability levels with respect to the failure rate levels. As shown in Table 2-3, the chart on the left is from MIL-PRF-55681. The reliability levels are defined with respect to failure rate levels in percent. The reliability level can also be expressed by BX life with different percentage of failures. In addition, the BX life can further be related to the level of Weibull reliability, so that the number of zeros in Eq. (2-14) represents the level of reliability. Five zeros in Eq. (2-14) approximately correspond to a reliability level *S*.

Table 2-3. Reliability levels as function of *2*-parameter Weibull reliability.

TABLE V. Product level designator.

Symbol	Product level
C	non-ER
M	1.0 1/
P	0.1 1/
R	0.01 1/
S	0.001 1/

1/ FRL (percent per 1,000 hours).

BX life to Failure Rate:	BX life to Weibull Reliability:
M: B1% life	M: B1% life = $\eta\cdot\{-ln[R(x_1\%)]\}^{1/\beta}$, where $R(x_1\%)$ =0.99
P: B0.1% life	P: B0.1% life = $\eta\cdot\{-ln[R(x_2\%)]\}^{1/\beta}$, where $R(x_2\%)$ =0.999
R: B0.01% life	R: B0.01% life = $\eta\cdot\{-ln[R(x_3\%)]\}^{1/\beta}$, where $R(x_3\%)$ =0.9999
S: B0.001% life	S: B0.001% life = $\eta\cdot\{-ln[R(x_4\%)]\}^{1/\beta}$, where $R(x_4\%)$ =0.99999

2-3-3. The Impact of Chip Sizes

In order to reveal the impact of chip size on the reliability of BME MLCCs, the effective area of a MLCC device with a different chip size has been measured and normalized with respect to EIA chip size of 0402, the smallest chip size in the group. Corresponding measured results are summarized in Table 2-4. The chip scaling factor ***S*** represents how many times of effective area a given EIA chip size to that of 0402. For example, the effective chip size of a 0805 MLCC is equal to 6.76 times of a 0402 MLCC connected in parallel.

As shown in Figure 2-2 and Eq. (2-8), the reliability of a 0805 MLCC can thus be expressed with respect to that of a 0402 MLCC as:

$$R_{0805} = R_{0402}^{6.76}.$$

In general, when the chip size scaling factor ***S*** is used, the reliability of a MLCC with an EIA chip size of *xy* can be expressed with respect to the reliability of a 0402 MLCC as:

Table 2-4. EIA chip size and calculated scaling factors for BME capacitors

Chip Size	Length (μm)	Width (μm)	Terminal-t (μm)	Side margin (μm)	End margin (μm)	Effective area (mm^2)	Chip Size Scaling Factor ***S***
0402	1000 ± 100	500 ± 100	250 ± 150	125	100	0.225	1.00
0603	1600 ± 150	810 ± 150	350 ± 150	175	100	0.763	3.39
0805	2010 ± 200	1250 ± 200	500 ± 200	250	150	1.520	6.76
1206	3200 ± 200	1600 ± 200	500 ± 200	250	150	3.510	15.60
1210	3200 ± 200	2500 ± 200	500 ± 200	250	150	5.940	26.40
1812	4500 ± 300	3200 ± 200	610 ± 300	300	200	10.920	48.53
2220	5700 ± 400	5000 ± 400	640 ± 390	320	220	23.074	102.55
1825	4500 ± 300	6400 ± 400	610 ± 360	300	220	23.244	103.31

$$R_{xy} = R_{0402}^{S}$$

When the chip size scaling factor increases by a hundredfold, the reliability declines: 45% when R_{0402} = 99%; 10% when R_{0402}= 99.9%; and 1% when R_{0402}= 99.99%. The reliability of MLCCs decreases with increasing chip size, but not significantly as compared to by number of dielectric layers.

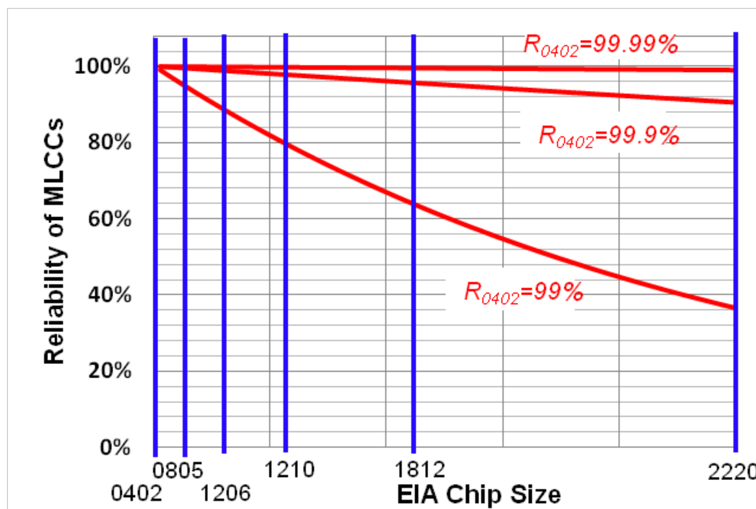

Figure 2-11. MLCC reliability $R_t(t)$ as a function of EIA chip size and the reliability of a 0402 MLCC R_{0402}

On the other hand, the dielectric thickness is also found to gradually increase with the MLCC chip size. Figure 2-12 shows the construction analysis results of average dielectric thickness as a function of chip size. According to Eq. (2-10), the MTTF of an MLCC follows a power-law increase with increasing dielectric thickness. Therefore, the reliability decreases due to increasing chip size have been fully “compensated” by increasing the dielectric thickness. As a result of that, the overall reliability of a MLCC will not change significantly with increasing capacitor chip size.

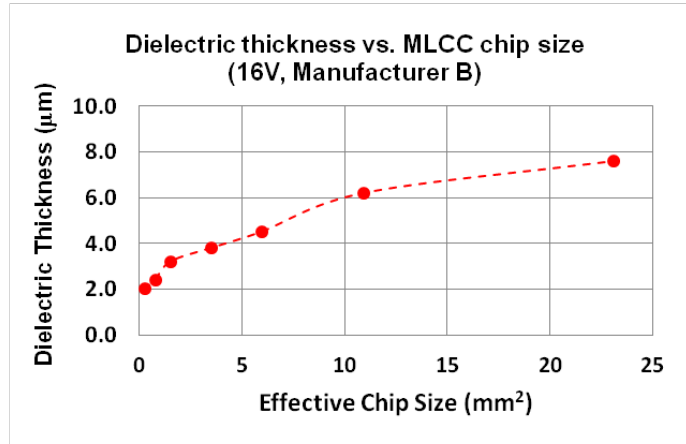

Figure 2-12. Measured average dielectric thickness as function of BME MLCC chip size.

In summary, the general expression of BME capacitor's reliability Eq. (2-1) can finally be written as:

$$R(t) = \varphi(N, d, \bar{r}, S) \times AF(V, T) \times \gamma(t)$$

$$= \left[1 - \left(\frac{\bar{r}}{d}\right)^{\alpha}\right]^{N} \left\{ e^{-\left[\frac{t}{\frac{A}{V^{n}} \cdot e^{\left(\frac{E_{a1}}{kT}\right)}}\right]^{\beta_1}} + e^{-\left[\frac{t}{Ce^{-bE} \cdot e^{\left(\frac{E_{a2}}{kT}\right)}}\right]^{\beta_2}} \right\}.$$

3. Selection of Commercial BME Capacitors for High Reliability Applications

All BME capacitors are fabricated for commercial applications. Per this study, Eq. (2-14) describes the impacts from BME capacitor structure on reliability. Application of Eq. (2-14) has two-fold: The manufacturer should use it as a first-principle guideline to make BME capacitors for high-reliability applications. The users of BME capacitors should perform construction analysis on the BME capacitors to make sure they meet specific criteria prior to tedious and costly lot qualification and quality conformance inspection. These requirements have been outlined in Table 3-1 for selection of BME capacitors.

Table 3-1. Selection criteria of BME capacitors for space-level applications

Inspection/Test	Test Methods, Conditions, and Requirements	Part Type/Level		
		1	2	3
1. Dielectric Type	The voltage temperature characteristic shall be referenced to the +25°C value and shall be applicable over the entire temperature range of -55°C to +125°C. Dielectric type C0G (N) shall be 0±30 ppm/°C, and dielectric type X7R (X) shall be +15, -15%.	X	X	X
2. Destructive Physical Analysis (DPA)	Destructive physical analysis shall be performed on each inspection lot of capacitors supplied to this specification. - DPA sample size shall follow MIL-PRF-123, Table XVII. - DPA shall be performed in accordance with the requirements of MIL-PRF-123, paragraph 4.6.1, except that paragraphs 3.4.1 and 3.4.2 shall be replaced with paragraph 2.3 herein. - Margin defects shall be determined using EIA 469, paragraph 5.1.3.	X	X	X
3. Microstructure Analysis	BME capacitors shall not be used for high reliability space applications if the following construction and microstructure criteria are not satisfied	X	X	X
3.1. Nickel Electrodes	All BME capacitors shall use nickel for internal electrodes			
3.2.Capacitor Structure Parameter	The structure parameter of a BME ceramic capacitor *P* with respect to its microstructure and construction details can be expressed as: $P = \left[1 - \left(\frac{\bar{a}}{d}\right)^{\alpha}\right]^{N}$ Where: d = Dielectric thickness that is the actual measured thickness of the fired ceramic dielectric layer. Voids, or the cumulative effect of voids, shall not reduce the total dielectric thickness by more than 50%. ā= Averaged ceramic grain size measured per the linear interception method. N = Number of individual dielectric layers. α= An empirical parameter that is applied voltage-dependent: α= 6 for V ≤ 50V, and α= 5 for V > 50V.			
3.3. Acceptance Criterion for X7R	The calculated *R* shall be greater than **1.00000** for the X7R dielectric			
3.4. Acceptance Criterion for C0G**1/**	The minimum dielectric thickness shall be greater than 3.0 micrometers for the NPO dielectric at V ≤ 50V and greater than 5.0 micrometers at V > 50V; *N* should be less than 300.			
4. Maximum dielectric constant	The maximum dielectric constant shall be 4000 for the X7R dielectric and 100 for the C0G dielectric.	X	X	X
5. Termination	Devices supplied to this specification shall have a termination coating of copper, nickel, or their alloy, or shall be base-metal barrier tin-lead solder (MIL-PRF-123, type Z) plated. Tin-lead solder plating shall contain a minimum of 4% lead, by mass.	X	X	X

1/: BME capacitors with NPO dielectric of $CaZrO_3$ are not ferroelectric and the MTTF is not controlled by the grain boundaries, therefore, NPO capacitors have a different selection criterion from those with X7R dielectric.

4. Lot Qualification Plan

Almost all BME capacitors are manufactured outside the United States. In-process and raw material control become important. Suppliers should not only provide the documentation on the raw material source and batch-to-batch consistency control, but also implement an in-process inspection plan to ensure that high-reliability BME capacitors are made.

4.1 In-Process Inspection would be performed for each production lot during the qualification. The inspection should be performed as per Table 4-1.

4.2. The raw material control and lot inspection shall follow MIL-PRF-123, paragraph 4.5.2.1.

Table 4-1. In-Process Inspection Plan

In-process inspection	Requirement MIL-PRF-123	Test method MIL-PRF-123	Sample size
Nondestructive internal examination (C-SAM)	Paragraph 3.5	Paragraph 4.6.1	100%
Pre-termination destructive physical analysis	Paragraph 3.6	Paragraph 4.6.2	80 (2)
Visual examination	Paragraph 3.7	Paragraph 4.6.3	100%
Post termination, unencapsulated destructive physical analysis	Paragraph 3.15	Paragraph 4.6.11	40 (0)

5. Qualification of BME Capacitors

For ceramic capacitors with established reliability, such as those PME capacitors that meet all requirements of MIL-PRF-123, the qualification of the products is only required to be performed during the initial qualification of the process and when processes or materials are changes. However, since BME capacitors are commercial product and do not have any established reliability, the qualification shall be performed for each production lot after the selection of BME capacitors per Table 3-1. The production lot qualification plan is summarized in Table 5-1. For comparison purposes, the specifications from different testing plans have been listed for reference; AEC-Q200 is the qualification plan that industry has been used for automotive grade BME capacitors.

Table 5-1: BME Capacitors Lot Qualifications

Inspection/Test	**Test Methods, Conditions, and Requirements**	**Sample Size**		
		AEC-Q200	**MIL-PRF-123**	**This Document**
Group I				
1. Thermal Shock	MIL-STD-202, Method 107, Condition B, min. rated temp. to max. rated temp. (when specified in the product specification/ data sheet, the min. and max. “storage” temp. shall be used in lieu of the specified operating temp.)	N/A	182	200
2. Voltage Conditioning (Burn-In)	4 x rated voltage, 125 °C, 160 hours (Level 1) 125 °C, 96 hours (Level 2) 125 °C, 48 hours (Level 3)	N/A	182	200
3. Electrical Measurements	As specified			
Capacitance Dissipation Factor DWV Insulation Resistance	MIL-STD-202, Method 305 MIL-STD-202, Method 305(shall be 306) MIL-STD-202, Method 301 MIL-STD-202, Method 302	100%	100%	100%
Group II		-	-	
1. Visual and Mechanical Examination, material, design, construction and workmanship	Visual and sample-based mechanical inspection to be performed to requirements of applicable military specification	100%	15(1)	100%
2. Destructive physical analysis	Destructive physical analysis shall be performed on each inspection lot of capacitors supplied to this specification. - DPA shall be performed in accordance with the requirements of MIL-PRF-123, paragraph 4.6.1, except that paragraphs 3.4.1 and 3.4.2 shall be replaced with paragraph 2.3 herein. - Margin defects shall be determined using EIA 469, paragraph 5.1.3.	10	15(1)	15(0)

Table 5-1: BME Capacitors Lot Qualifications (Cont'd)

Inspection/Test	Test Methods, Conditions, and Requirements	Sample Size		
		AEC-Q200	MIL-PRF-123	This Document
Group IIIb - Nonleaded devices				
1. Terminal strength	AEC-Q200-006; MIL-STD-202, Method 211	30	12(1)	15(0)
2. Solderability	MIL-STD-202, Method 208	15	12(1)	15(0)
3. Resistance to soldering heat	MIL-STD-202, Method 210; condition C	30	12(1)	15(0)
Group IV				
1. Voltage-temperature limits	Capacitance change over the range of temperatures and voltages specified shall not exceed limits of specification. NPO Capacitors shall be tested in accordance with MIL-PRF-123 BP characteristics.	N/A	12(1)	15(0)
2. Moisture resistance	MIL-STD-202, Method 106 20 cycles (first 10 cycles with rated voltage applied) DWV, IR and DC to specification **AEC-Q200-006 removed this test in version D**	77	12(1)	15(0)
Group V				
1. Humidity, steady state, low voltage*	Not required for BME capacitors	N/A	12(0)	
1. Biased Humidity	MIL-STD-202, Method 103 **AEC-Q200 Biased Humidity**	77	N/A	125(0)
2. Beam Load Test	**AEC-Q200 -003**	30	N/A	15(0)
3. Resistance to solvents	MIL-STD-202, Method 215	5	12(1)	15(0)
Group VI				
Life	MIL-STD-202, Method 108 T_{test} = maximum operating temperature V_{test} = 2 X Vrated (**1X Vrated perAEC-Q200-006**) Duration: 4,000 hours for level 1, 2,000 hours for levels 2 and 3 IR, ΔC, and DF to specification	77	123(1)	125(0)

*: Testing for humidity, steady state, and low voltage in Group V is required for PME capacitors with potential micro cracks and silver electrode migration. For BME capacitors the biased humidity testing is better to reveal the defects due to exposure to humidity.

6. Quality Conformance Inspection

Before delivery, all BME capacitors shall be subjected to quality conformance inspection testing to ensure that they meet selected requirements of this document. Quality conformance inspection shall be performed as follows:

6.1. Group A inspection shall be performed per Table 6-1.

Table 6-1. Group A inspection

In-process inspection	Requirement MIL-PRF-123	Test method MIL-PRF-123	Sample size
Subgroup 1 Thermal shock and voltage conditioning 1/ 2/	Paragraph 3.10	Paragraph 4.6.1.1	100%
Voltage conditioning at +85°C 2/ 3/	Paragraph 3.10	Paragraph 4.6.6.3	100%
Subgroup 2 Visual and mechanical inspection; material, physical dimensions, design, construction, marking, and workmanship	Paragraph 3.1, 3.4, 3.24, and 3.25	Paragraph 4.6.3	20 (0)
Subgroup 3 Destructive physical analysis	Paragraph 3.15	Paragraph 4.6.11	40 (0)

1/: For solder coated nonleaded capacitor chips, thermal shock and voltage conditioning in accordance with 4.6.6.1 and 4.6.6.2 may be performed prior to addition of final metallization; and if performed, shall not be required during group A.
2/: The DWV post test is not applicable if optional voltage conditioning was performed at **400** percent or more of the rated voltage.
3/: Voltage conditioning at +85°C is only required for solder coated nonleaded capacitor chips that had voltage conditioning performed prior to final metallization.

6.2. Group B inspection should be performed as shown in Table 6-2 below:

Table 6-2. Group B Inspection

Inspection	Required Paragraph	Test Method Paragraph	Sample Size	Accept/Reject
Subgroup 1 Thermal shock Life test	MIL-PRF-123 Paragraph 3.10 Paragraph 3.23	MIL-PRF-123 Paragraph 4.6.6.1 Paragraph 4.6.19	125	0
Subgroup 2 Voltage-temperature limit Moisture resistance	MIL-PRF-123 Paragraph 3.19 Paragraph 3.20	MIL-PRF-123 Paragraph 4.6.15 Paragraph 4.6.16.2	12	0
Subgroup 3 Terminal strength Solderability Resistance to soldering heat	MIL-PRF-123 Paragraph 3.16 Paragraph 3.17.2 Paragraph 3.18.2	MIL-PRF-123 Paragraph 4.6.12.2 Paragraph 4.6.13.2 Paragraph 4.6.14.2	12	0

7. Voltage Rating and Derating of BME Capacitors with X7R Dielectric

7-1. Microstructure and Voltage Rating, Derating

Many electrical components exhibit extended life when voltage derating is practiced, indicating the failure mechanism is primarily due to excess of applied voltage (electric field). This is also true for BME capacitors with $BaTiO_3$ dielectric material. However, the voltage rating and derating process in ceramic $BaTiO_3$ is determined by its unique microstructures.

As shown in Figure 2-8 a ceramic dielectric layer consists of close-packed grains of $BaTiO_3$. One of the better-known structural characteristics of a $BaTiO_3$ grain is the formation of a core-shell structure in each $BaTiO_3$ grain: a single crystal core is enclosed by a thin layer of non-ferroelectric shell (Figure 7-1). This inhomogeneous core-shell structure also reveals a significant difference in the measurement of conductivity: the shell is typically several magnitudes higher in insulating resistance than that of the core (interior of a grain).

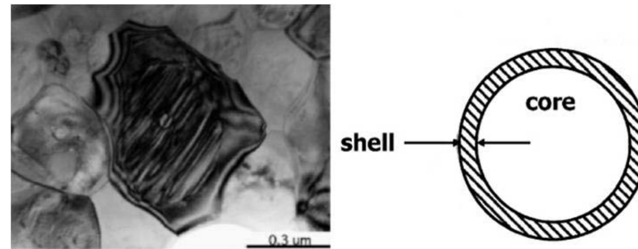

Figure 7-1. A typical core-shell grain structure in $BaTiO_3$ dielectric layer of a BME capacitor.

When an external voltage is applied, this inhomogeneity in the resistance between an interior grain and a grain boundary will cause a significantly inhomogeneous distribution of voltages among the grains: the grain boundaries will sustain the majority of the voltage drop in a dielectric layer.

For two dielectric layers with the same thickness d and applied voltage $V_{applied}$, the smaller the grain size, the lower the voltage will be shared by an individual grain. In order to accurately describe this inhomogeneity and its impact on the reliability of a $BaTiO_3$ dielectric layer, it is important to use *voltage per grain* to reflect the applied voltage on the performance of the dielectric layer.

As illustrated in Figure 2-8 and previous described in Eq. (2-10), the voltage per grain V_{grain} can be simply written as:

$$V_{grain} = \frac{V_{applied}}{\left(\frac{d}{\bar{r}}\right)} = V_{applied} \times \left(\frac{\bar{r}}{d}\right). \tag{7-1}$$

A number of BME capacitors from different manufacturers with different chip size, capacitance, and rated voltage have been processed for microstructure analysis to determine the Volts/Grain (V_{grain}.) Corresponding results are summarized in Table 7-1. It is clear that at a given rated voltage, the $\boldsymbol{V_{grain}}$ is almost a constant. It decreases with decreasing rated voltage of BME capacitors. Similarly, the number of grains per dielectric layer does not change more than 13%

when the rated voltage is 25V. From these testing data one can conclude that ***the rated voltage of a BME capacitor with X7R $BaTiO_3$ dielectric is determined by the microstructure of dielectric material.***

Table 7-1. Number of grains and voltage per grain of BME capacitors

CAP ID*	Rated Voltage	Grain Size (μm)	Dielectric Thickness(μm)	No. of grains per layer	Voltage per Grain (V)
A08X22525	25	0.305	3.89	12.75	1.96
B08X10525	25	0.400	4.60	11.50	2.17
C08X22525	25	0.320	3.80	11.88	2.11
B08X33425	25	0.420	5.80	13.81	1.81
A06X10425	25	0.470	7.89	16.79	1.49
B06X22425	25	0.340	4.20	12.35	2.02
B04X47325	25	0.305	4.00	13.11	1.91
C04X47325	25	0.386	4.40	11.40	2.19
B12X10525	25	0.421	6.15	14.61	1.71
B12X47525	25	0.376	4.34	11.54	2.17
C08X56425	25	0.339	4.00	11.80	2.12
P08X10425	25	0.790	20.20	25.57	0.98
A06X10516	16	0.296	3.01	10.17	1.57
A12X10616	16	0.344	3.51	10.20	1.57
C04X10416	16	0.332	3.40	10.24	1.56
A08X47416	16	0.319	3.75	11.76	1.36
B12X68416	16	0.375	6.21	16.56	0.97
C08X22516	16	0.224	3.81	17.01	0.94
C12X10616	16	0.264	2.80	10.61	1.51
B08X22516	16	0.340	3.23	9.50	1.68
B08X56416	16	0.373	4.21	11.29	1.42
C08X47516	16	0.230	2.49	10.83	1.48
B12X10516	16	0.475	7.82	16.45	0.97
B04X10416	16	0.342	3.05	8.91	1.80
B12X10606	6.3	0.365	3.11	8.51	0.74
B04X10406	6.3	0.323	2.50	7.74	0.81
B04X56306	6.3	0.407	3.00	7.37	0.85
B06X10506	6.3	0.426	2.80	6.57	0.96
C08X10606	6.3	0.330	2.23	6.76	0.93
B08X22506	6.3	0.419	3.42	8.16	0.77
A12X22606	6.3	0.309	1.82	5.90	1.07
B06X22406	6.3	0.373	4.01	10.76	0.59
P06X10405	5.0	0.770	12.60	16.36	0.39

*: Capacitor ID: C (manufacturer ID); 08 (EIA chip size, 08=0805); X (dielectric type, X=X7R); 475 (cap values, 475=4,700,000 pF); 16 (rated voltage). For example: D06X36405 = 360000pF, 5V, 0603, from manufacturer D. First letter P represents PME capacitors.

Eq. (7-1) also explains that why smaller grains are always favorable for better reliability performance, because when dielectric thickness d and applied voltage $V_{applied}$ is fixed, the dielectric with smaller grain size will have lower voltage per grain, which, according to the reliability life testing results in Figure 2-9, will lead to a longer dielectric reliability life.

Per MIL-PRF-123, all PME capacitors with X7R-type dielectric shall have a minimum dielectric thickness of 20 μm at 50V rating. In general, a 50% voltage derating is required for PME capacitors with 50V rating for space applications. This corresponds to a value of $V_{grain} = 1.18V$ as shown in Table 7-2. Accordingly, the percent of voltage derating for BME capacitors can be

determined by simply matching that same V_{grain} value for a PME capacitor. This gives rise to a 60% voltage derating factor for BME capacitors, i.e. a 10V BME capacitor, when derated by 60%, will equal to 60% × 10V=4V).

Table 7-2. Determination of voltage derating for BME capacitors

Technology	Rated voltage	Dielectric thickness *d* (µm) (Measured)	Grains per layer (Measured)	Voltage (V) at 60% derating/No. of grains	Max. V/grain After 60% Derating	Average Grain Size (µm)	Minimum *d* after derating (µm)
PME	50V	20.1-22.3	21.10-27.34	25/21.10*	1.18*	0.50	16.88
BME	50V	6.50-9.00	17.00-20.10	20/17.00	1.18	0.38	10.34**
BME	25V	3.20-6.15	11.40-12.75	10/11.40	0.88	0.39	7.11
BME	16V	2.80-4.21	8.90-11.80	6.4/8.90	0.72	0.34	4.84
BME	6.3V	1.82-4.01	6.60-10.76	2.52/6.60	0.39	0.39	4.08

*: 50% derating for a 50V PME MLCC. **: According to AVX ESA testing vehicle, *d* = 9 µm.

It is also worth noting that V_{grain} in Table 7-2 decreases with decreasing rated voltage for BME capacitors. This is simply because the BME capacitors with lower rated voltage always have a thinner dielectric layer. The variation in the grain size will result in more reduction in minimum number of grains for thinner grains; an effect that is less critical in BME capacitors with thicker dielectric layers.

The minimum dielectric thickness d_{min} as a function of rated voltage can also be determined experimentally using the formula below:

$$d_{min}(after\ derating) = \left(\frac{d}{\bar{r}}\right)_{min} \times \bar{r} \times 1.6$$

Where $\left(\frac{d}{\bar{r}}\right)_{min}$ represents the smallest number of grains per dielectric layer and therefore a worst-case scenario. The multiple factor of 1.6 is due to the 60% voltage derating that will allow for the same percent of dielectric thickness to be added as a safety margin. Figure 7-2 shows the minimum dielectric thickness against rated voltage which forms a near linear relationship.

It is important to point out that the minimum dielectric thickness values obtained here are only for calculated voltage derating practice.

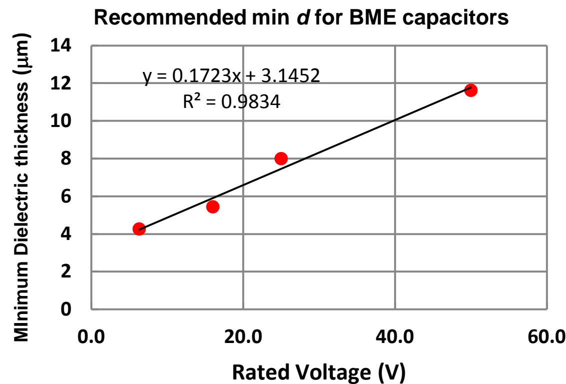

Figure 7-2. Recommended minimum dielectric thickness verses rated voltage that was experimentally determined in this study.

7-2. Determination of Maximum Ambient Temperatures

When an alternating current flows through a capacitor, heat will be generated. The evaluation of this heat generation and dissipation is called ripple current test. Ripple current is the root mean square (rms) value of alternating current flowing through a capacitor. In order to determined the maximum temperature increase due to the ripple current, it is necessary to understand how much heat will be generated at a given level and how effectively the generated heat can be dissipated.

If a capacitor is conducting ripple current, the power generated due to the current is $\approx I^2 \times ESR$, where I is the ripple current and ESR is the equivalent series resistance of a capacitor. Figure 7-3 shows the typical ESR values measured for a variety of capacitors. Clearly a MLCC has the lowest ESR values and therefore has less heat generation if the same level of ripple current is applied to all capacitors.

The thermal dissipating ability of a MLCC was also studied in early 1980s when the decision had to be made on whether ripple current testing should be required in the military standard for PME MLCCs.

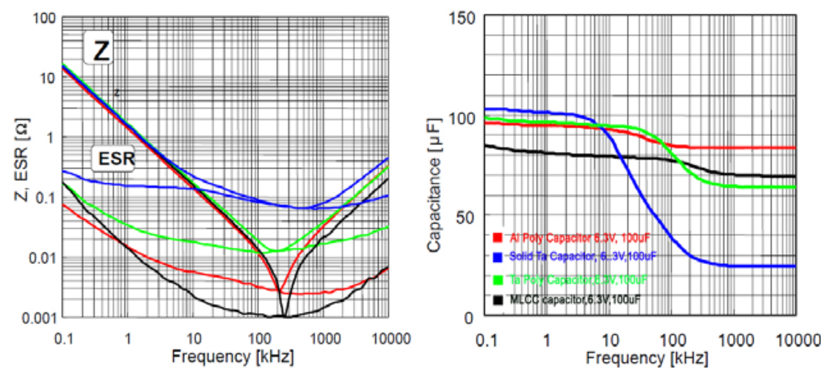

Figure 7-3. Capacitor technology Comparison of ESR and capacitance change against frequency

Figure 7-4 shows a thermal structure that was built for MLCCs by F. M. Schabauer and R. Blumkin [25], which allows the theoretical determination of the temperature rise of an MLCC due to AC current flowing through it. This in-depth analysis has given rise to following conclusions:

(1). The temperature rise (ΔT) caused by the ripple current should not exceed 20°C above the ambient temperature of the capacitor.

(2). Peak to peak voltage value (*Vp-p*) and zero to peak voltage value (*Vo-p*), including DC bias for the applied voltage, must be within the rated voltage (DC).

(3). The maximum operating temperature (110°C), including the amount of self-generated heat, should not be exceeded.

As a result of this study, the ripple current test has been decided not to be needed in military specifications for MLCC evaluations. Indeed, ripple current in ceramic capacitors is typically processed at the circuit designer level, as an application issue. Nowadays, most MLCC suppliers provide free software for ripple current estimation and numbers of application notes are also provided by the manufacturers to circuit designers for MLCC power rating.

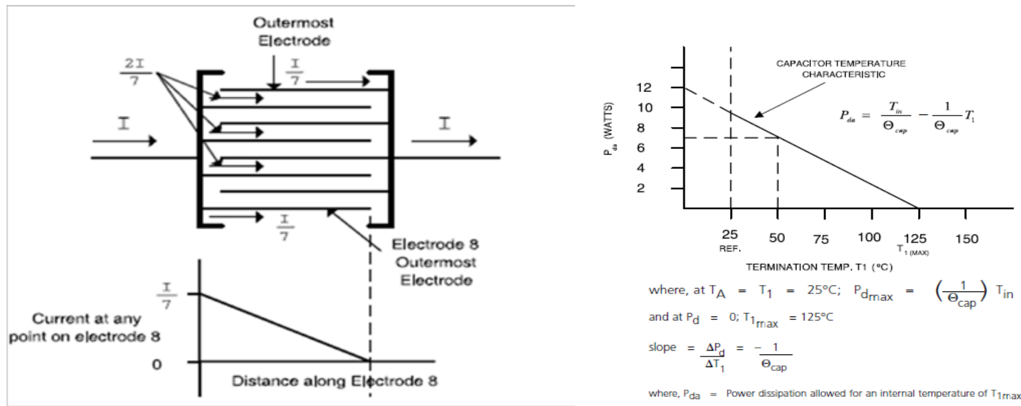

Figure 7-4. Thermal structure of a MLCC (left) and the calculated results on power rating of MLCCs

Although this theoretical work was performed for PME capacitors, it can be readily applied to the ripple current testing in BME capacitors. Both BME and PME capacitors consist of a number of internal electrode plates. These electrode plates act as heat extractors (heat sinks) into the thermally resistive ceramic block. The more plates into that ceramic block, the easier the heat generated can flow out of the block. When compared to PME capacitors for a same chip size and same voltage rating, BME capacitors normally have more internal electrode plates and thinner dielectric layers. As a result of that, BME capacitors often possess a better thermal structure for heat dissipation. A recent ripple current testing study on a number of BME capacitors have shown the temperature increase due to ripple current is negligible [26].

No military specifications require ripple current testing of PME MLCCs. Ripple current testing for BME capacitors is similarly not required by AEC Q200 or by this document.

The voltage derating is more critical for $BaTiO_3$-based X7R dielectrics since reliability and voltage robustness are highly dependent on volts per grain. BME capacitors with NPO dielectrics are non-ferroelectric and are not grain boundary-dependent. When processed correctly, the NPO-type dielectric with $CaZrO_3$ showed extremely high dielectric breakdown strength (>8 times the related voltage at 165°C). As result, only smaller voltage derating factors at high temperatures are necessary for ensuring high-reliability performance [27].

7.1. Derating shall be performed by the designer in accordance with the requirements set in Table 7-3 herein for different dielectric types.

7.2. Voltage derating is accomplished by multiplying the maximum operating voltage by the appropriate derating factor appearing in Table 7-3 herein.

7.3. The derating factor applies to the sum of peak AC ripple and DC voltage applied.

Table 7-3. Voltage De-rating Chart for BME Capacitors

Dielectric Type	Voltage De-rating Factors	Maximum Ambient Temperature
X7R	0.6	110°C
NPO	0.8	125°C

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