Development of Guidelines for Base-Metal Electrode (BME) Multilayer Ceramic Capacitors (MLCCs)

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Basic Facts of BME Products

- As a commercial technology, most BME capacitors are manufactured for high volumetric applications: i.e., highest capacitance per volume
- Only a small portion of commercial-off-the-shelf (COTS) BME capacitors can meet high reliability applications
- Two options when beginning work with commercial BME capacitors
  - Approach 1
    - Select from BME product catalog using a quick turnaround screening method (pick up a few good apples from a bucket of a mixture) to eliminate those that will never pass high reliability qualifications
    - Use an existing qualification documentations for high reliability evaluations of a specific product line
    - Existing Documents: MIL-PRF-123 for PME capacitors; MIL-PRF-55681, NASA-EEE-INST-002, GSFC S-311-P-829C, AEC-Q200, GIDEP, etc.
  - Approach 2
    - Select units from various suppliers (typically 100% screened and meeting a certain level of reliability, e.g., automotive grade) with moderate cap values, and perform significant voltage de-rating
    - Develop a part selection list and a general guideline that may apply to several suppliers' products : Commodity products
- Different source, different behavior

Presented by David (Donhang) Liu at the G-11/G-12 Industrial Base Metal Electrode (BME) Capacitors WebEx, hosted by workspace.techamerica.org, April 8, 2013 and published on nepp.nasa.gov.

Some Questions on BME Capacitors

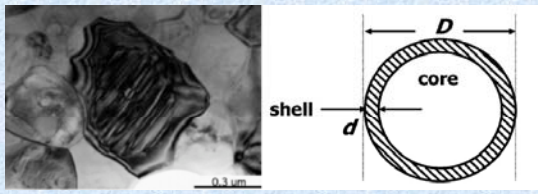
- What determine the rated voltage and how to derate it?
- Do we need a minimum dielectric thickness for BME as for PME?
- How to simply screen BE capacitors for high-reliability applications? If possible?
- Impact of *microstructures* (dielectric thickness, grain size) and *macrostructures* (number of layers, chip size, etc.) on reliability?
- What is the true impact of oxygen vacancy migrations on the reliability and failure modes of BME capacitors? (*D. Liu, CARTS conference paper, 2013*)
- Is ripple current testing really needed for BME capacitors?

Guideline Development for BME Capacitors

List of Publications on BME Capacitors Funded by NASA NEPP Programs

1. D. Liu, H. Leidecker, T. Perry, and F. Felt, "Accelerating Factors in Life Testing of High-Voltage Multilayer Ceramic Capacitors," *CARTS Proceedings*, pp. 245, (2005)
2. D. Liu and M. Sampson, "Reliability Evaluation of Base-Metal-Electrode Multilayer Ceramic Capacitors for Potential Space Applications," *CARTS Proceedings*, pp. 45, (2011)
3. D. Liu, "Failure modes in capacitors when tested under a time-varying stress," *CARTS proceedings*, pp. 210, (2011)
4. D. Liu and M. Sampson, "Some Aspects of the Failure Mechanisms in $BaTiO_3$-Based Multilayer Ceramic Capacitors," *CARTS Proceedings*, pp. 59, (2012) (*CARTS Outstanding Paper Award*)
5. D. Liu, "Highly Accelerated Life Stress Testing (HALST) of Base-Metal Electrode Multilayer Ceramic Capacitors," *CARTS proceeding*, pp. 235, (2013)
6. R. Weachock and D. Liu, "Failure Analysis of Dielectric Breakdowns in Base-Metal Electrode Multilayer Ceramic Capacitors," *CARTS Proceedings*, pp. 151, (2013)

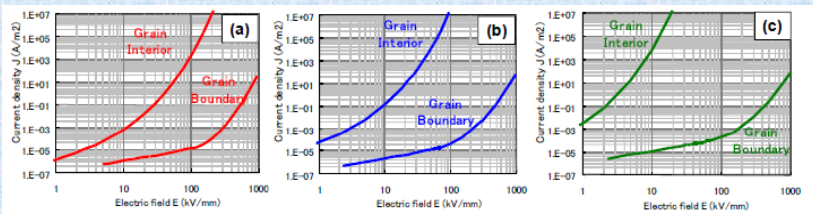
What Determines the Rated Voltage of a BME capacitor with X7R Dielectric?



Two basic facts about ferroelectric $BaTiO_3$ dielectrics

1. Inhomogeneity in resistance
   - For X7R dielectric with large grains, a core-shell structure is often reported due to the inhomogeneity between grain boundary and the bulk of the grain
   - For dielectric with small grain, the inhomogeneity in resistivity has been revealed, i.e., grain boundary always exhibits higher resistivity

What Determines the Rated Voltage of a BME capacitor with X7R Dielectric?



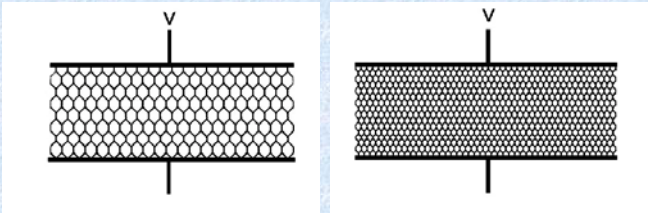
ICC3: Symposium 6: Advances in Electro Ceramics
IOP Conf. Series: Materials Science and Engineering **18** (2011) 092007

Two basic facts about ferroelectric $BaTiO_3$ dielectrics

1. Inhomogeneity in resistance
   - The applied voltage distribution is inhomogeneous
   - Due to the formation of a high **insulating** depletion layer at the grain boundary, most of the voltage will be applied on the grain boundary regime

- V/grain is one of the key parameters that determines the dielectric strength in the $BaTiO_3$ dielectric layer

What Determines the Rated Voltage of a BME capacitor with X7R Dielectric?



Two basic facts about ferroelectric $BaTiO_3$ dielectrics

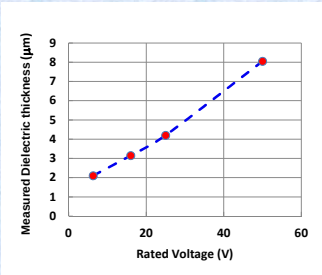
2. Impact of average grain size
   - When applied voltage and the dielectric thickness is identical for two capacitors, the one with smaller grain size has better electric strength
   - This is why smaller particles are always preferred for BME capacitors
   - The voltage per grain is lower for BME capacitor with smaller grains

$$Voltage\ per\ grain = \frac{V}{(d/r)}$$

key parameters that determines the dielectric strength in the $BaTiO_3$ dielectric layer

Voltage De-rating: An Engineering Approach

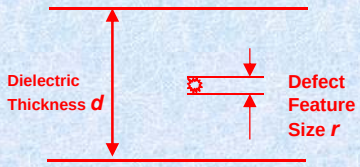
- Per MIL-PRF-123, all capacitors with Precious-Metal Electrode (PME) and X7R-type dielectric shall have a minimum dielectric thickness of 20 μm at 50V rating
- For BME capacitors with X7R dielectrics, an engineering chart for voltage de-rating was developed after cross-sectioning ~100 BME MLCC samples
- 50% voltage de-rating appears adequate
- Minimum dielectric thickness vs. rated voltage can be defined

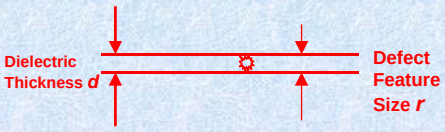


Technology	Rated voltage	Dielectric thickness *d* (μm) (Measured)	Grains per layer (Measured)	Voltage (V) at 50% de-rating/grains	Voltage (V)/grain	Minimum *d* after de-rating (μm)
PME	50V	20-22	22-28	25/(22-28)	1.14	17.6
BME	50V	7.5-10.2	23-25	25/(23-25)	1.09	9.8
BME	25V	3.4-4.6	12-13	12.5/(12-13)	1.04	4.2
BME	16V	2.5-3.5	9-10	8/(9-10)	0.89	3.2
BME	6.3V	2.0-2.2	6-7	3.2/(6-7)	0.53	2.1

Note: BME capacitors normally have better microstructures, i.e., smaller grain size and more uniform grain size distributions, and therefore they should have better V/grain

Voltage De-rating: An Alternative Approach





Dielectric layer reliability: $R_i(t) \to 1, when\ d \gg r; R_i(t) \to 0, when\ d \approx r.$

For Weibull model: $R(t) = e^{-\left(\frac{t}{\eta}\right)^{\beta}} \cdot \left[1 - \left(\frac{r}{d}\right)^{\xi}\right]$

Since: $r \approx c \times \bar{r}, \quad \bar{r}\ is\ the\ average\ grain\ size$

We have: $P = \left[1 - \left(\frac{r}{d}\right)^{\xi}\right] = \left[1 - \left(\frac{\bar{r}}{d}\right)^{\alpha}\right], \quad (\alpha \geq 5)$

***P* is a geometric factor that determines the dielectric reliability with respect to the microstructure of an MLCC.**

Voltage De-rating: An Alternative Approach (Cont'd)

With External Stress: $\eta(V,T) = \frac{C}{V^n} \cdot e^{-\frac{E_a}{kT}}$

We have: $R_i(t) = R_w(t) \cdot \left[1 - \left(\frac{\bar{r}}{d}\right)^{\alpha}\right] = e^{-\left[\frac{t}{C} V^n \cdot e^{\frac{E_a}{kT}}\right]^{\beta}} \cdot \left[1 - \left(\frac{\bar{r}}{d}\right)^{\alpha}\right], \alpha \geq 5$

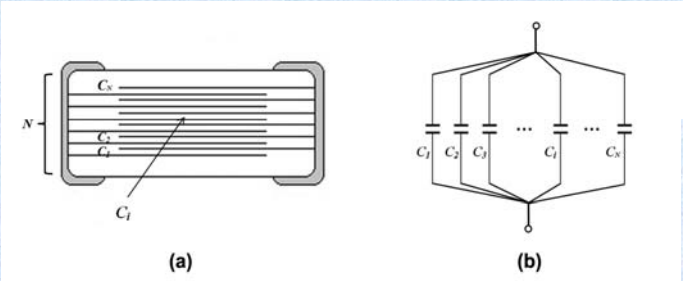
In many cases: $R_w(t \leq 10^3\ years) = e^{-\left[\frac{t}{C} V^n \cdot e^{\frac{E_a}{kT}}\right]^{\beta}} = 1$

So finally *a single layer dielectric reliability* can be simplified as:

$$R_i(t \leq \eta) \approx \left[1 - \left(\frac{\bar{r}}{d}\right)^{\alpha}\right]$$

***α* is an empirical constant that depends on the processing conditions and microstructure of a ceramic capacitor.**
α ≈ 6 (V ≤ 50) and α ≈ 5 (V >50) For BME MLCCs
α ≈ 5 for most PME MLCCs

Reliability: From a Single Dielectric Layer to an MLCC Device?

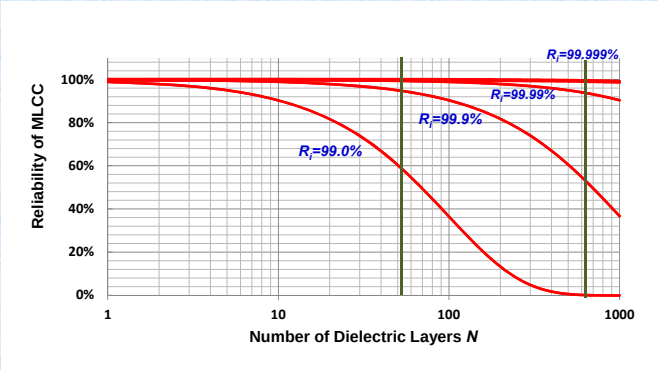


Total capacitance: $C_t = C_1 + C_2 + C_3 \ldots + C_i \ldots + C_N = N \cdot C_i$

Total reliability: $R_t = R_1 \times R_2 \times R_3 \ldots \times R_i \ldots \times R_N = R_i^N$

$R_i(t)$: Single dielectric layer reliability, as discussed earlier

Impact of number of dielectric layers: From Single Layer To Multilayer



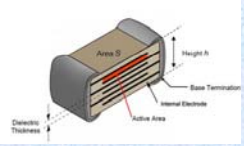
- The reliability of an MLCC R_t decreases with increasing N
- The value of N can be as high as 1000!

$$R_t(t \le \eta) = R_i(t)^N = \left[1 - \left(\frac{\bar{r}}{d}\right)^{\alpha}\right]^N, \quad (\alpha \ge 5)$$

MLCC Reliability: Impact of the Chip Size

Chip Size	Length (μm)	Width (μm)	Terminal-t (μm)	Side margin (μm)	End margin (μm)	Effective area (mm^2)	Chip size scaling factor
0402	1000 ± 100	500 ± 100	250 ± 150	125	100	0.225	1.00
0603	1600 ± 150	810 ± 150	350 ± 150	175	100	0.763	3.39
0805	2010 ± 200	1250 ± 200	500 ± 200	250	150	1.520	6.76
1206	3200 ± 200	1600 ± 200	500 ± 200	250	150	3.510	15.60
1210	3200 ± 200	2500 ± 200	500 ± 200	250	150	5.940	26.40
1812	4500 ± 300	3200 ± 200	610 ± 300	300	200	10.920	48.53
2220	5700 ± 400	5000 ± 400	640 ± 390	320	220	23.074	102.55
1825	4500 ± 300	6400 ± 400	610 ± 360	300	220	23.244	103.31

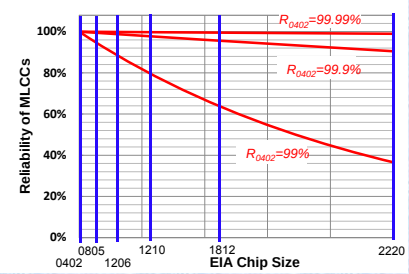
- Effective chip size 0805 is equal to 6.76 times 0402 MLCCs connected in parallel
- Reliability: $R_{0805} = R_{0402}^{6.76}$
- In general: $R_{xy} = R_{0402}^{S}$

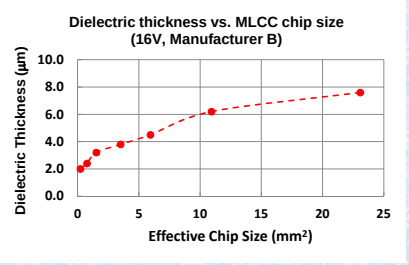


- Where ***S*** is the MLCC *chip size scaling* factor with respect to the chip size of an 0402 MLCC; *xy* is the EIA chip size

MLCC Reliability: Impact of the Chip Size (Cont'd)

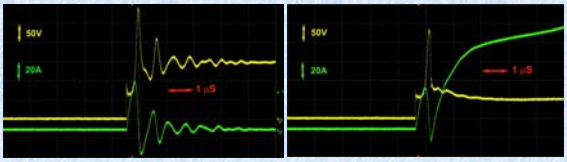
- The reliability of MLCCs decreases with increasing chip size, but not significantly
- When the chip *size scaling factor* increases by a hundredfold, the reliability declines:
  - 45% when R_{0402} = *99%*
  - 10% when R_{0402} = 99.9%
  - 1% when R_{0402} = 99.99%
- On the other hand, the dielectric thickness also gradually increases with MLCC chip size
- Since the reliability of an MLCC roughly follows a power-law increase with increasing dielectric thickness, the reliability decreases due to increasing chip size have been fully "compensated"
- Chip size has not been a concern with respect to MLCC reliability. GIDEP only has two examples for chip size-related failures with thin dielectrics (CKR06) and exceptional ratios of chip length and width (CDR02).
- *Aspect ratio is the KEY.* The same design rule applies to CMOS gate capacitors.





Robustness to Surge Test for BME Capacitors

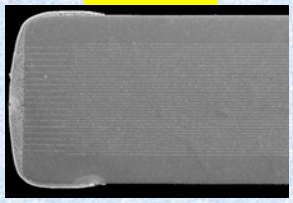
- A NEPP-funded study on BME capacitors under extreme surge conditions (more than 100%) revealed that the BME capacitor is one of a few capacitor products that exhibit superior performance for surge robustness
- The surge breakdown voltage is at least 10 times that of the rated voltage for BME capacitors and 5 times that for PME capacitors
- The difference can be well understood due to the microstructure and construction of BME capacitors

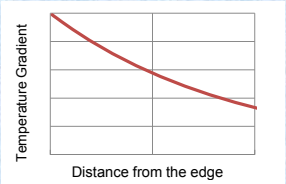


Capacitor ID	Rated Voltage (V)	Cathode/Electrode Structures	$V_{br}(100ppm)/V_{rated}$	$V_{br}(100ppm)$
Ta #1	10.0	Solid Ta, Fused	0.49	4.9
Ta #2	4.0	Solid Ta (MnO_2)	0.48	1.92
Ta #3	6.0	Ta Polymer	0.57	3.42
Al #1	6.3	Al Polymer/Stacked	1.46	9.20
Al #2	6.3	Al Polymer/Stacked	1.58	9.95
Al #3	12	Al Polymer/Stacked	1.25	15.00
Al #4	6.3	Al Polymer/Stacked	1.79	11.28
Al #5	6.3	Al Polymer/Wound	1.22	7.69
Al #6	4.0	Al Polymer/Laminated	1.83	7.32
Al #7	2.0	Al Polymer/Laminated	2.27	4.54
CC-1	6.3	Ceramic/BME	12.81	80.70
CC-2	6.3	Ceramic/BME	17.03	107.28
CC-3	6.3	Ceramic/BME	10.14	63.86
CC-4	6.3	Ceramic/BME	13.67	86.12
CC-5	6.3	Ceramic/BME	13.89	87.52
CC-6	5.0	Ceramic/PME	5.30	26.50
CC-7	6.3	Ceramic/BME	18.98	119.60

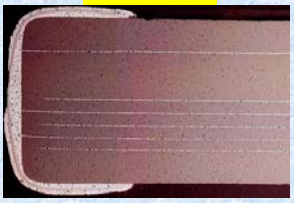
Impact of AC Ripple Current: A Thermal Structure Issue

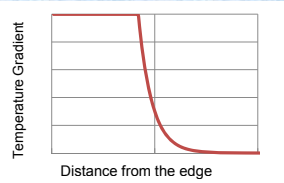
BME MLCC





PME MLCC

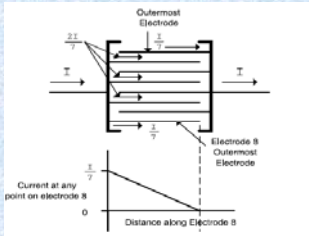


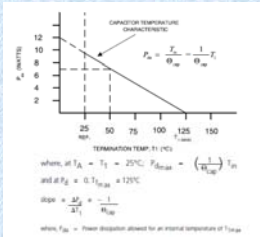


- PMEs with the lower capacitance values of a given chip size (same dielectric and voltage rating) have fewer electrode plates than BMEs with the same chip size and higher capacitance ratings.
- These electrode plates act as heat extractors (heat sinks) into the thermally resistive ceramic block.
- The more plates into that ceramic block, the more easily heat can flow out of the block.

Impact of AC Ripple Current: A Classic Model

A well-studied thermal model for MLCCs by F. M. Schabauer and R. Blumkin, at American Technical Ceramics, RF Design, May 1981





- Ripple current creates a potential local temperature gradient. A thermal structure was built for MLCCs that allows the theoretical determination of the temperature rise of an MLCC due to AC current flowing through it. The model has also been used for soldering heat flow simulations.
- Application notes to circuit designers for MLCC power rating. Many suppliers provide free software for ripple current estimation.
  - The temperature rise (ΔT) caused by the ripple current should not exceed 20°C above the ambient temperature of the capacitor.
  - Vp-p value and Vo-p value, including DC bias for the applied voltage, must be within the rated voltage (DC).
  - The maximum operating temperature 110ºC), including the amount of self-generated heat, should not be exceeded.
- There have been no MIL specifications required for ripple current testing of PME MLCCs in the last 30 years. *MIL specifications are even less likely to be required for BME capacitors.*

A General Expression of Reliability for MLCCs

$$R(t) = \varphi(N, d, \bar{r}, S) \times AF(V, T) \times \gamma(t)$$

$\gamma(t)$: Statistical distribution that describes the individual variation of properties (Weibull, log normal, normal)

$AF(V,T)$: A function that responds to the external stresses (independent of individual units)

$\varphi(N, d, \bar{a}, S)$: Impacts due to the characteristics of a capacitor device (structure, construction, etc.)

For PME MLCCs: $\varphi(N, d, \bar{r}, S) = 1$

Min. dielectric thickness per MIL-PRF-123
Microstructure has shown no impact on reliability

$$AF(V,T) = \frac{t_1}{t_2} = \left(\frac{E_2}{E_1}\right)^n \left(e^{\frac{E_a}{k}\left(\frac{1}{T_1} - \frac{1}{T_2}\right)}\right)$$

Well-known *Propokowicz-Vaskas equation* valid for most PME capacitors(n~3, E_a~1-2 eV)
-Inverse power-law for external field
-Arrhenius relation for temperature

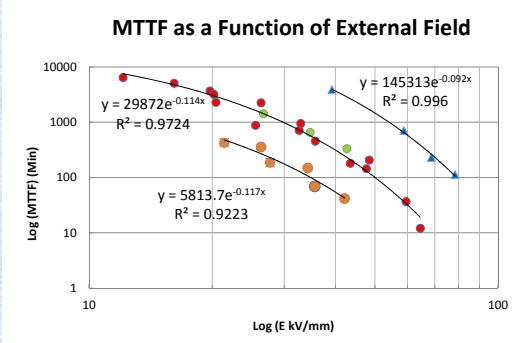
$$\gamma(t) = e^{-\left(\frac{t}{\eta}\right)^{\beta}}$$

Time-to-failure (TTF) distribution follows Weibull

Established model fits and has ensured the reliability of PME capacitors for >30 years!

Accelerating Function Does Not Always Follow Power-Law in BME MLCCs

- Accelerating function for BME capacitors has been found to be more complicated
- Three models have been proposed, depending on the external electric field strength
- *To be evaluated*



$$AF(V,T) = \frac{t_1}{t_2} = e^{(-b(E_1-E_2))} \times \left(e^{\frac{E_a}{K}\left(\frac{1}{T_1}-\frac{1}{T_2}\right)}\right)$$

Less Aggressive: E-model at low electric stress

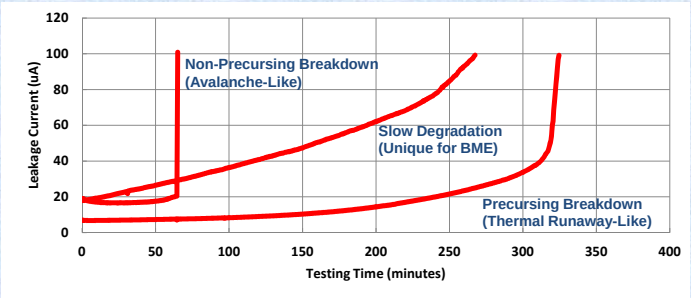
$$AF(V,T) = \frac{t_1}{t_2} = \left(\frac{E_2}{E_1}\right)^n \left(e^{\frac{E_a}{K}\left(\frac{1}{T_1}-\frac{1}{T_2}\right)}\right)$$

Most Aggressive: Inverse power-law in intermediate E -- Longest TFF data

$$AF(V,T) = \frac{t_1}{t_2} = e^{\left(-\frac{a}{k}\left(\frac{E_1}{T_1}-\frac{E_2}{T_2}\right)\right)} \times \left(e^{\frac{E_a}{K}\left(\frac{1}{T_1}-\frac{1}{T_2}\right)}\right)$$

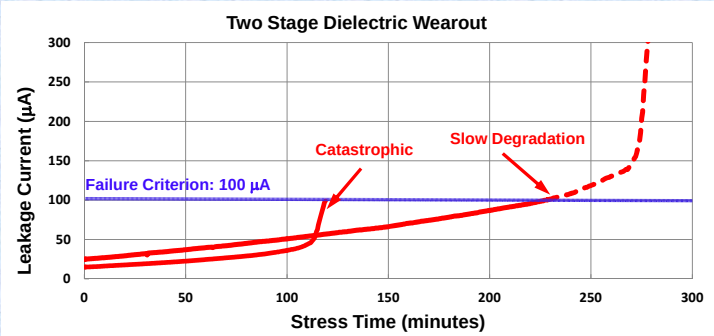
Least Aggressive: High field E model -- Shortest TTF data

Time-Dependent Dielectric Breakdown (TDDB): Failure Modes



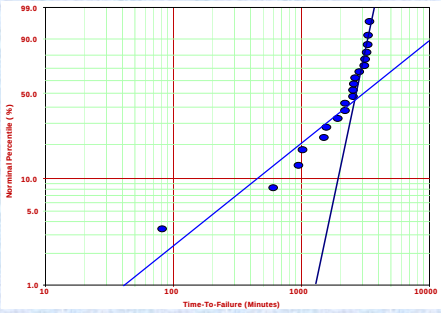
- **Avalanche-like and thermal runaway-like failure modes**
  - ***Avalanche***: catastrophic and rapid (in nanoseconds for SiO_2); no sign of breakdown
  - ***Thermal runaway***: local increase of leakage results in local temperature rise, which causes further leakage. A positive feedback loop is formed , causing a catastrophic failure (slower and more gradual leakage current increase prior to breakdown)
- These two failure patterns are hard to experimentally distinguish in BME MLCCs since any TDDB will involve some degree of thermal damage (avalanche-like breakdown is in the mini-second range for MLCCs -- very slow)
- The thermal conductivity and thermal diffusivity of $BaTiO_3$ ceramics are much less than that of SiO_2
  - Thermal conductivity (W/MK): SiO_2 = 149, $BaTiO_3$ = 2.86
  - Thermal diffusivity (mm^2/S): SiO_2 = 86, $BaTiO_3$ = 1.18

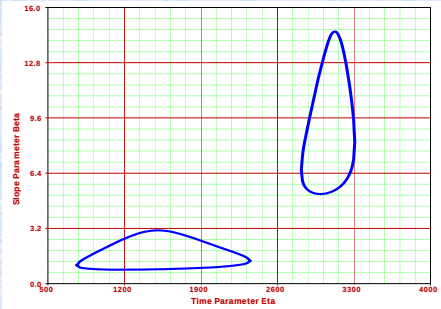
TDDB: Two-Stage Dielectric Wearout Failure Mode (Cont'd)



- It is more reasonable to consider the avalanche-like and thermal runaway-like failures as indistinguishable and to simply refer to these failures as catastrophic (*supported by FA results*)
- A two-stage dielectric wearout failure mode is better for describing the failure behavior in BME MLCCs with $BaTiO_3$-based X7R dielectrics
- Two-stage dielectric wearout: A slow degradation, characterized by a nearly linear leakage increase, followed by a time-accelerating catastrophic failure
  - *Slow degradation*: leakage increases with time nearly linearly due to oxygen vacancy migration until the failure criterion (100 µA) is reached (parts failed prior to catastrophic failures)
  - *Catastrophic failure*: leakage current increases gradually, followed by time-accelerating catastrophic failures

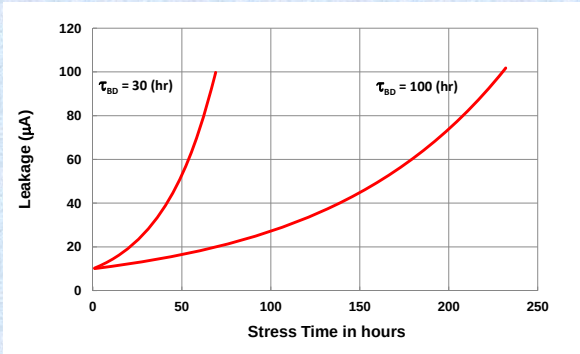
Weibull Modeling Results





- Weibull probability plot and corresponding contour plot clearly show the existence of two distinct failure modes!
- Although the two-stage failure behaviors may be attributed to a single dielectric wearout failure mode, statistically, they must be treated like two different failure modes: when processed for the slow degradation, the TTF data for catastrophic failures shall be considered suspensions, and vice versa

Understanding the Impact of τ_{SD} to MLCC Reliability



If we assume: $$\frac{I_2}{I_1} = e\left(\frac{t_2 - t_1}{\tau_{SD}}\right) = e\left(\frac{\Delta t}{\tau_{SD}}\right) = 2$$

Then we have: $$\tau_{SD} = \frac{\Delta t}{ln\,(2)} = 1.4427 \times \Delta t$$

Δt is the time that leakage current doubles in value

BME MLCC Guideline Development

- Selection of BME capacitors:
  - Eliminate BME capacitors that were developed for high volumetric efficiency applications
  - Distinguish NPO (C0G) and X7R dielectrics
- Procurement of "automotive" grade BME capacitors for high-reliability evaluations
  - Shoulder-to-shoulder comparison of AEC-Q200 and MIL-PRF-123, Table IX and EEE-INST-002
  - In-process qualification to MIL-PRF- 123, Table X
- Quality Conformance Inspection (QCI) to Groups A, B, and C of MIL-PRF-123
- A practical part list for BME capacitors
- Voltage de-rating: Contributions from microstructure and BME construction (engineering approach and alternative approach)
- A few words on humidity testing for BME capacitors
- Is ripple current testing really necessary for BME capacitors?

Selection of BME Capacitors

Inspection/Test	Test Methods, Conditions, and Requirements	Part Type/Level 1	2	3
1. Dielectric Type	The voltage temperature characteristic shall be referenced to the +25ºC value and shall be applicable over the entire temperature range of -55ºC to +125ºC. Dielectric type NPO (N) shall be 0±30 ppm/ ºC, and dielectric type X7R (X) shall be +15, -15%.	X	X	X
2. Destructive Physical Analysis (DPA)	Destructive physical analysis (pre-termination) shall be performed on each inspection lot of capacitors supplied to this specification. - DPA sample size shall follow MIL-PRF-123, Table XVII. - DPA shall be performed in accordance with the requirements of MIL-PRF-123, paragraph 4.6.1, except that paragraphs 3.4.1 and 3.4.2 shall be replaced with paragraph 2.3 herein. - Margin defects shall be determined using EIA 469, paragraph 5.1.3.	X	X	X
3. Microstructure Analysis	BME capacitors shall not be used for high-reliability space applications if the following construction and microstructure criteria are not satisfied	X	X	X
3.1. Nickel Electrodes	All BME capacitors shall use nickel for internal electrodes			
3.2. Capacitor Structure Parameter	The structure parameter of a BME ceramic capacitor *P* with respect to its microstructure and construction details can be expressed as: $P=[1-(\bar{a}/d)^{\alpha}]^{N}$ Where: d = Dielectric thickness that is the actual measured thickness of the fired ceramic dielectric layer. Voids, or the cumulative effect of voids, shall not reduce the total dielectric thickness by more than 50%. $\bar{a}$= Averaged ceramic grain size measured per the linear interception method. N = Number of individual dielectric layers. α= An empirical parameter that is applied voltage-dependent: α= 6 for V ≤ 50V, and α= 5 for V > 50V.			
3.3. Acceptance Criterion	The calculated *P* shall be greater than 99.999% for the X7R dielectric			
3.4. The minimum dielectric thickness	Greater than 3.0 micrometers for the NPO dielectric at V ≤ 50V and greater than 5.0 micrometers at V > 50V; *N* should be less than 300.			
4. Maximum dielectric constant	The maximum dielectric constant shall be 4000 for the X7R dielectric and 100 for the NPO dielectric.	X	X	X
5. Termination.	Devices supplied to this specification shall have a termination coating of copper, nickel, or their alloy, or shall be base-metal barrier tin-lead solder (MIL-PRF-123, type Z) plated. Tin-lead solder plating shall contain a minimum of 4% lead, by mass.	X	X	X

Qualification from AEC-Q200 to MIL-PRF-123

Items done per AEC-Q200

Stress	No.	Reference	Additional Requirements
Pre- and Post-Stress Electrical Test	1	User Spec.	Test is performed at 25±5°C except as specified in the applicable stress reference and the additional requirements in Table 2.
High Temperature Exposure (Storage)	3	MIL-STD-202 Method 108	Unpowered 1000 hours. Measurement at 24±4 hours after test conclusion. The maximum rated temperature should be employed for the dielectric used in the device.
Temperature Cycling	4	JESD22 Method JA-104	1000 Cycles (-55°C to +125°C) Measurement at 24±4 hours after test conclusion. 30min maximum dwell time at each temperature extreme. 1 min. maximum transition time.
Destructive Physical Analysis	5	EIA-469	Only applies to SMD Ceramics. Electrical Test not required.
Biased Humidity	7	MIL-STD-202 Method 103	1000 hours 85°C/85% RH. Note: Ceramics only - Specified conditions: Rated Voltage and 1.3 to 1.5 volts. Add 100Kohm resistor. Tantalums - Rated Voltage Only. Measurement at 24±4 hours after test conclusion. For ceramics that have silver content (e.g., PdAg electrodes), the low voltage portion of this test must also be performed.
Operational Life	8	MIL-STD-202 Method 108	Condition D Steady State T_A=125°C. 2/3 rated for Tantalum caps Full rated for Ceramic caps Measurement at 24±4 hours after test conclusion. The maximum rated temperature and voltage rating for the dielectric employed in the device shall be used.
External Visual	9	MIL-STD-883 Method 2009	Inspect device construction, marking and workmanship. Electrical Test not required
Physical Dimension	10	JESD22 Method JB-100	Verify physical dimensions to the applicable device specification. Note: User(s) and Suppliers spec. Electrical Test not required.
Terminal Strength (Leaded)	11	MIL-STD-202 Method 211	Test leaded device lead integrity only. Conditions: Ceramics: A (454 g), C (227 g), E (1.45 kg-mm). Tantalums: A (2.27 kg), C (227 g), E (1.45 kg-mm).
Resistance to Solvents	12	MIL-STD-202 Method 215	Note: It is applicable to marked and/or coated components. Add Aqueous wash chemical OKEMCLEAN (A 6% concentrated Oakite cleaner) or equivalent. Do not use banned solvents.
Mechanical Shock	13	MIL-STD-202 Method 213	Figure 1 of Method 213 SMD: Condition F LEADED: Condition C

Items not done per MIL-PRF-123

BME Capacitors Qualifications Inspection per MIL-PRF-123 Table IX

Inspection/Test	Test Methods, Conditions, and Requirements	Sample Size AEC-Q200	Sample Size MIL-PRF-123	EEE-INST-002 Part Type/Level 1	2	3
GROUP I						
1. Thermal Shock	MIL-STD-202, Method 107, Condition B, min. rated temp. to max. rated temp. (when specified in the product specification/ data sheet, the min. and max. "storage" temp. shall be used in lieu of the specified operating temp.)	N/A	182 (200)	X	X	
2. Voltage Conditioning (Burn-In)	4 x rated voltage, 125 °C, 160 hours (Level 1) 125 °C, 96 hours (Level 2) 125 °C, 48 hours (Level 3)	N/A	182 (200)	X	X	X
3. Electrical Measurements	As specified					
Capacitance	MIL-STD-202, Method 305	-	-	100%	100%	100%
Dissipation Factor	MIL-STD-202, Method 305(shall be 306)	100%	100%	100%	100%	100%
DWV	MIL-STD-202, Method 301	-	-	100%	100%	100%
Insulation Resistance	MIL-STD-202, Method 302	-	-	100%	100%	100%
Group II						
1. Visual and Mechanical Examination, material, design,construction and workmanship	Visual and sample-based mechanical inspection to be performed to requirements of applicable military specification	100%	15(1)	X	X	X
2. Destructive physical analysis	Destructive physical analysis shall be performed on each inspection lot of capacitors supplied to this specification. - DPA shall be performed in accordance with the requirements of MIL-PRF-123, paragraph 4.6.1, except that paragraphs 3.4.1 and 3.4.2 shall be replaced with paragraph 2.3 herein. - Margin defects shall be determined using EIA 469, paragraph 5.1.3.	10	15(1)	5(0)	3(0)	X
Group IIb - Nonleaded devices						
1. Terminal strength	AEC-Q200-006; MIL-STD-202, Method 211	30	12(1)	12(0)	12(1)	N/A
2. Solderability	MIL-STD-202, Method 208	15	12(1)	5(0)	3(0)	N/A
3. Resistance to soldering heat	MIL-STD-202, Method 210; condition C	30	12(1)	12(0)	12(1)	N/A

Qualification from AEC-Q200 to MIL-PRF-123 (Cont'd)

Items done per AEC-Q200

Stress	No.	Reference	Additional Requirements
Vibration	14	MIL-STD-202 Method 204	5g's for 20 min., 12 cycles each of 3 orientations Note: Use 8"X5" PCB .031" thick 7 secure points on one long side and 2 secure points at corners of opposite sides. Parts mounted within 2" from any secure point. Test from 10-2000 Hz.
Resistance to Soldering Heat	15	MIL-STD-202 Method 210	No pre-heat of samples. Note: Test condition D for SMD. Test condition B for Leaded. Pre-heat condition of 150ºC, 60-120sec is allowed for ceramic components.
ESD	17	AEC-Q200-002 or ISO/DIS 10605	
Solderability	18	J-STD-002	For both Leaded & SMD. Electrical Test not required. Magnification 50 X. Conditions: Leaded: Method A @ 235°C, category 3. SMD: a) Method B, 4 hrs @155°C dry heat @235°C b) Method B @ 215°C category 3. c) Method D category 3 @ 260°C.
Electrical Characterization	19	User Spec.	Parametrically test per lot and sample size requirements, summary to show Min, Max, Mean and Standard deviation at room as well as Min and Max operating temperatures. Parameters C, DF, IR at min / room / max temperatures to be measured at a minimum. SEE PARAMETER TABLE FOR SUGGESTIONS.
Board Flex	21	AEC-Q200-005	Required for MLCCs only. 60 sec minimum holding time.
Terminal Strength (SMD)	22	AEC-Q200-006	
Beam Load Test	23	AEC-Q200-003	Ceramics Only

Items not done per MIL-PRF-123

Inspection/Test	Test Methods, Conditions, and Requirements	Sample Size		EEE-INST-002 Part Type/Level		
		AEC-Q200	MIL-PRF-123	1	2	3
Group IV						
1. Voltage-temperature limits	Capacitance change over the range of temperatures and voltages specified shall not exceed limits of specification. NPO Capacitors shall be tested in accordance with MIL-PRF-123 BP characteristics.	N/A	12(1)	12(0)	12(1)	
2. Moisture resistance	MIL-STD-202, Method 106 20 cycles (first 10 cycles with Vrated applied) DWV, IR and DC to specification AEC-Q200-006 removed this test in version D	77	12(1)	12(0)	12(1)	N/A
Group V						
1. Humidity, steady state, low voltage	MIL-STD-202, Method 103, Condition A. AEC-Q200 Biased humidity. **Note:** 85/85 at rated voltage for 1000 hours per AEC-Q200 shall be applied for BME capacitors. The low voltage portion is not necessary for BME capacitors (See further explanations)	77	12(0)	12(0)	5(0)	N/A
2. Resistance to solvents	MIL-STD-202, Method 215	5	12(1)	N/A	N/A	N/A
Group VI						
Life	MIL-STD-202, Method 108 Ttest = maximum operating temperature Vtest = 2 X Vrated (**1X Vrated perAEC-Q200-006**) Duration: 2,000 hours for level 1, 1,000 hours for levels 2 and 3 IR, ΔC, and DF to specification	77	123(1)	44(0)	44(1)	N/A

- Many AEC-Q200 test results met and sometimes exceeded those of MIL-PRF-123, with some exceptions
- Big variations in the number of test samples (*TBD*)