

What Twenty Years of Solid-State Recorders Tells Us about the Next Twenty

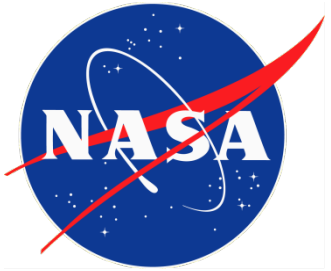
Ray Ladbury

Radiation Effects and Analysis Group

NASA Goddard Space Flight Center

To be presented by Ray Ladbury at the Single-Event Effects Symposium and Military and Aerospace Programmable Logic Devices (SEE-MAPLD), La Jolla, CA, April 9-12, 2013, and published on http://nepp.nasa.gov/.

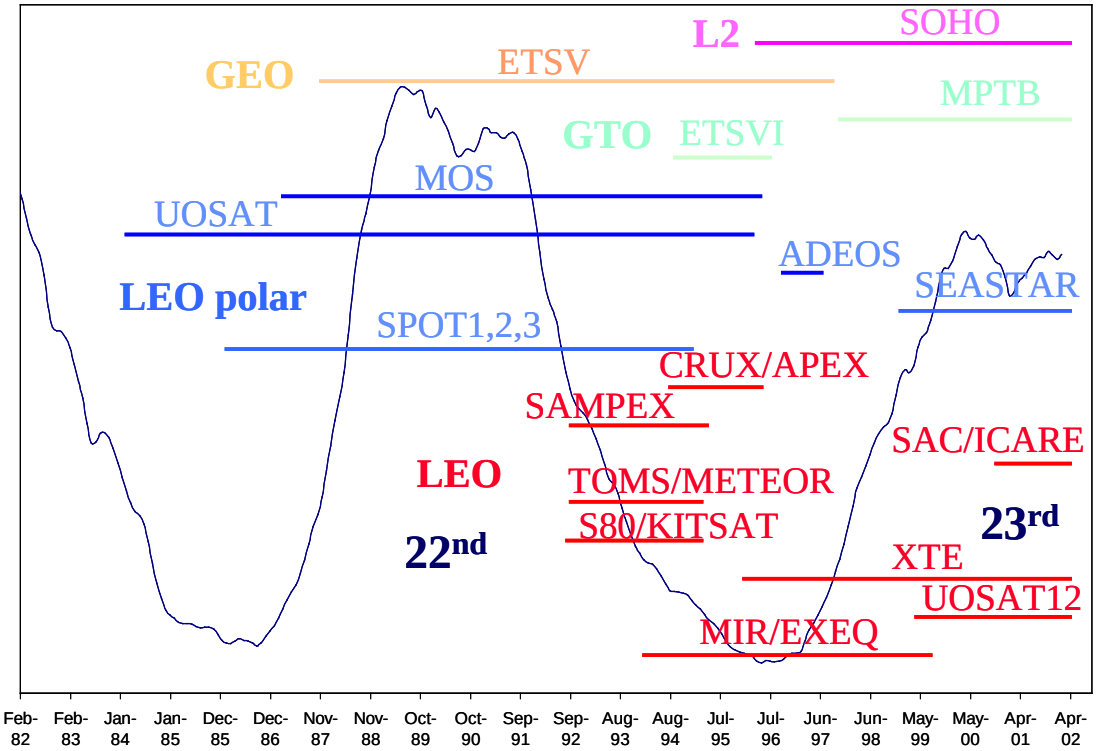
Why Study Solid-State Recorders?



- Solid-state recorders (SSRs) perform a critical mission function
  - Allow efficient data return and mission continuity when transfer impossible
- SSRs use very large amounts of commercial memory
  - Commercial memories have >30x density of radiation hardened memories
    - Now dominated by Synchronous Dynamic Random Access Memory (SDRAM)
  - Each SSR is an on-orbit test of up to thousands of state-of-the-art-memory die
    - Increases likelihood of seeing new or rare events and failure modes
    - May allow exploration of part-to-part- variation.
- Commercial memory chips have high sensitivity to single-event effects (SEE)
  - High sensitivity + high density→validate radiation-environment and SEE rate models
  - Ubiquity of SSRs allows comparison of operation in many environments
- Because SSRs use commercial memory, their technology changes rapidly
  - Do hardening techniques of the past still work?
  - Have new units operated as did their predecessors?
- Memory is the gateway drug for commercial electronics

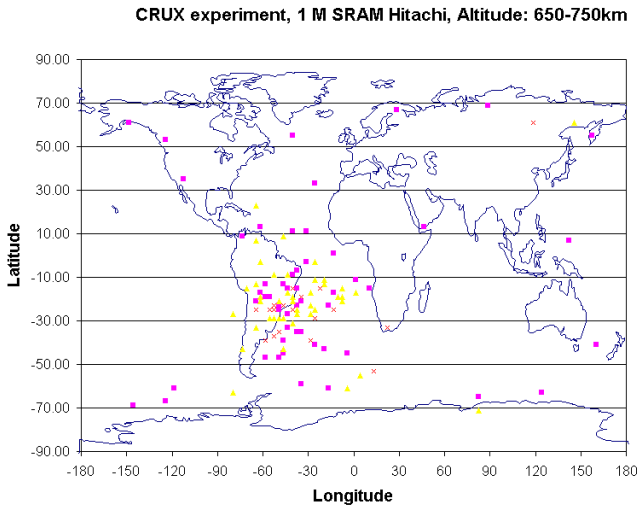
Missions for 2002 Study

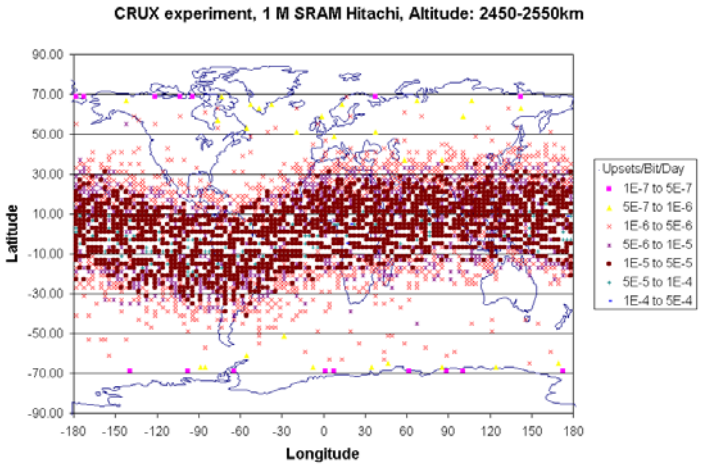
Original study done by Christian Poivey in 2002

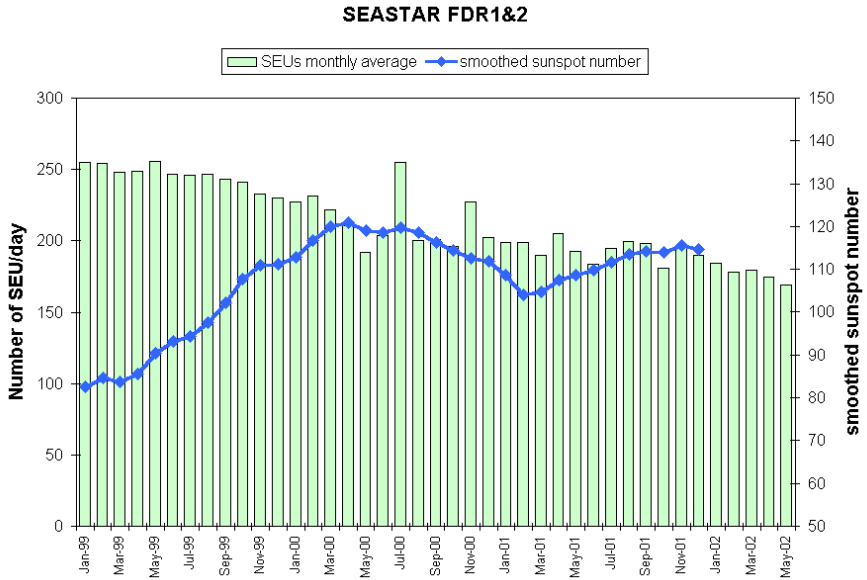


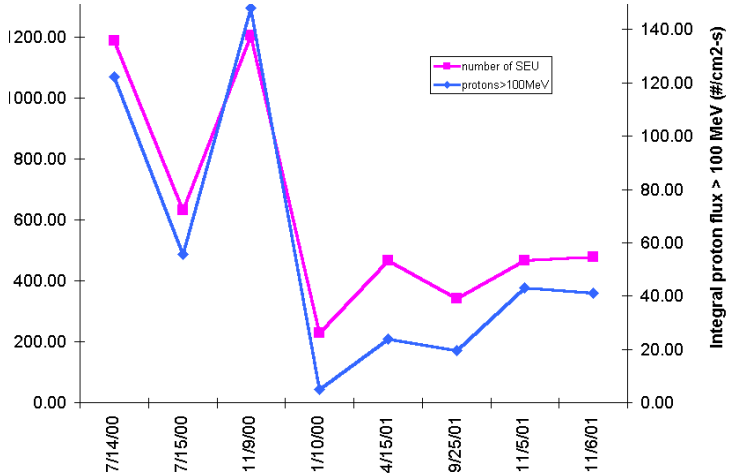
- Original study
  - >2 solar cycles
  - >60 missions/experiments
  - SRAM (up to 1 Mbit) (static random access memory)
  - DRAM (up to 16 Mbit)
- Update adds data for
  - Two published studies
  - 5 missions
  - 64-512 Mbit SDRAM Completes 24th Solar Cycle
  - Environments from low-Earth orbit (LEO) to interplanetary

Guideline 1: Know your Mission Environment

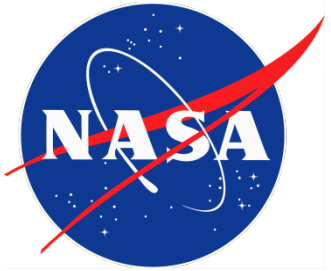








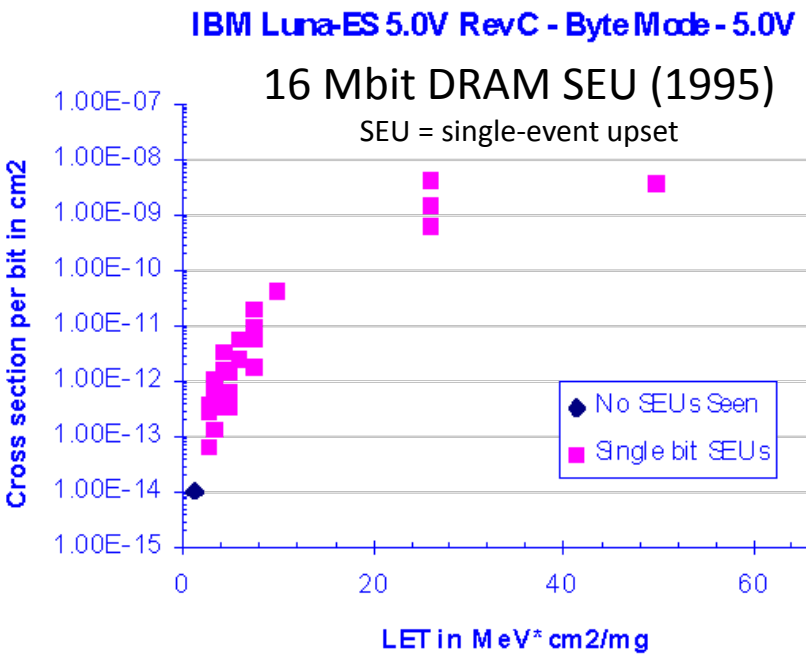
Guideline 2: Know Your Requirements

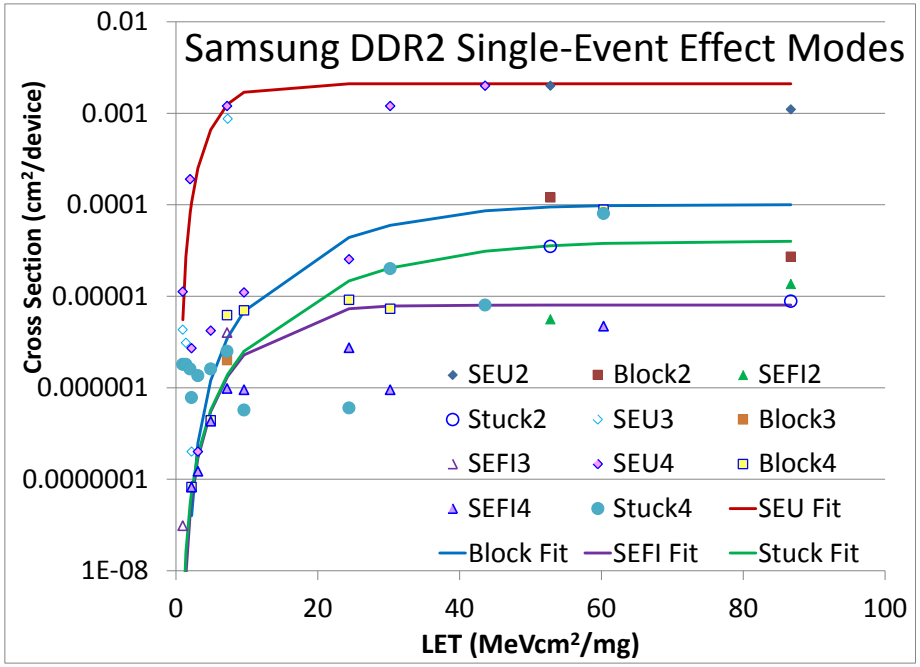


- Is application a 1 TB data recorder or a 10 Gbit scratchpad?
  - Error Detection and Correction (EDAC) options and available architectures (*e.g.*, for interleaving bits in data words) very different
- What is important?
  - Is bit-error rate really important for video data?
  - Do you care if <<1% of science frames are lost due to recoverable Single-Event Functional Interrupt (SEFI)?
  - If SEU are single-bit, and block errors are >100x rarer, is single-bit correction acceptable in lieu of double-bit correction?
  - How long does data stay in memory?
- What are the physical requirements?
  - Memory size, speed, physical dimensions, power consumption, etc.
- What are the performance requirements?

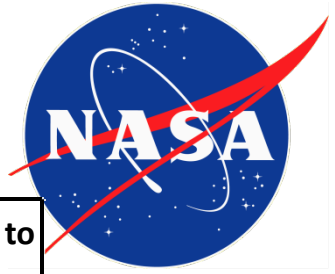
Guideline 3: Know Your Device SEE Response

- Is response simple or complex?
  - Does device exhibit nonrecoverable SEFIs, stuck bits, multi-bit errors?
    - Double Data Rate (DDR2) SDRAM much more complex than 16 Mbit DRAM
- How well are rates known?
  - How large are statistical errors (*e.g.*, Poisson fluctuations)?
  - How well is part-to-part and/or lot-to-lot variation bounded



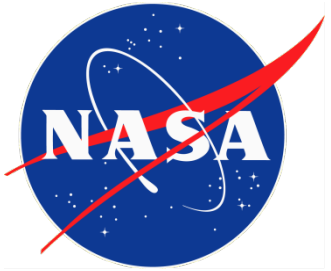


Guideline 4: Consequences & Remediation



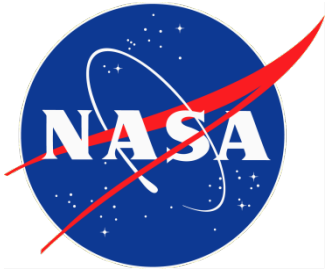
Radiation Risk	Consequence	Remediation	Impact to design
Destructive Single-Event Latchup (SEL)	Permanent loss of 1 die in memory array	Redundant die in array such that probability of meeting End-of-Life (EOL) requirements is high	Severe
Nondestructive SEL	Loss of all data on affected die/stack	Requires power cycle of affected die/stack for recovery	Moderate to severe
Single-Event Functional Interrupt (SEFI) requiring power cycle	Loss of functionality on affected die; Loss of most or all data on affected die/stacks	Requires power cycle of affected die/stack for recovery; EDAC may	Moderate to severe
Recoverable SEFI	Temporary loss of functionality; Loss of large amounts up to all data on affected die.	EDAC + Organzation of data words across independent die; FPGA programmed w/ ability to refresh mode registers/reset device	Moderate
Stuck Bits	Uncorrectable loss of data integrity in affected bits/symbols	EDAC can correct incorrect bit, but capability permanently degraded	Minor
Multi-Bit Upset (MBU)	Correctable loss of data for multiple bits in same word	EDAC must have sufficient power to correct w/c MBU (usually no worse than w/c SEFI)	Moderate
Multi-Cell SEU	Multiple bits upset, but in different words	EDAC	Minor
SEU	single-bit upset	EDAC	Minor

Guideline 5: Know Options for SSR Hardening



- SSR hardening relies on a multi-tiered approach
  - First line of defense is conservative SEE testing
    - Testing goal #1: Find a part with SEL rate as close to 0 as possible
    - Testing goal #2: Ensure rate for SEFI requiring power cycle as close to 0 as possible
    - Testing goal #3: Get sufficient data to BOUND rates for all SEE modes
    - Allow for part-to-part variation in SEE rates—estimate rates conservatively
  - Second tier is Error Detection and Correction (EDAC)
    - EDAC code calculates error correction bits from values of data bits and can detect and correct errors up to some maximum size if discrepancies are found.
    - Other mitigations needed to ensure worst-case error does not exceed EDAC capability
  - Other mitigations
    - Goal is to keep errors from overwhelming EDAC—either all at once or cumulative
    - Interleave words across multiple die (die width is a good "symbol" length), so that even if all bits on a single die corrupted, EDAC can still correct data words
    - Scrub entire SSR periodically so probability of errors accumulating in any period small
- For small memory applications interleaving may not be possible
  - Triplicate voting may be more efficient.

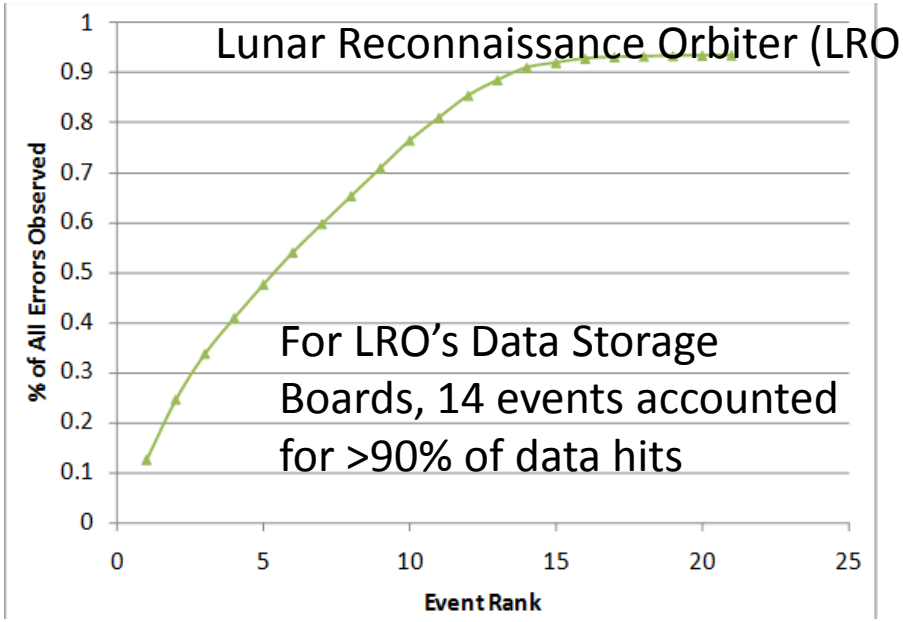
Guideline 6: These are Commercial Parts

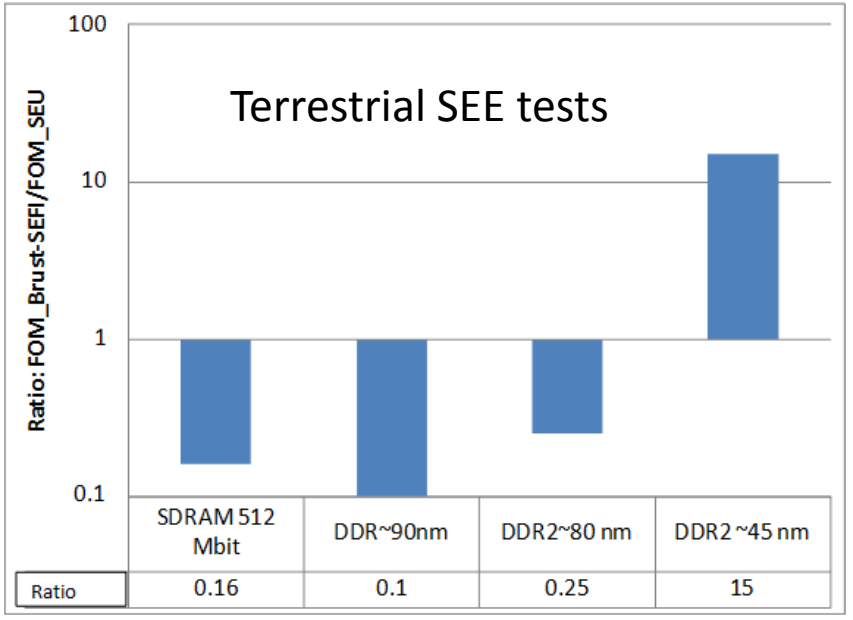


- Product life-cycles are short (~18 months)
  - Procuring test lot, radiation testing, qualification, etc. can leave little time to procure part before it becomes obsolete or is revised.
  - A revised part means starting all over again.
- Lot-traceability may not be possible
  - Need to ensure test sample is representative of flight parts some other way
  - Part-to-part variation in SEE response may be larger than for MIL or space parts
  - Threat of counterfeit parts is real unless source is trusted
- Commercial memories are too complicated to test completely
  - Cannot test all possible operating-mode combinations
  - Parts exhibit a variety of disruptive error modes (e.g. SEFI, SEL)
  - Lack of traceability means should test larger sample; may not be possible
- These factors argue for significant margin when estimating SEE rates
  - Needs to be remembered by designer as well as SEE analyst—if rate drives design and increases cost, pushing back may be fruitful

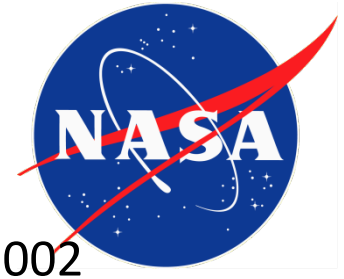
Changes Since 2002 I: Memories

- SEL performance has been variable, but improved since 2008
- SEU—per bit SEU rates remain very low (~10^{-12}-10^{-11} per bit day)
- Multi-bit upsets usually due to control logic or read errors due to interleaving
- Stuck bits have been manageable (<10^{-5} per device day)
- SEFIs and block errors have accounted for increasing proportion of errors
  - Large blocks of multibit errors increase importance of powerful EDAC





Changes Since 2002 II: Recorders

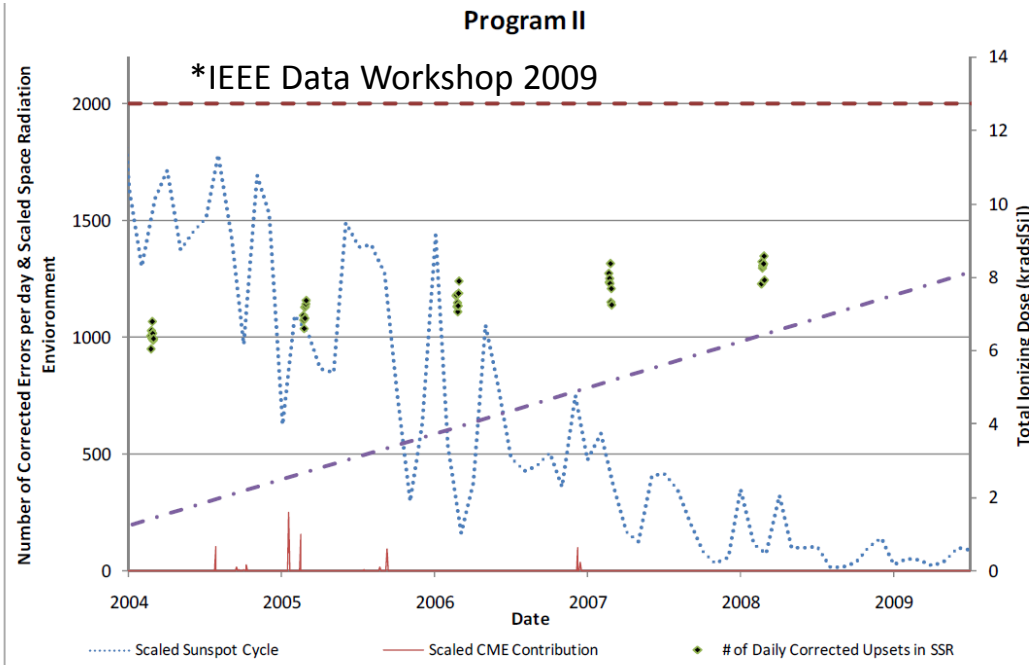


- SDRAMs have dominated bulk data storage applications since 2002
  - Most SSRs have used Elpida 256 Mbit or 512 Mbit SDRAM
  - First DDR devices flown in 2013 (Delay-Locked Loop (DLL) disabled)
- Data words are larger—increased from 16 bits to 32 bits
  - Encourages use of wider SDRAMs, requiring more powerful EDAC or degrading margins
- DRAM die often stacked 4-8 in a package to save board real estate
  - Since die share a common power supply, cannot cycle power to individual die
    - If SEFI or nondestructive SEL require power cycle all data on stack lost.
    - Note that use of FLASH or other nonvolatile eliminates this problem
- Mitigation has become more sophisticated
  - Greater symbol/word width favors multi-symbol error correction
  - SEFI requiring a power cycle for recovery favor sparser interleaving
- Recorder performance
  - Most recorders cannot utilize full speed of DDR2/3 devices.
  - Mitigations available continue to be effective—no data lost in studies reviewed

Changes Since 2002 III: Flight Data

Only 2 published studies comparing on-orbit and predicted SEE rates

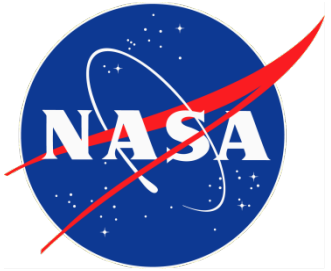
- Schaefer et al.* Looked at SEU in 64, 128 & 256 Mbit SDRAMs
  - Space weather effects difficult to discern
  - Effect of solar cycle evident
  - Predicted:Observed varies from 1.26-10.2
  - No trend with technology



- GSFC looked at data storage boards (DSB) for LRO
  - Elpida 512 Mbit SDRAM
  - >90% of errors occurred in Block errors
  - Predicted SEU rate ~6x observed—estimated with good statistics
  - Poor Statistics for SEFI and block errors, so prediction overestimates rate >100x
  - CREME96 estimates rates adequately up to 512 Mbit generation

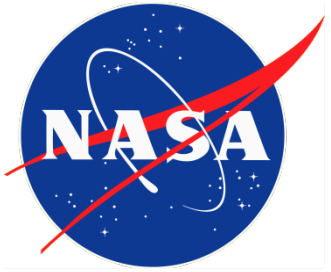
Error Mode	Predicted #/dev-day	Observed #/dev-day
SEU	1.54E-02	3.10E-03
Logic Errors	1.00E-02	1.70E-04
Block Errors	3.50E-03	3.30E-05
SEFI	<0.000008	<6.4E-6
Stuck bits (permanent)		<1E-5

SSRs of The Future



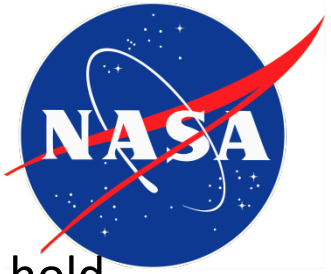
- Near future will use DDR2/3/4
  - 2-4 Gbit die, >2 GHz operation possible
  - Challenges
    - Too fast for radiation hardened controllers—can run <100 MHz w/ DLL disabled
    - Increased width of part and word length may require sophisticated EDAC
    - Common VDD of stacked die make recovery from SEFI more challenging
- Improved endurance, retention, TID and SEE performance make FLASH viable
  - Nonvolatile storage a significant advantage and >density than SDRAMs
  - Challenges
    - Too slow for many applications
    - Page Erase and other operational characteristics inconvenient in some applications
    - Susceptible to hard SEE failure during Write and Erase operations
- Whatever comes next???
  - Nonvolatile—top candidates are resistive RAM & Spin-Torque Transfer RAM
    - Hope: >DDR4 speed, >FLASH density, memory cell likely hard to SEE
    - Challenges will come from support/control circuitry

Additional Guidelines And Advice



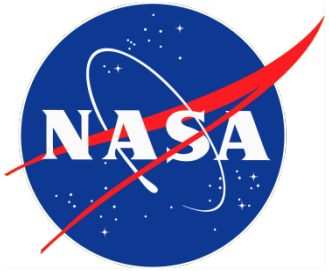
- Guidelines and hardening techniques from 2002 still hold well
- Additional trends worth noting
  - Continued consolidation of commercial memory manufacturers
    - Limits choices and adds another risk for procurement
  - Increasing prevalence of SEFI/block errors vs. SEU
    - Some applications may get by with limited EDAC
    - Some may really need multi-symbol correction
    - Need to understanding application and conservatism of rate estimates
      - SEFI very disruptive to testing, so rates estimated with poor statistics
  - Increasing complexity of memory makes every test application specific
    - Need to understand application if test is to be valid
  - For DDR2/3, SEU cross section does not scale with effective LET
    - Introduces more uncertainty into rate estimation
    - SEFI/ block errors still scale, but estimation poor due to poor statistics

Conclusions



- Conventional Guidelines and hardening techniques for SSRs still hold
  - Although parts have changed—they are still commercial and subject to same market forces and risks
  - Hardening techniques work because they address consequences of SEE modes
    - Permanent failure of entire part (e.g. single-event latchup, burnout)
    - Permanent partial failure of part (e.g. stuck bit)
    - Unrecoverable loss of functionality requiring power cycle (SEFI)
    - Large blocks of data lost (block error)
    - Small amount of data lost (single-event upset)
    - Effects of any single error confined to a single die
    - Usually ensure at least 1 worst-case error correctable (data loss + functionality)
- Trends such as stacking, wider part and longer data words pose challenges
  - Hardening techniques can be adapted to ensure data remain secure
- Hardening will also work for any new technologies that come along

Acknowledgements



- The author thanks the NASA Electronic Parts and Packaging (NEPP) Program for support of this work, the Lunar Reconnaissance Orbiter for data and Ken LaBel for helpful discussions