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Special Issue

CGA Assemblies under Thermal Cycling

Column-grid arrays (CGAs) have drawn much recent attention. These packages do not always come with column attachment; the article discusses CGAs with two column styles. NASA does not recommend any particular provider of column attachments. The users should make their own determination of which provider to use. This special issue of the *EEE Parts Bulletin* was written by Dr. Reza Ghaffarian, a packaging specialist at Jet Propulsion Laboratory.

ABSTRACT

Commercial-off-the-shelf column grid array packaging (COTS CGA) technologies in high-reliability versions are now being considered for use in electronic systems. For space applications, these packages are prone to early failure due to the severe thermal cycling in ground testing and during flight, mechanical shock and vibration of launch, and other less severe conditions, such as mechanical loading during descent, rough terrain mobility, handling, and ground tests. As the density of these packages increases and the size of solder interconnections decreases, susceptibility to thermal loading, mechanical loading, and cycling fatigue grows even more. This article presents an overview of area array technology trends and key factors affecting damage and failure under thermal cycling conditions. Examples of failure of CGA assemblies under thermal cycling with both pure solder columns and copper wrapped columns are presented. Also, industry has released a number of specifications in response to the current needs of electronics rapid growth in commercial applications (especially for mobile use), and a brief discussion on this topic is also provided. Understanding key reliability factors will facilitate use of newly available very dense field-programmable gate array (FPGA) packages by defining reliability risks and mitigation approaches.

BACKGROUND

Area array packages such as ball-grid arrays (BGAs) and chip scale (size) packages (CSPs) are now widely used for many commercial electronics applications, including portable and telecommunication products. The CGA versions are now being considered for high-reliability applications with generally much harsher thermal and mechanical cycling requirements than those for commercial use [1-4]. Technical challenges for BGA/CSP packages, such as the behavior of solder joints under thermal and mechanical loading, have become a “moving target” to meet development requirements for higher density die with their associated continuous increase in pin count input/output (I/O), decrease in pitches, and newly introduced packaging styles (including stack technology).

Solders in surface mount technology (SMT) are unique because they provide both electrical interconnection and mechanical load-bearing elements for attachment of packages on a printed circuit board (PCB). Damage and failures have meaning only in the context of interconnections since a solder joint in isolation is neither reliable nor unreliable. Failures are induced either within the package or external to the package on a PCB. Solder joints are a key interface element that can cause damage progression and eventual failures including in CGA packages and assemblies. Figure 1 illustrates trends for area array packages including CGAs.

This moving target of advanced electronic packaging (including CGA) becomes extremely challenging for high-reliability applications. Unlike many early microelectronic technologies that aimed mostly at meeting applications for high-reliability and ruggedness; consumer electronics is now driving the trends for electronic packaging and assembly. With that being the primary driver, materials and processes are transitioning to lead-free (Pb-free) solder alloy in order to enforce restrictions on hazardous substances (ROHS) for commercial electronics systems.

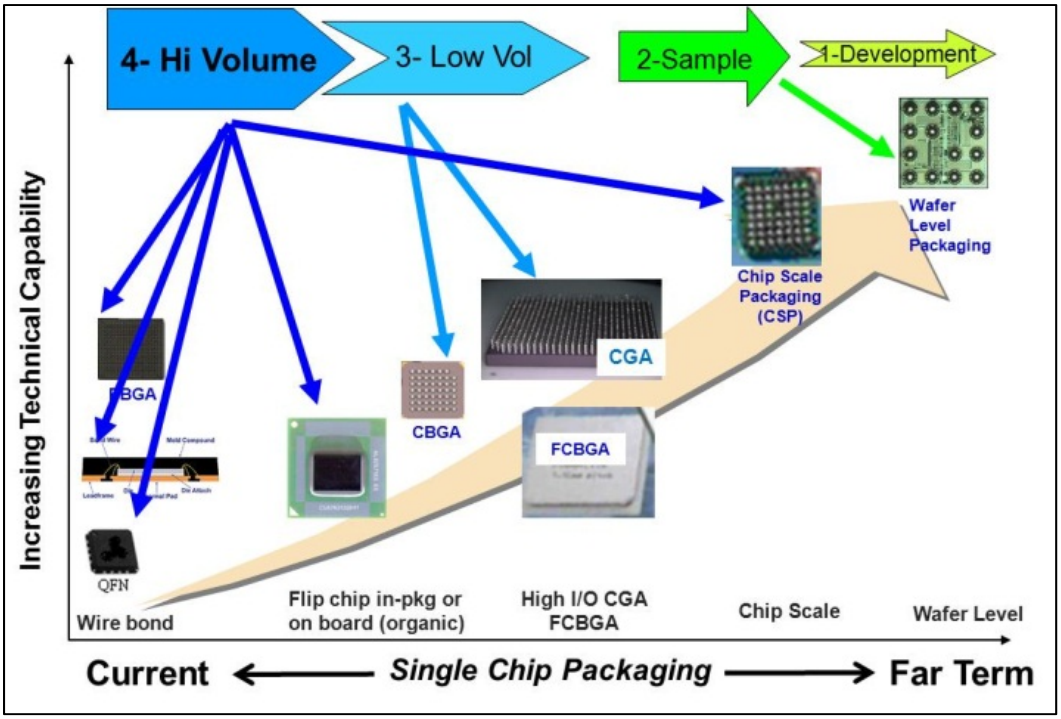

Figure 1. Microelectronic trends for single packaging technologies. (FCBGA = flip chip ball grid array; QFN = quad flat no lead)

While there is a drive to develop new low dielectric constant (low-k) dielectrics and advanced organic substrate materials, the higher melting temperatures of these solder alloys are pushing the limits of their reliability. For high reliability, industry now uses specialty electronics, along with either adapted consumer electronics or specifically tailored versions.

For example, for CGAs under thermal cycling conditions (see Figure 2), three elements play key roles in defining damage progression and reliability: global, local, and solder alloy deformation. In CGAs, solder columns also act as loadbearing elements between the package and the board in a fashion similar to metallic leads such as those for a ceramic quad flat pack (CQFP). The characteristics of these three elements — package (e.g., die, substrate, solder joint, and underfill), PCB (e.g., polymer, copper, plated through hole, microvia), and solder joints (e.g., via balls or columns) — together with the use conditions (the design life and acceptance failure probability for the electronic assembly) determine the reliability of CGA assemblies.

DAMAGE/FAILURES UNDER THERMAL CYCLING

The elements of system microelectronics reliability under static/cycling/dynamic thermal and mechanical loadings are the device, the package, the PCB, and their interconnections along with consideration of design for reliability prior to assembly and subsequent manufacturing, as well as quality assurance implementation. Premature failures may also occur due to workmanship defects and the lack of sound manufacturing and design for reliability. These could confound the reliability test results in the early product development. Damage due to stresses induced at various steps of manufacturing, testing, and environmental exposures, and during application, can cause failures due to thermal and mechanical overloading or wear-out mechanisms during fatigue cycles. Stress induced during the packaging process could cause cracking of the die and package or failures of interconnections due to overloading. Conversely, lower loading could cause fatigue failures due to repeated thermal cycling or mechanical loading exposures. Physics-of-failure for each case is different, and in some cases they may contradict each other.

The majority of fatigue failures of solder joints in surface mount assemblies are due to global coefficients of thermal expansion (CTE) mismatch induced damage, while early failure may be due to workmanship anomalies and local interfacial integrity deficiencies [5]. The global expansion mismatches result from differential thermal expansions of a package and the PCB assembly. These thermal expansion differences stem from differences in the CTEs and thermal gradients as the result of heat dissipation from functional die within package. Global CTE-mismatches typically range from $\Delta\alpha$~2 ppm/°C (2×10^{-6}) for CTE-tailored high reliability assemblies to $\Delta\alpha$ ~14 ppm/°C for ceramic packages (e.g., CGA) on FR-4 PCBs. The shear strain (γ) representative of the global CTE mismatch due to thermal excursion is given as the following.

$$\gamma = (\alpha_C - \alpha_S)\,(T_c - T_0)\,L/H = (\Delta\alpha)\,(\Delta T)\,L_D/H \qquad (1)$$

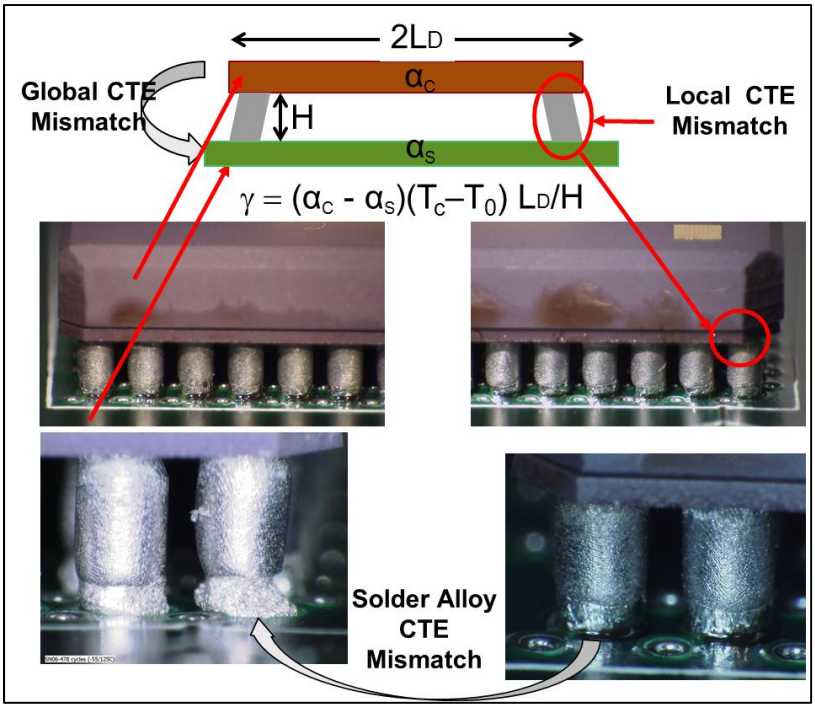

Figure 2. Three key elements that define reliability under thermal stress are global, local, and solder alloy deformation. (Equation terms defined under Equation 1.)

Global CTE mismatches typically are the largest, since all three parameters determining the thermal expansion mismatch, i.e., the CTE-mismatch ($\Delta\alpha = \alpha_C - \alpha_S$), the temperature swing ($\Delta T = T_c - T_0$), and the largest acting package length (L_D), also known as distance to neutral point (DNP), can be large. In thermal cycling, this global expansion mismatch causes cyclical stress, and thus fatigue on the solder joints. The cumulative fatigue damage can ultimately cause the failure of one of the solder joints (typically a corner joint in a CGA) causing permanent functional electrical failure that initially may be intermittent. The shear strain representing damage in each cycle is proportional to $\Delta\alpha$, ΔT, and L_D, and is inversely proportional to the package/PCB separation height (H). For this reason CGAs are selected for higher package sizes and I/Os since thermal strain is lower for higher column height (H) than for their CBGA counterparts; therefore, it is expected to show better thermal cycling fatigue life.

The local expansion mismatch results from differential thermal expansions of the solder and the base material of the package or PCB assembly. These thermal expansion differences result from differences in the CTE of the solder and those of the base materials together with thermal excursions. Local CTE-mismatches (e.g., solder alloy/copper pad) typically range from $\Delta\alpha$ ~7 ppm/°C with copper to ~18 ppm/°C with ceramic. Local CTE mismatches typically are smaller than the global expansion mismatches, since the acting distance, the maximum wetted area dimension, is much smaller (on the order of tens of mils, e.g., 20 mils (0.5 mm) for a typical column diameter).

At the micro-level, solder alloy CTE mismatches cover microstructural changes due to solder alloy being a mixture of two or more elements or grains with different characteristics. The grain structure of tin–lead solder is inherently unstable. The grains will grow in size over time as the grain structure reduces the internal energy of a fine-grained structure formed during SMT cooling. This grain growth process is increased by exposures at elevated temperatures as well as strain energy input during cyclic loading. The grain growth process is thus an indication of the accumulating thermal fatigue damage increasing with increasing maximum temperature and dwell time.

Figure 3 shows optical photomicrographs of a cross-sectioned CGA 717 I/O assembly after thermal cycling. The column type is copper-wrapped solder column with about 20-mil diameter. It clearly shows signs of cracking; the cracks penetrated to a maximum of about 50% of the pad diameter. Such cracks could progress to failure.

Figure 4 shows cross-sectional optical photomicrographs for a CGA 1144 I/O package assembly after thermal cycling. This package has high-lead solder (tin–lead alloy) columns, which show different responses to thermal cycling than copper-wrapped columns. At the top is a photomicrograph from the package section revealing a flip chip die attach configuration with internal solder balls. The center photomicrographs clearly show that columns at the package corners are tilted away from package center the package center. Without copper wrap for stabilization, significant tilt occurs due to the higher CTE mismatch of the corner solder joints, especially because they are at the farthest distances from the package neutral point. There is also evidence of cracks, although the crack lengths were less than 50% of the pad diameter.

DAMAGE/FAILURES DUE TO MECHANICAL LOADING

Figure 5 presents schematically key damage and failures under thermal and mechanical loading, with an emphasis on mechanical loading and failures. Area array packages, in general, and CGA/FCBGA specifically, lack thermal and mechanical resistance generally observed for plated through hole (PTH) and leaded package assemblies soldered with Sn37Pb alloys. Lack of thermal/mechanical resistance is further aggravated with the use of Pb-free solder alloys, especially under harsh thermal cycling and dynamic loading such as drop and vibration. Mechanical stress conditions may induce additional failures in addition to those induced by thermal cycling, including solder joint brittle fracture and PCB/package pad interfacial failures.

For these reasons, new specifications (in addition to traditional thermal cycling requirements) are being generated by industry to better characterize SMT materials properties (package, PCB) and strain limitation (PCB, solder), as well as methods of defining mechanical resistance to repeated mechanical loading such as drops.

Specifications on Static and Dynamic Mechanical Testing

Figure 6 lists a number of specifications generated in recent years by commercial industry, particularly by the Association Connecting Electronics Industries (IPC) [6] and the Joint Electron Device Engineering Council (JEDEC) [7] in response to increasing demands on area array packages and their miniaturized versions and stack technologies. It also includes the key military specification (MIL-STD-810F) [8] that was updated (in 2008).

The key specifications for evaluation under mechanical testing are as follows.

(1) Joint IPC/JEDEC 9702 covers basic mechanical bend testing characterization and strains to failures using four points, a bend test method commonly used by industry. Specific strain gage attachment requirements are delineated in IPC-JEDEC-9704.

(2) Joint IPC/JEDEC 9707 covers a new test method that is more applicable for area array packages. It uses spherical loading at points rather than loading through cylindrical rod as was used in four-point bend testing defined in IPC 9702. This standard supplements existing standards for mechanical shock during shipping, handling, or field operation, as well as filling the gap for IPC/JEDEC 9702 to better characterize maximum strain levels. The two specifications provide a common method of establishing the fracture resistance of board-level package interconnects to flexural/point loading during PCB assembly and test operations. No pass/fail qualification requirements are provided, since each package/assembly is considered unique.

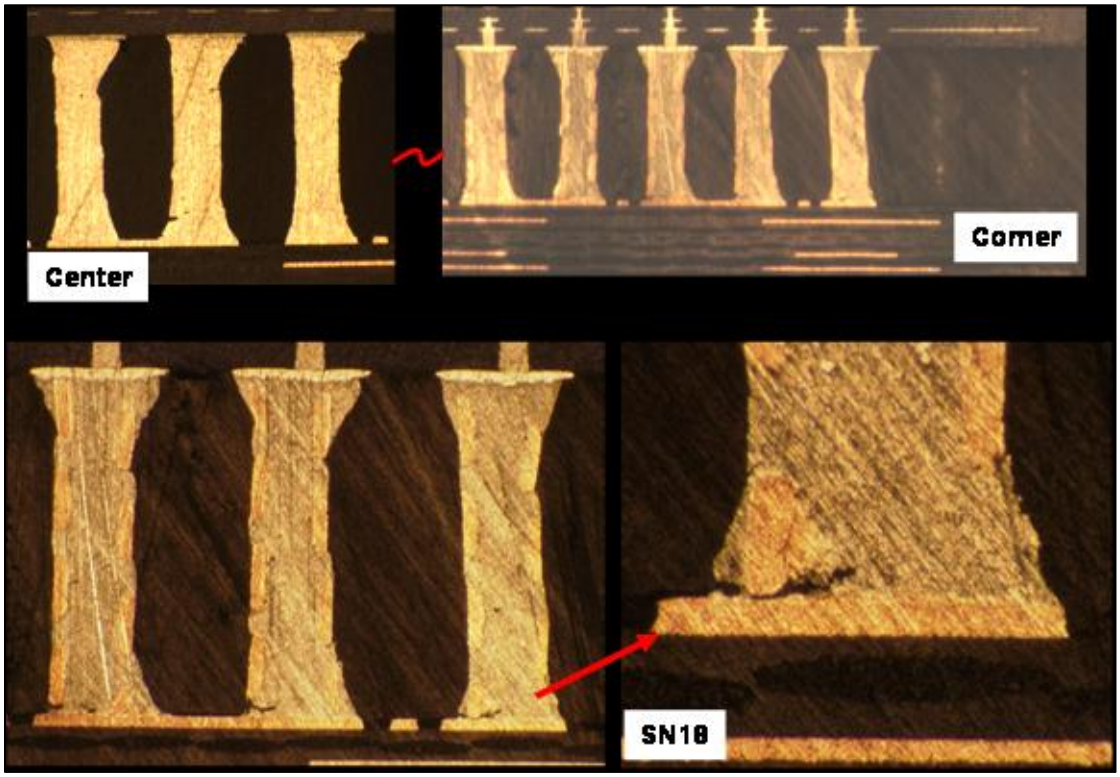

Figure 3. Cross-sectional optical photomicrographs of CGA 717 I/O assembly with non-solder mask defined (NSMD) pad design after thermal cycling.

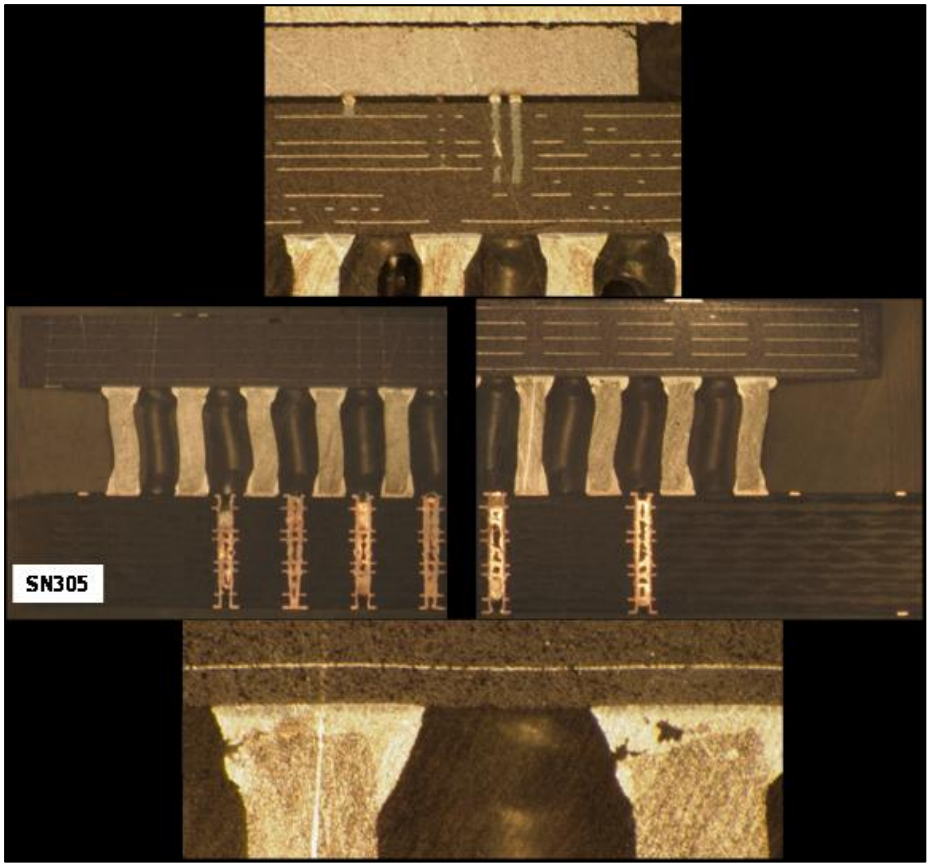

Figure 4. Cross-sectional photomicrograph of the CGA 1144 I/O assembly after thermal cycling.

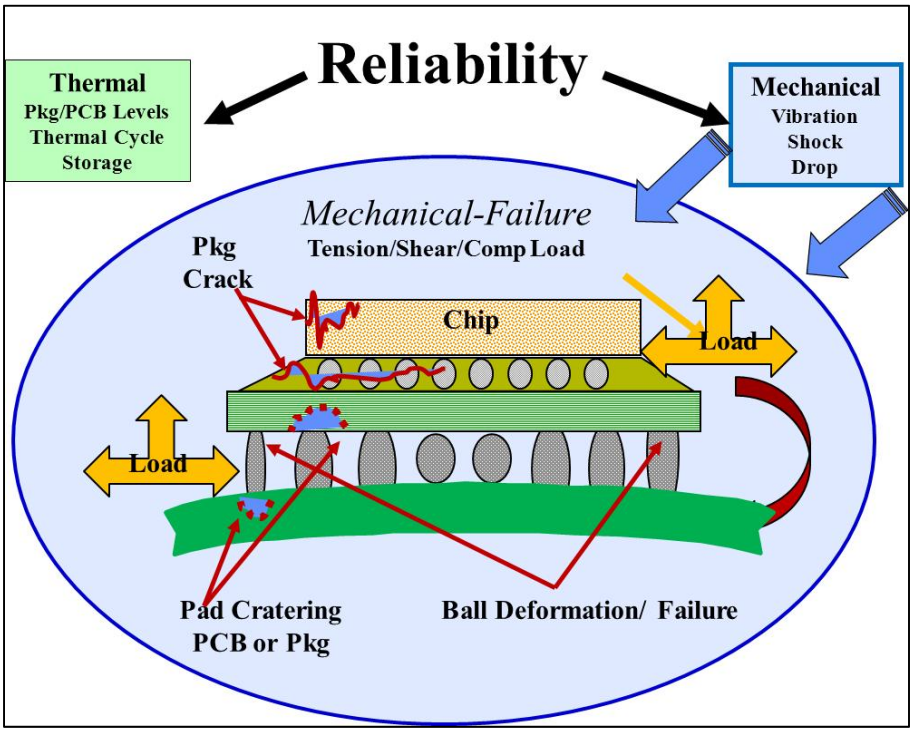

Figure 5. Reliability under thermal and mechanical loading with typical failure mechanisms under mechanical loading for area array package and assembly.

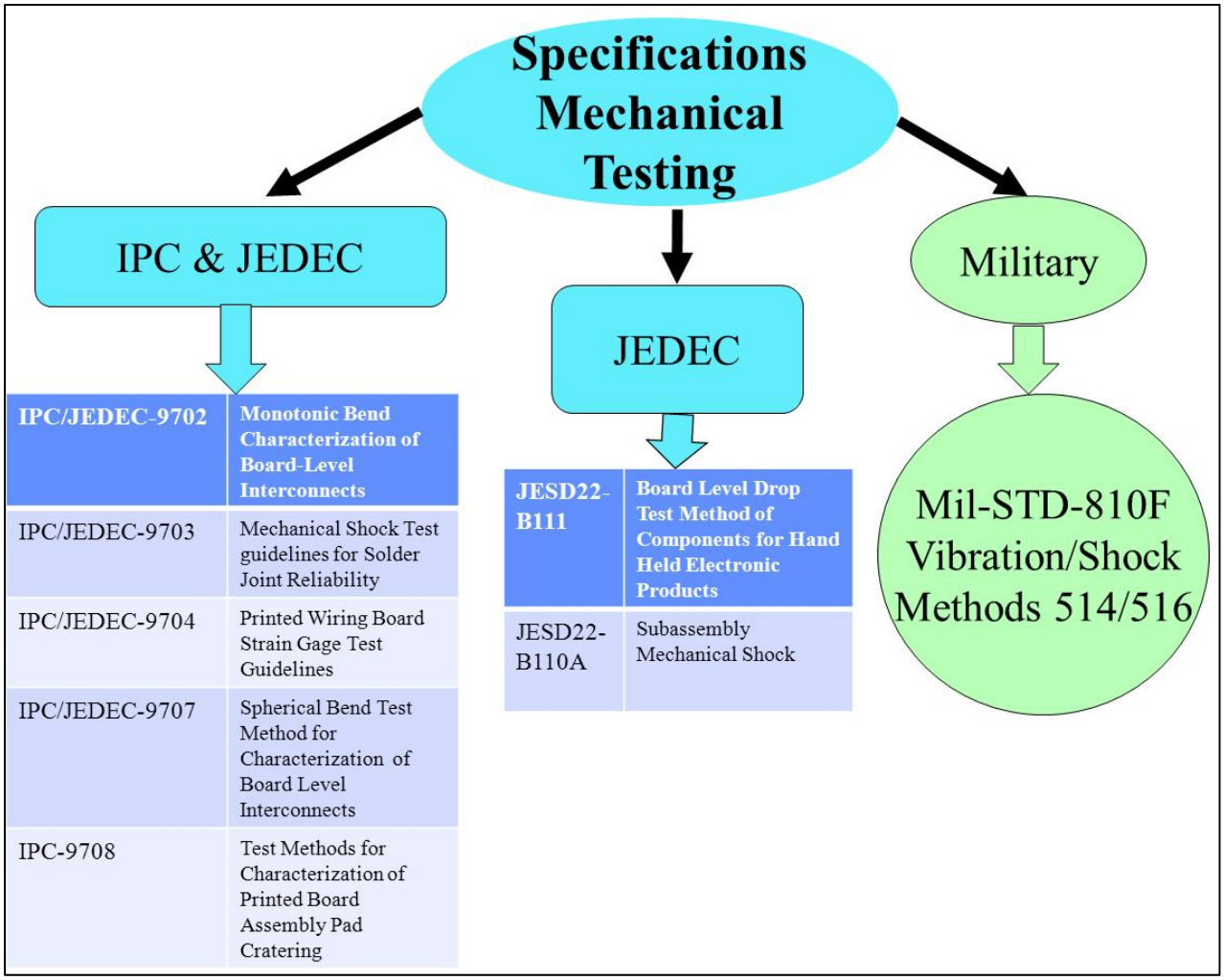

Figure 6. Key Commercial and military specifications for mechanical testing, including those that define bending, drop, vibration, and shock for behavior of microelectronics.

(3) IPC 9703 covers generic guidelines for mechanical drop and shock testing. These are only guidelines because of requirements differences between industries. The document scope includes: a) methods for defining mechanical shock use conditions, b) methods to define system level and system board level component testing that correlates to the use conditions, and c) guidance on the use of experimental metrologies for mechanical shock tests.

(4) IPC 9708 is generated in response to newly observed board failures (pad cratering) resulting from the move to implement Pb-free solder alloys. Pb-free solders are generally stiffer than tin–lead solders; they can transfer more of the applied global strain to the assembly. The Pb-free approach requires higher reflow temperatures that induce higher residual stress/strains in the assembly. Pb-free is typically assembled with phenolic-cured PCB materials that are more brittle than conventional dicyandiamide-cured (dicy-cured) FR-4 materials. These strains could eventually relax over time, but if mechanical strain is applied shortly after reflow, pad cratering could occur at lower mechanical strain levels.

(5) JEDEC JESD-B111 was developed for portable electronics in response to the need to define resistance to repeated drops, which is required for mobile applications. The shock pulse requirement for a PCB assembly is defined based on JESD22-B110, condition B, Table 1 (or JESD22-B104-B, Table 1) with 1500 Gs, 0.5 millisecond duration, and half-sine pulse. This specification is widely used by industry, and data are valuable for high-reliability applications. JESD-B210A defines resistance to mechanical shock.

(6) MIL-STD-810F covers many aspects of environmental testing (including mechanical vibration and shock), and it is well established for conventional microelectronics for high-reliability applications.

SUMMARY

The National Aeronautic and Space Administration (NASA) has numerous specifications that address approaches on evaluating resistance to thermal storage/cycling and mechanical loading at various levels for conventional packages, such as leaded components. In addition, workmanship requirements to meet harsher mechanical environments are in place. These specifications may not, however, be directly applicable for advanced electronics packages, especially for area array and 3D stack packages and assemblies. Commercial industry has developed new specifications for characterization of advanced electronics packages that are extremely valuable. These requirements should be reviewed, and their applicability for high-reliability applications should be identified and tailored in order to be able to effectively tap into these vast resources of commercial test data base. This article summarized a few key advanced electronics packaging and assemblies evaluated under thermal cycling; identifying damage and failure mechanisms that could be further explored. It was shown that failures for CGAs under thermal cycling occurred either at the package or PCB sites with microcracking on either site. For example, CGA 717 I/O with copper-wrapped columns showed signs of damage and microcracking at the PCB interface whereas CGA 1144 I/O with solid solder columns showed signs of microcracking at the package interface sites, both revealed by cross-sectioning. For the latter column style, because of less rigidity, tilting of columns (especially corner columns) was apparent after thermal cycling exposure. These detailed investigations improve understanding of key reliability mechanisms based on the test results for CGAs. They will facilitate the use of newly developed very dense FPGA area array packages with known reliability and mitigation approaches. This will allow greater processing power in a smaller board footprint and with a lesser system mass.

ACKNOWLEDGMENTS

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[7] JEDEC, JEDEC home page. (http://www.jedec.org/, accessed June 19, 2013)

[8] “Search Mil Specs & Drawings,” DLA website, DLA Land and Maritime, Columbus, OH. http://www.landandmaritime.dla.mil/Programs/MilSpec/DocSearch.aspx, accessed June 19, 2013)

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CLASS Y UPDATE

The Defense Logistics Agency Land and Maritime (DLA-VAC) on April 9–10, 2013 hosted a coordination meeting on the draft of MIL-PRF-38535, Revision K, that introduces Class Y, a space product category created to infuse new technology (such as the Xilinx Virtex-4 and 5 FPGAs and other similar products) into the military standards. There was a general consensus that the Class Y changes must be implemented soon. Based on the decisions made during this meeting, Rev. K was updated and sent out for review. The review period is now over, and DLA-VAC is adjudicating the responses, and they will release Rev. K. Any comments received by DLA-VAC not related to the decisions made at the coordination meeting will be considered for the next revision. The point of contact at DLA-VAC is Mr. Muhammad Akbar. For further details, contact **Shri Agarwal at 818-354-5598.**

GIDEP Alerts/Advisories

Contact your GIDEP Representative for a copy of:

Suspect Counterfeit	6L-A-13-01 Suspect Counterfeit, Microcircuit, SRAM, C5-A-13-01A Suspect Counterfeit, Microcircuit, Digital, Microprocessor, ID1-A-13-01 Suspect Counterfeit, Microcircuit, 5V Byte Alterable EEPROM, L1-A-13-01 Suspect Counterfeit, Integrated Circuit, Memory, SRAM, 512 KX8
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Reduced Schedule of Meetings

(Communication from DLA)

Due to "sequestration" and other budgetary negotiations in Congress and the associated contingency planning at DLA due to these negotiations, all travel that can be deferred will be deferred indefinitely. The publishing of the audit schedule will also be suspended during this time. For the rare exceptions to the travel deferment, you should hear from the responsible engineer/technician or Branch Chief directly. If you have any questions, please direct them to Joe Gemperline, (614) 692-0663, or Joseph.Gemperline@dla.mil.

NASA Parts Specialists Recent Support for DLA Land and Maritime Audits:

None.

Upcoming Meetings

- JEDEC JC-13, Columbus, Ohio, Sept. 16–19, 2013
- Space Passive Component Days, 1st International Symposium, ESA/ESTEC, Noordwijk, the Netherlands, September 24–26, 2013 http://www.globaleventslist.elsevier.com/events/2013/09/space-passive-component-days/

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