National Aeronautics
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Use of Commercial FPGA-Based Evaluation Boards for Single-Event Testing of DDR2 and DDR3 SDRAMs

R. L. Ladbury[1], K. A. LaBel[1], M. D. Berg[2], E. P. Wilcox[2], H. S. Kim[2], C. M. Seidleck[2], A. M. Phan[2]

Radiation Effects and Analysis Group
NASA Goddard Space Flight Center
Greenbelt, MD 20771 USA

[1] NASA Goddard Space Flight Center
[2]MEI Technologies, INC

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Ye Olde Table of Acronyms

DIMM=Dual In-line Memory Module
DDRX=Double-Data Rate of the Xth Generation
FBGA=Flip-chip Ball Grid Array
FPGA=Field Programmable Gate Array
IP=Intellectual Property
LET=Linear Energy Transfer
SDRAM=Synchronous Dynamic Random Access Memory
SEE=Single-Event Effect
SEFI=Single-Event Functional Interrupt
SEL=Single-Event Latchup
SEU=Single-Event Upset
SOTA=State Of The Art
VHDL=Very-high-speed integrated circuit Hardware Description Language

DDRX SDRAM* Test Challenges

Need complicated **IP to control and test memory

Ever increasing speed means frequent new tester development

***SOTA Memory requires SOTA controller**

Generation	Max Size	Data Rate
SDRAM	512 Mbit	<150 MHz
DDR*	1 Gbit	200-400 MHz
DDR2	2 Gbit	400-1066 MHz
DDR3	4 Gbit	800-2133 MHz
DDR4	4 Gbit	>2133 MHz

Part preparation difficult, risky

High density= high data rate

Signal Integrity, Board layout are critical

Procurement of test parts difficult

Possible ****SEL makes power-control desirable

Is there a better way to get a look at a new generation?

*DDRX SDRAM = Xth Generation Double Data Rate Synchronous Dynamic Random Access Memory

***SOTA = State Of The Art **IP = Intellectual Property ****SEL = Single-Event Latchup

What About Commercial Evaluation Boards?

IP available for control, but not optimized for test

Part preparation still difficult

Uses readily available *DIMMs

Tester development: Eval Boards pace memory advances

Generation	Max Size	Data Rate
SDRAM	512 Mbit	<150 MHz
DDR*	1 Gbit	200-400 MHz
DDR2	2 Gbit	400-1066 MHz
DDR3	4 Gbit	800-2133 MHz
DDR4	4 Gbit	>2133 MHz

Cannot control power To single die, but SEL risk decreasing (?)

Controller and Memory advance at ~same rate

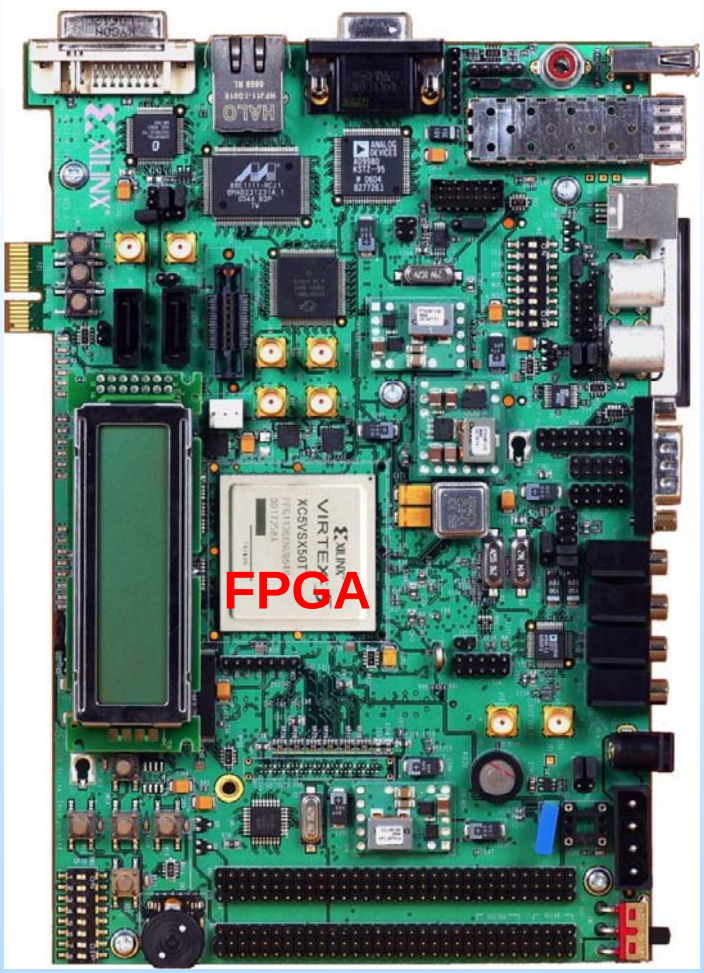
Eval boards built for high data rate

Board layout optimized for signal integrity

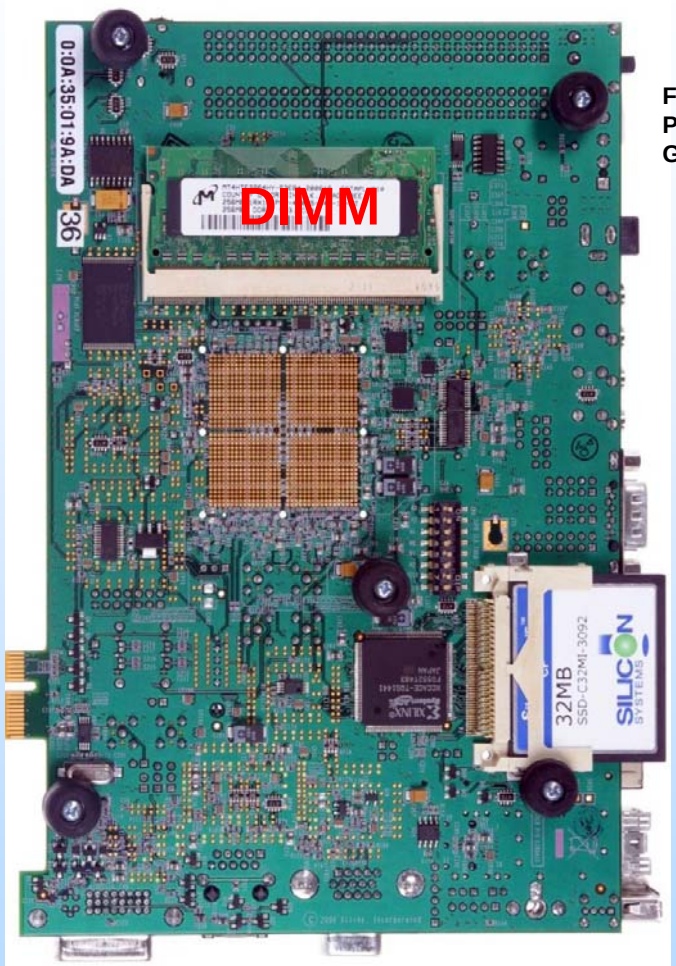
*DIMM=Dual In-line Memory Module

ML506 V5-Based DDR2 Eval Board

FPGA Side of Eval Board



DIMM Side of Eval Board



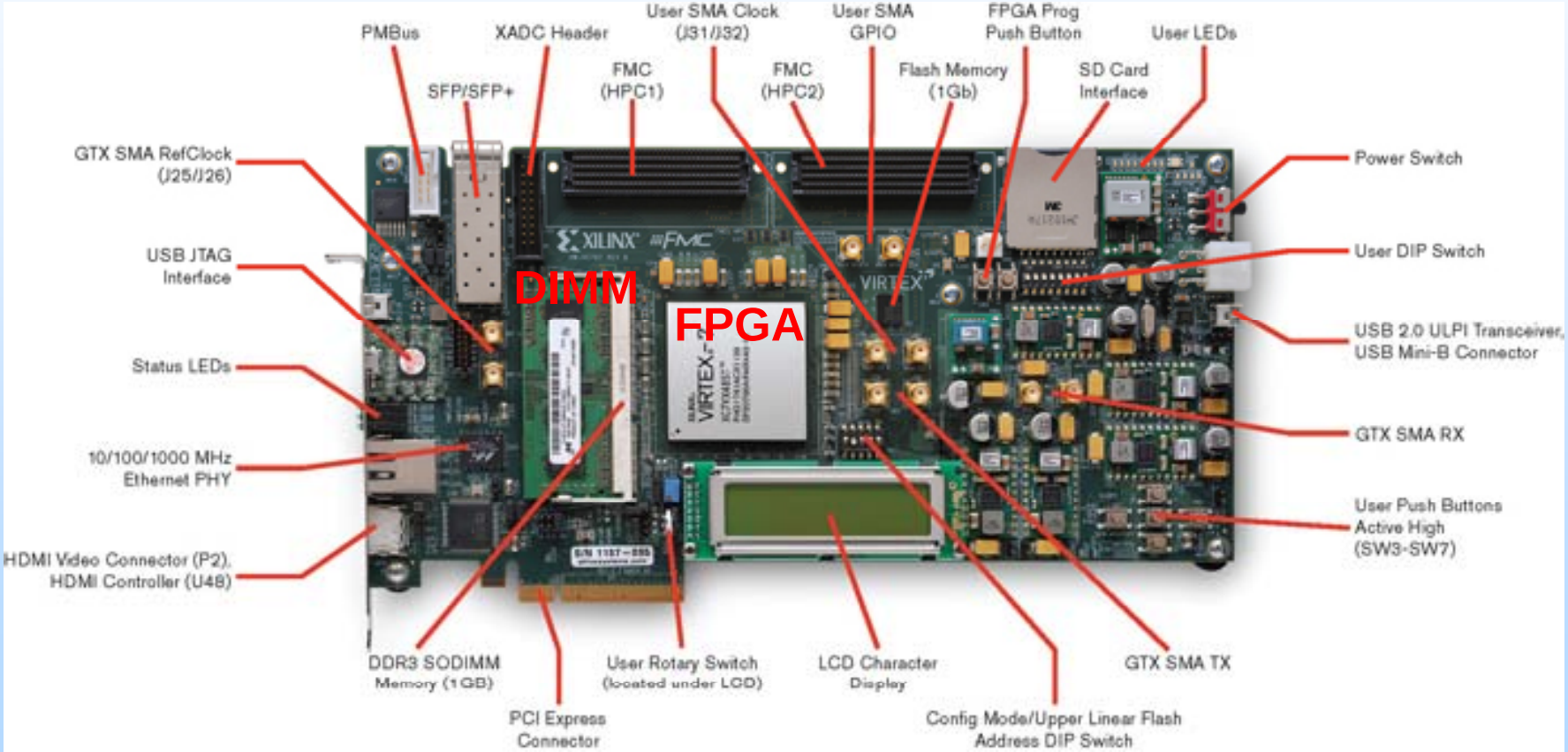
FPGA=Field Programmable Gate Array

FBGA=Flip-chip Ball Grid Array

DDR2 FBGA is Samsung K4T1G084QF-BCE7
DDR2 DIMM is Samsung M470T2863FB3-CE6 1 Gbyte module

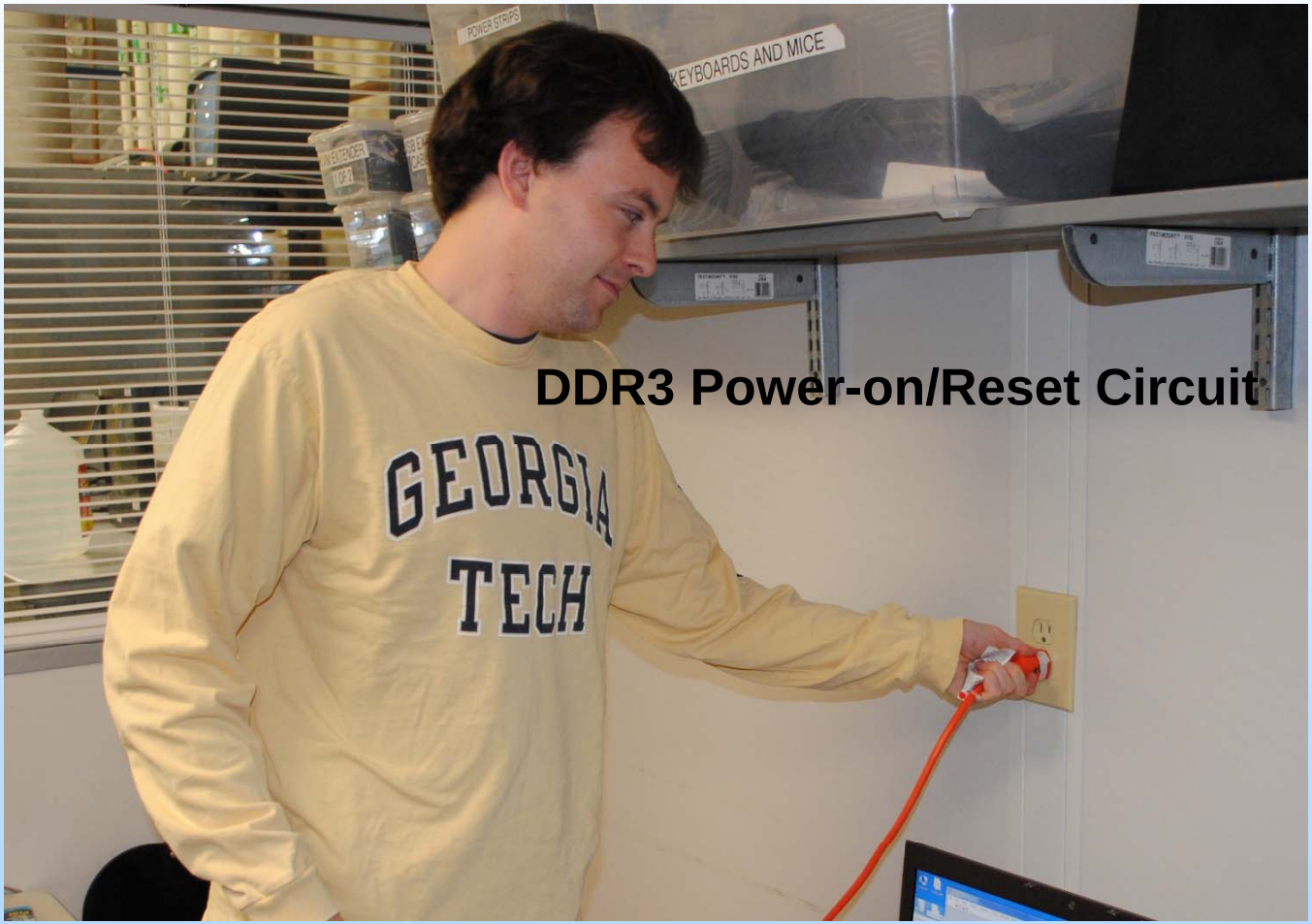
Xilinx V7-Based DDR3 Eval Board

- **VC707 DDR3 board more**
  - **Lots of features we do not need on a tester**
- **DIMM M471B5773DH0-CH9 uses FBGA K4B2G0846D-xxxx (Rev. D die)**
- **DIMM M471B5173BH0-CH9 uses FBGA K4B4G0846B-HCH9 (Rev. C die)**



Improvised Features

- **Of course, some features we take for granted are not available**



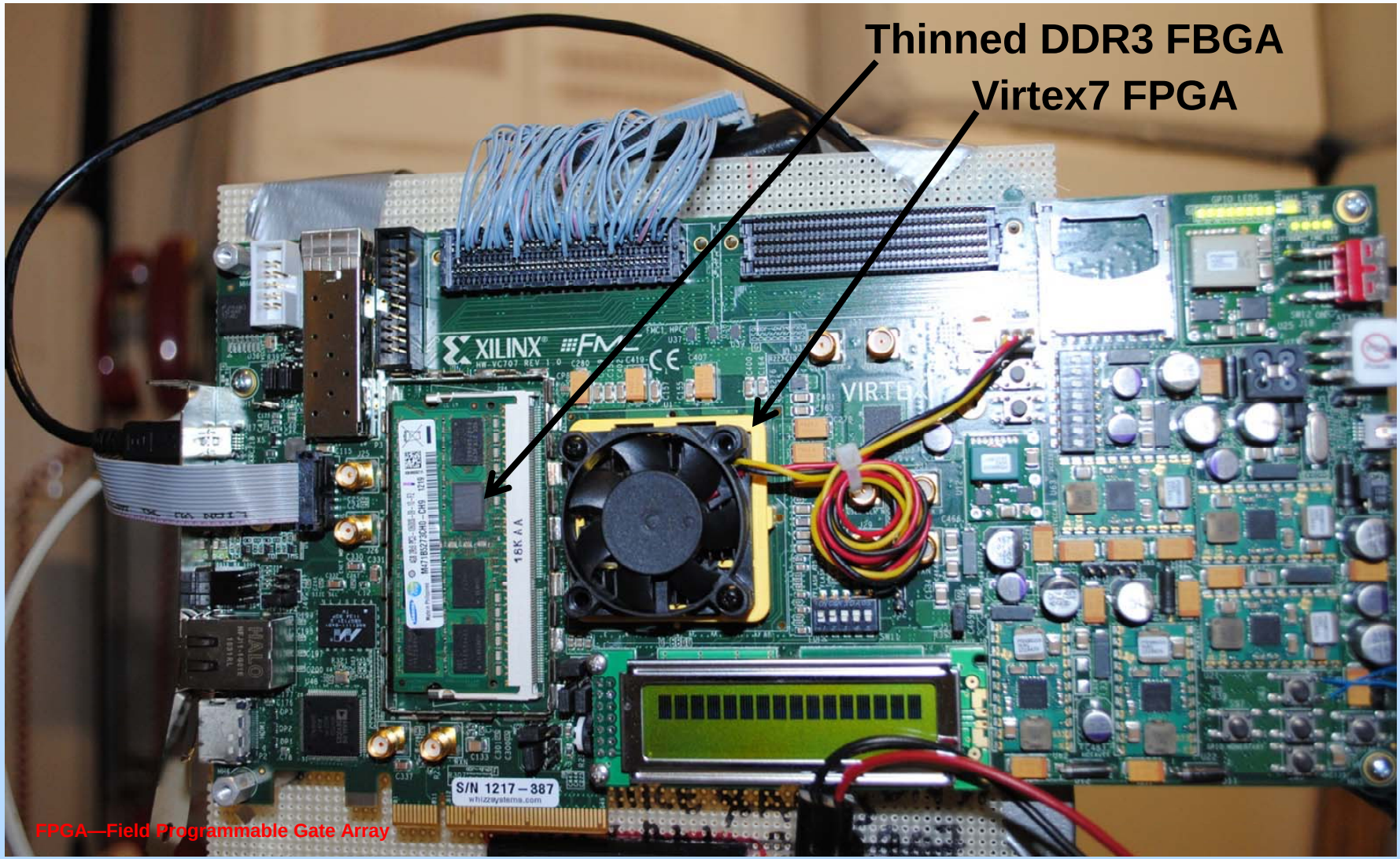
DDR3 Power-on/Reset Circuit

Thinning and Polishing DIMMs

- **DIMMs are fragile—mechanical thinning produced <50% yield.**
  - **Low-pressure+high speed worked best.**
  - **Thickness ranged from 120-200 microns—OK for 25 MeV/nucleon tune.**

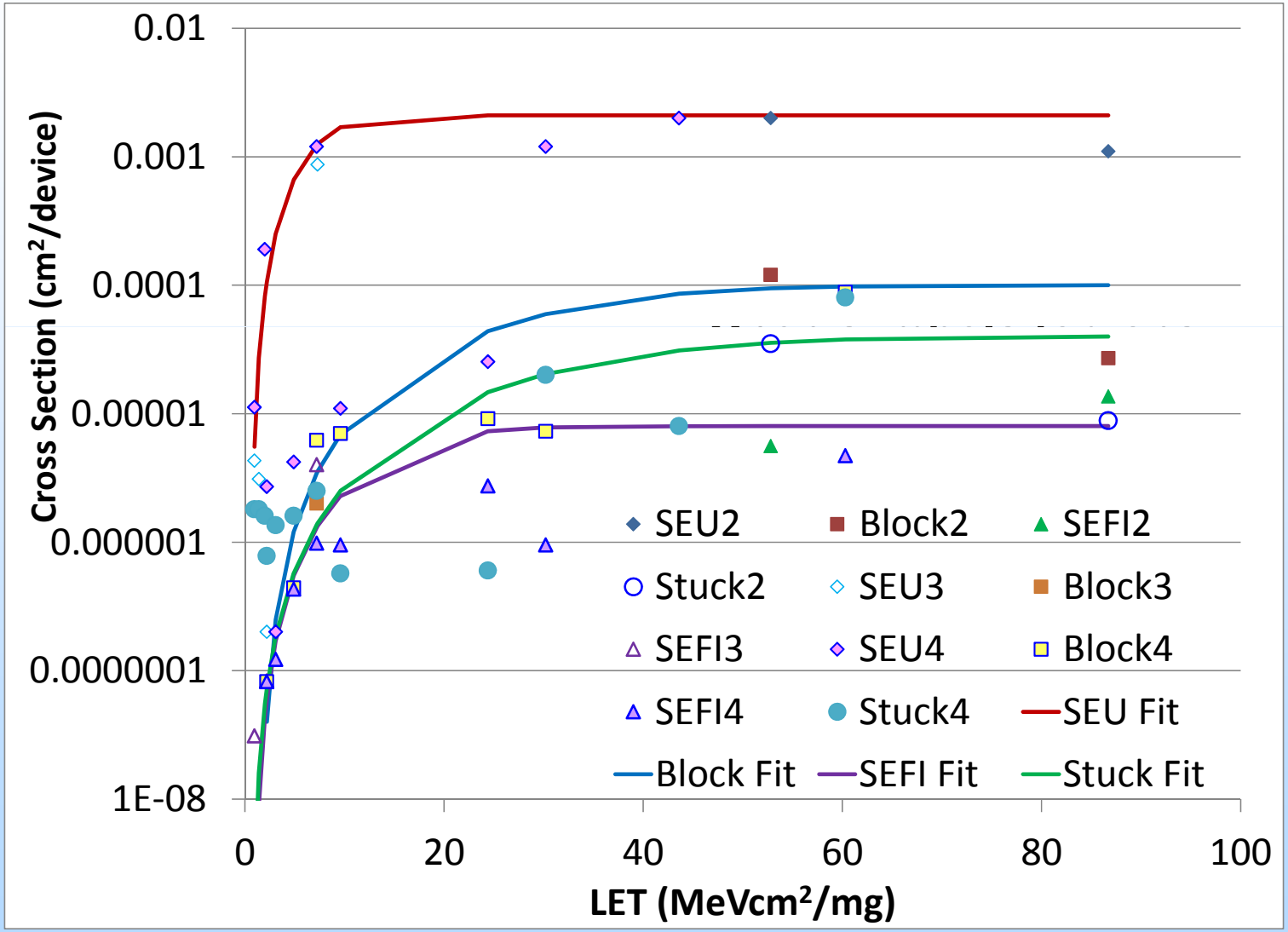
Setup at TAMU

– VC707 eval board configured as a tester at Texas A&M



FPGA—Field Programmable Gate Array

σ_{SEE} vs. LET for Samsung DDR2



SEU=Single-Event Upset

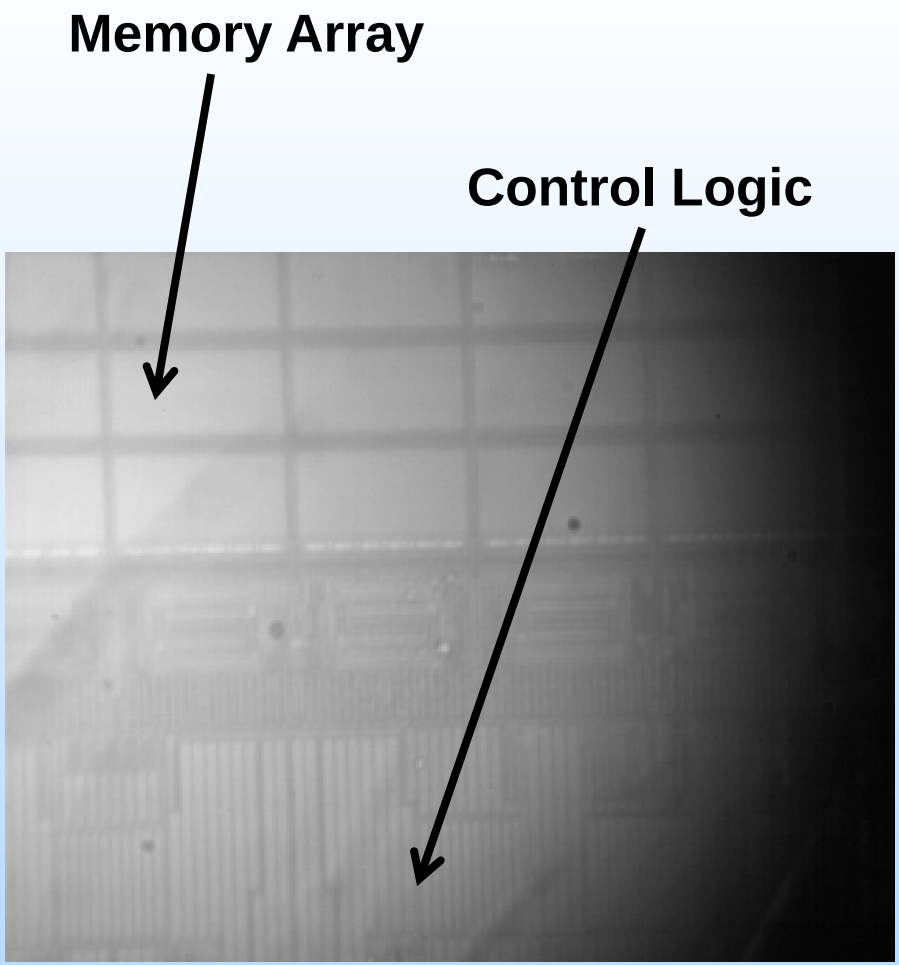
SEFI=Single-Event Functional Interrupt

LET=Linear Energy Transfer

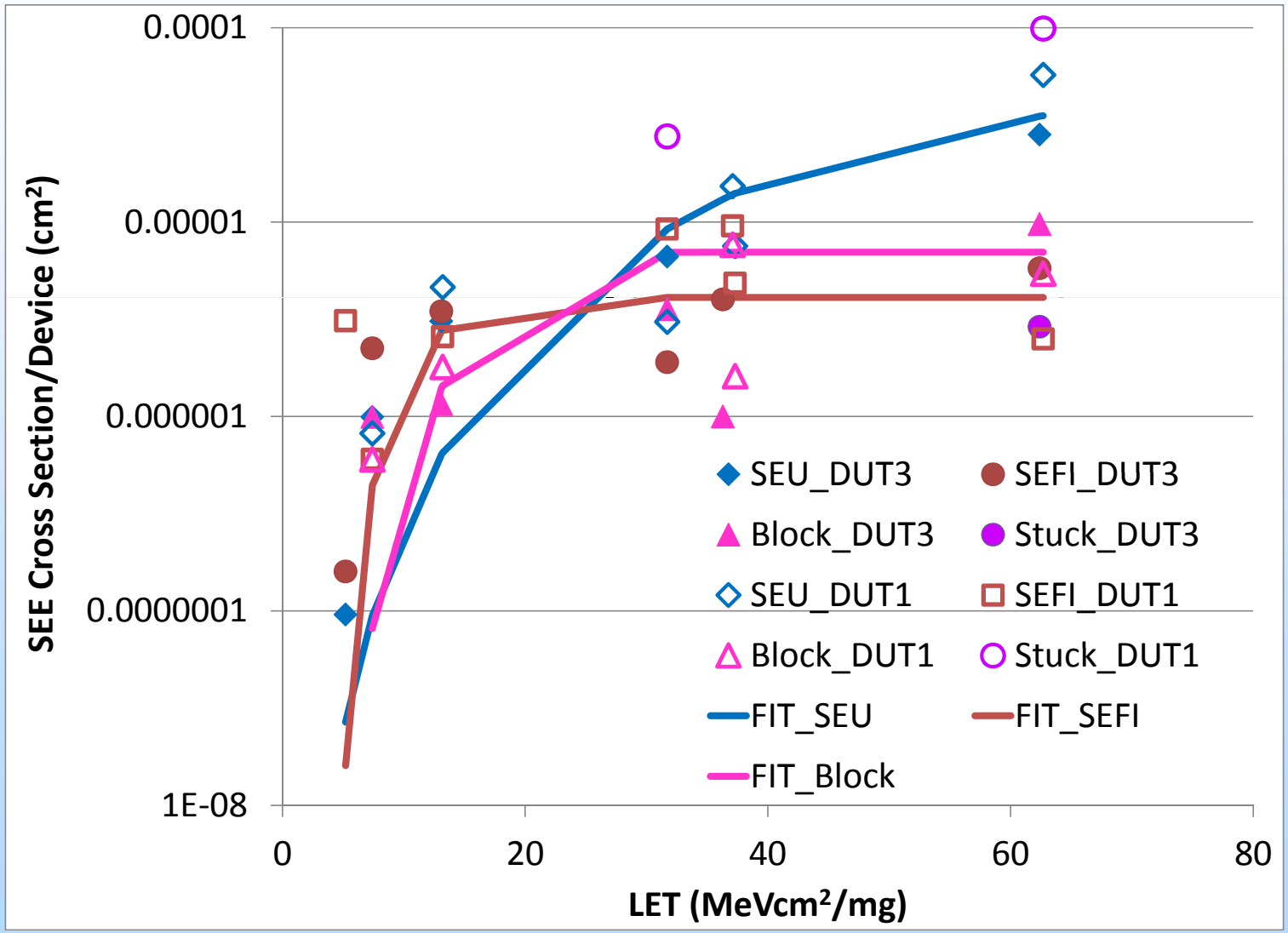
SEE=Single-Event Effect

DDR3 Results: NRL 2-Photon Pulsed Laser

- Errors affected from 1-bit to thousands
  - Block errors (column, row)
  - Burst errors (8, 32…)
  - SEFI
    - Hard reset needed to recover
    - Sometimes 2 hard resets
    - None of SEFIs required power cycle for recovery during laser testing
- No errors in memory arrays
  - More overburden than we think over memory arrays?
  - Sufficient margin on data retention that memory capacitor cannot discharge when access transistor hit?



σ_{SEE} vs. LET for Samsung DDR3



Eval Boards as SEE Testers

- Both ML506 (DDR2) and VC707 (DDR3) successful as testers
  - Operated reliably over hundreds of runs
  - DIMMs work as test vehicles—thinning poses issues (see below)
- Caveats
  - ML506 posed significant issues with timing when reconfigured as tester
  - VC707 IP was in Verilog (not VHDL*) and also posed timing challenges
  - Note: Configuration of FBGAs on a DIMM may vary from spec (e.g. which stores high and which low bits,)—really it says so in the spec!
    - Need to verify before the test
- Data sets are very large and require post-processing
- DIMMs pose their own issues
  - Thinning and polishing FBGAs on DIMM is tricky and low-yield; parts 120-200 microns thick could be problematic for low-energy ion testing
  - Cannot control current to individual memory chips—problematic for SEL

*VHDL=Very-high-speed integrated circuit Hardware Description Language

Conclusions

- **Samsung DDR2 SDRAMs exhibit**
  - **High susceptibility to SEU, block errors, and SEFI (Onset LET~1Mevcm^2/mg)**
  - **Moderate stuck bit susceptibility—onset probably >20 Mevcm^2/mg), as some stuck bits seen at low LET likely due to multiple ion hits**
  - **SEFI requiring power cycle for recovery were seen—rare events**
- **Samsung DDR3 SDRAMs significantly harder than DDR2 devices**
  - **Onset LETs for SEU, block errors and SEFI 3-5 Mevcm^2/mg**
  - **Stuck bits seen only for LET>25 Mevcm^2/mg (significant part-to-part variation)**
  - **A few % of SEFIs required power cycle for recovery**
- **Commercial FPGA Eval boards can be used as DDRX testers**
  - **Positives**
    - **Performed reliably, yielding good quality data**
    - **Less expensive than a custom tester**
    - **DIMMs readily available—can be adapted to SEE testing**
  - **Challenges**
    - **Significant modifications to IP for DRAM controller needed for SEE testing**
    - **Board not optimized for SEE testing**
    - **Cannot control power to individual DUT on DIMM**

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