Lessons Learned from Radiation Induced Effects on Solid State Recorders (SSR) and Memories

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Table of Contents

1 Background

This document represents an update to the original study from 2002. Where possible, we have retained the language and format of the original. New material is labeled with a section that includes the dates 2002-2012. In some cases we have altered the original to improve clarity or for consistency with the updates. The emphasis of the original study was the effect of space radiation environments on the performance of state-of-the-art commercial memories, although it also contains guidelines for successful use of commercial memories in space. For the update, there were fewer space-borne experiments, so the emphasis is more on guidelines for use of the latest Synchronous Dynamic Random Access Memories (SDRAMs) in space.

1.1 Introduction

Solid State Recorders (SSR) have replaced the electromechanical tape recorders to store onboard science and engineering data in the early nineties. They provide increased data storage capacity for a reduced power and weight. However SSR uses commercial, non-hardened, memories that are particularly susceptible to the space radiation environment. Because of this, radiation mitigation techniques and system-level monitoring capabilities have been implemented to handle radiation effects such as Single Event Upsets (SEU) and Multiple Bit Upsets (MBU). Thus, as a byproduct of the monitoring tasks which form a normal part of a spacecraft's "house-keeping" process, useful data [1-8] have been gathered the last ten years on the radiation tolerance of memories used in SSR. In the same way, SEU data have also been gathered on Onboard Computer (OBC) memories[9-10].

In addition, specific non-hardened memory experiments [11-22] have been flown that give additional information.

1.1.1 Update for 2002-2012

SSRs have continued as the dominant data storage technology for space missions. During this period, commercial SDRAM have been the predominant memory technology used in these recorders, and radiation effects susceptibility has continued to be one of the main drivers in SSR design. Although several studies of SDRAM radiation susceptibilities have been published during this period,[Lawrence, Ladbury, Koga], relatively few on-orbit studies have been published during this past decade.[Ladbury, Schaeffer] More recently, Single Event Effect (SEE) testing has concentrated on double-data-rate (DDR) SDRAMs, especially the second and third generation memories (DDR2 and DDR3). However, to date, no SSRs based on DDR SDRAMs have been flown.

1.2 Radiation effects and memories

1.2.1 Single Event Effects

1.2.1.1 Destructive Events

Modern memories are potentially sensitive to Single Event Latchup (SEL) like all CMOS devices. Generally the risk of SEL in space is limited to heavy ions and devices fabricated on epitaxial substrates are less prone to be sensitive to SEL. However some devices fabricated on epitaxial substrates exhibit SEL sensitivity [23-25], and protons could induce latchup in sensitive technologies [26-29].

As gate oxide thickness and feature sizes decrease Single Hard Errors (SHE) have been observed on memories. We can distinguish two types of SHE: first, stuck memory cells due to local total ionizing dose deposition ("microdose") [30-32], and second, Single Event Gate Rupture (SEGR) failures. SEGR failures have been observed on Dynamic Random Access Memories (DRAMs) [33], Electrically Erasable Programmable Read Only Memory (EEPROM), and Flash Programmable Read Only Memories (PROMs) [34,35,36]. EEPROM are more sensitive during write/programming operation because of the higher voltages applied on thin oxides during these operations [37].

1.2.1.1.1 Destructive SEE 2002-2012

SDRAMs continued to exhibit susceptibility to SEL and SHE during this period. Most parts exhibited SEL susceptibility at the 256 Mbit generation of SDRAMs.[Koga2000] Susceptibility was also common for 512 Mbit parts.[Ladbury, Koga/Langley, J. Bertrand] One exception was the Elpida EDS5104ABTA memory, which has not exhibited SEL sensitivity even at elevated temperature. This last memory has been the basis for most SSRs and

other bulk memory applications for the past 8 years primarily because of its immunity to SEL. Many DDR,[Ladbury_2006] and DDR2[Ladbury_2008, Koga_2010] exhibited SEL susceptibility. Recently, DDR3 SDRAMs have not exhibited SEL susceptibility.[Hermann, Grurmann, Koga]

1.2.1.2 Non Destructive Events

Static Random Access Memories) (SRAMs) and DRAMs are extremely sensitive to heavy ion and proton induced Single Event Upset (SEU). They are also sensitive to Single Event Multiple Bit Upsets (MBU) by the following mechanisms:

- diffusion of charge to closely spaced junctions that upsets several neighboring cells [38,39].
- a particle striking a memory at a grazing angle of incidence that intersects several sensitive regions and cause multiple upsets [39,40].
- a particle strike in the interface and/or control circuitry of the device that cause large numbers of bits to upset in row, column errors or block errors [39, 41, 42, 43]. These errors in control logic may lead to Single Event Functional Interrupts (SEFI) that need a reset or even a power cycling to restore nominal operations of the device. Complex state of the art memories like SDRAMs are significantly sensitive to SEFI [44].

EEPROMs and flash EPROM memory cells are not altered by heavy ions and protons in read mode, but Single Event Transient (SET) in the peripheral circuitry induce reading errors on one or several bits of a data word [36,45]. In write or programming mode, these devices are extremely sensitive and this can result in a significant number of programming errors: single bit errors or block errors and even SEFI [35,36].

1.2.1.2.1 Nondestructive SEE since 2002

The most notable trend since 2002 is the increasing importance of SEFI and block errors relative to SEU. Fig. 1 shows the numbers of addresses upset due to block errors for the Elpida 512 Mbit SDRAM. Since block errors occur with a rate greater than 1% that of SEU, and the average block error upsets hundreds of addresses, it is clear that control-logic upsets resulting in SEFI and block errors will dominate the data errors for this device.

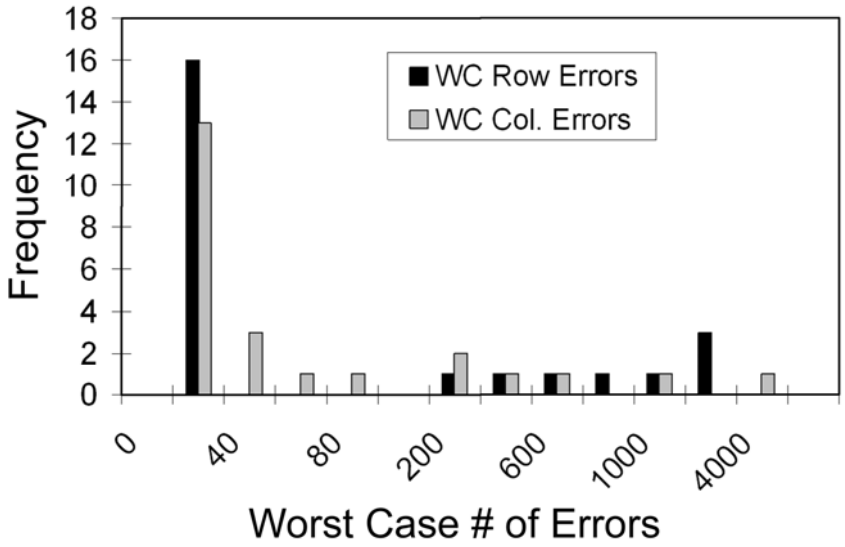

Fig. 1: Block errors can upset hundreds to thousands of errors, while occurring at rates greater than 1% of the SEFI rate. This means most corrupted data will come about due to block errors and SEFI.[67]

The increasing importance of block errors and SEFI persists for DDR, DDR2 and DDR3 devices (see Fig. 2). However, the inclusion of a Phase-Lock-Loop to facilitate double data rate operation presents a new SEFI mechanism—disturbance of the clocking to the extent that normal functionality cannot be restored without resynching the memory. These errors can complicate recovery from a disruptive SEFI. This may be one reason why DDR2/3 devices have exhibited an increasing susceptibility to SEFI (Fig. 2). While not every DDR2/3 manufacturer has seen such explosive growth in SEFI susceptibility, the rate of block errors and SEFI has grown enough that these error modes dominate data errors (correctable or not).

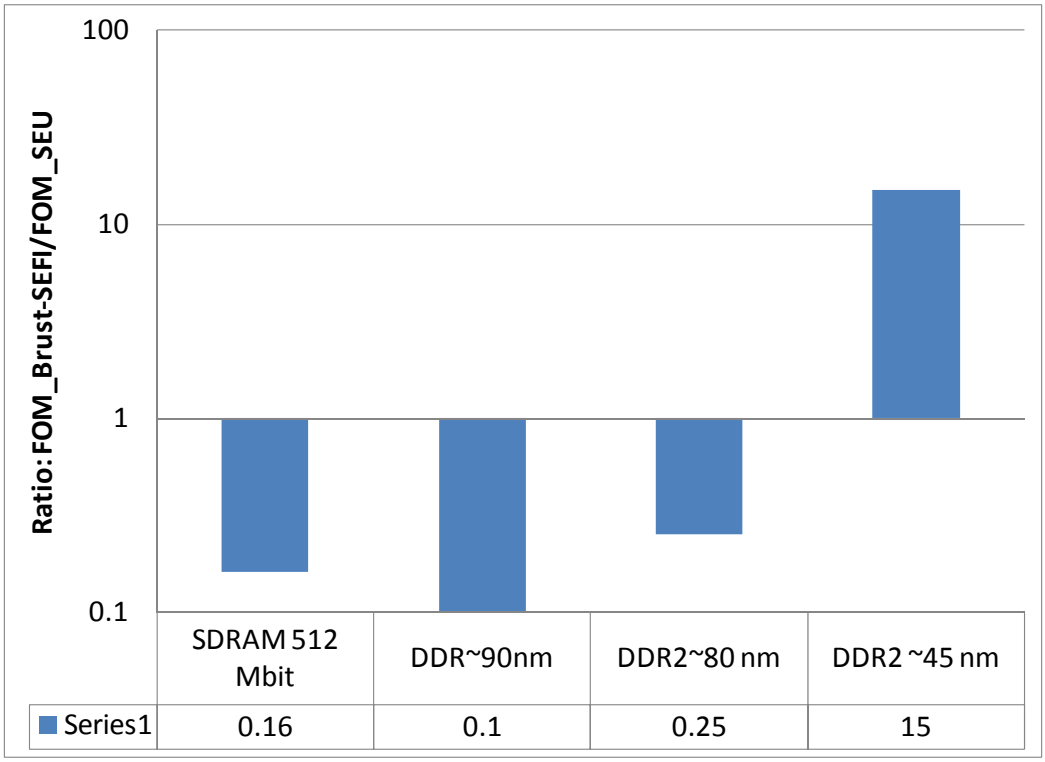

Fig. 2 Although the ratio of block errors and/or SEFI to SEU remained in the range of 0.1 to 1 during most of the period covered by this update—more recent tests (e.g. Koga et al. 2010) have shown a marked increase in SEFI and block error rates. Shown here is the ratio of the Figure of Merit for SEFI/block errors to the FOM for SEU vs. generation of SDRAMs.

1.2.2 Total Dose Effects

SRAMs and DRAMs are sensitive to Total Ionizing Dose (TID). The first effect of TID at the device level is a significant increase of the standby current, and a decrease of the retention time of DRAMs, followed by the loss of bits (stuck bits) [46-48]. As for other commercial devices, the TID sensitivity varies significantly for different device types and also for different devices of the same type. The increase of standby current is noticeable after a few krad(Si) and the first memory cell in error appears after a total dose level ranging from 8 to >100 krad(Si) depending on the device type [46-49].

EEPROMs and flash EPROM are also sensitive to TID. The degradation is higher when exposed to radiation during programming operations. When the parts are irradiated in read mode, they can withstand TID levels ranging from 5 to 30 krads(Si) without functional failures. However, they may fail programming operations after only a few krad(Si) [36, 50-51].

1.2.2.1 TID Effects from 2002-2012

Because SDRAM and DDR SDRAMs are state-of-the-art CMOS parts, they share the same TID trends expected due to scaling. Degradation due to TID generally decreases as technologies scale to lower feature sizes (and thinner oxides), and SDRAM/DDR/DDR2 technologies have been no exception. Early during the period covered by this update, one study revealed significant variability in TID performance of 256 Mbit parts, with some parts failing at 15 krad(Si) and others failing at over 200 krad(Si).[58] The test parts in this study did not have lot traceabilty, so it was thought that the variability was predominantly lot-to-lot rather than part-to-part within a wafer lot. This was subsequently confirmed by other studies that did have lot traceability[59]

Studies of devices in the 512 Mbit generation of SDRAMs also revealed susceptibility to TID degradation between 30 and 50 krad(Si).[60] Double-data-rate (DDR) SDRAMs were found to remain functional at dose levels above 100 krad(Si) of protons.[61] DDR2 devices in the 90 nm generation of devices remained functional up to 250 krad(Si)[62] and for more recent devices (40-50 nm feature size) up to 800 krad(Si).[62] These increases in TID hardness are roughly commensurate with other part types fabricated in highly scaled CMOS. [Annealing]

In general, although operating currents may increase with dose for many test conditions, failure often occurs with little warning as a few addresses or bits lose functionality and more bits join them as dose increases. Elevated temperature or decreased refresh rate increase the number of failed bits. Usually, while the control logic is the first to exhibit parametric degradation, the memory cells are the first component of the SDRAM to fail functionally.

2 Flight Data

2.1 Introduction

Fig. 3 and Table I list all the flight data on memories available in the literature along with the space environment for the mission. It gives information about the spacecraft name, the memory application (data on SSR memory, on-board computer (OBC) memory, or experiment), the memory size, the type of memory, the part type and manufacturer, the period of flight and the type of orbit. Fig. 3 plots the periods of flight of the data listed in Table 1. The available data covers more than a full solar cycle on different types or orbits, including Low Earth Orbit (LEO), LEO polar, L1 LaGrange Point, Geostationary Earth Orbit (GEO) and highly elliptical GEO transfer Orbits (GTO) orbits exposed to GCR and solar particles, LEO polar orbits exposed to GCR and solar particles and also trapped protons in the South Atlantic Anomaly, and finally LEO inclined orbits, less exposed to GCR and solar particles but more exposed to the trapped particles radiation. LEO mission radiation environments tend to be dominated by trapped protons, especially in the South Atlantic Anomaly (SAA). Polar LEO missions are exposed to Galactic Cosmic Rays (GCR) above the poles, while solar particles and GCR dominate for GEO, L1 and GTO environments.

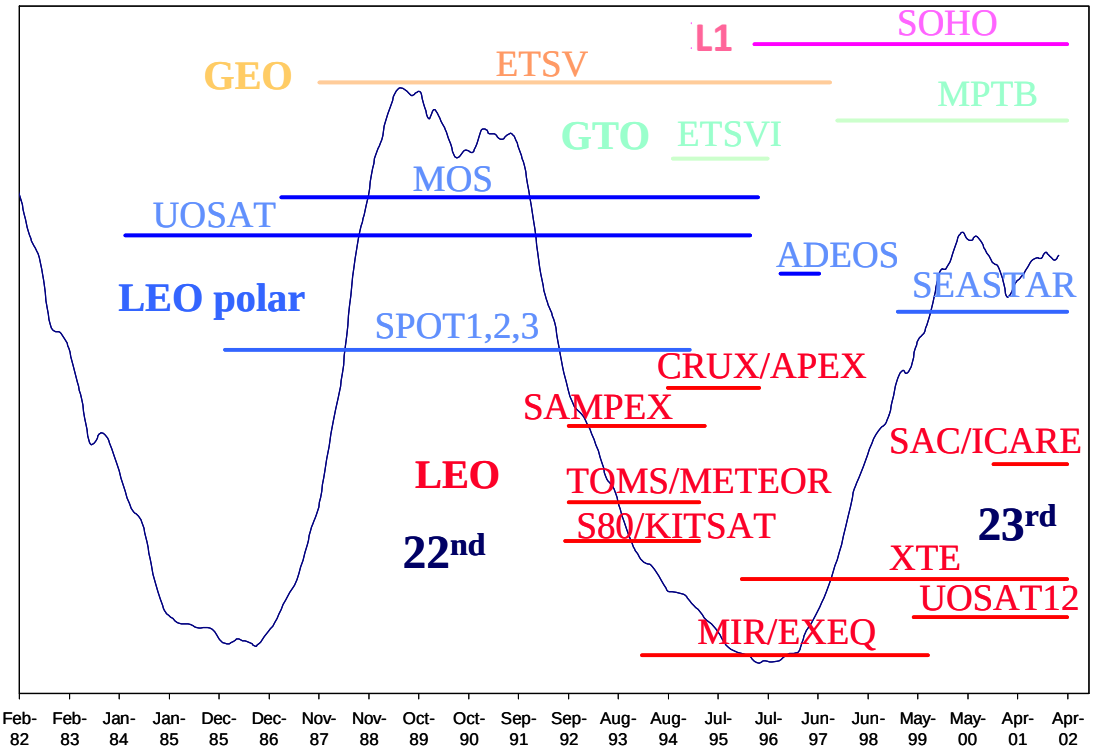

Fig. 3: Period of flight of the different data available. The different orbit types are identified by colors: L1 in magenta, GEO in orange, GTO in green, LEO polar in blue, and other LEO in red. The number of sunspots has also been plotted (black curve) to illustrate the solar activity.

Table I: Missions Reporting On-Orbit Data for Radiation Performance of Commercial Memories (1/2)

Spacecraft	Data type	size	type of memory	part number	manuf.	Start	End	Orbit	data ref.
SOHO	SSR	2Gbit	DRAM 4M*1	SMJ44100	TI	04/01/96	8/30/01	L1	[3]
MOS-1	OBC	1.5Kbit	SRAM 0.5K	93419	FCD	03/01/87	11/30/95	909 km, 99deg	[9]
MOS-1b	OBC	16Kbit	SRAM 4K	CMM5114	RCA	02/07/90	4/25/96	909 km, 99deg	[9]
ETSV	OBC	512Kbit	SRAM64K	uPD4464D-20	NEC	11/24/87	9/12/97	GEO	[9]
ETSVI	OBC	512Kbit	SRAM64K	91901	NEC	09/03/94	6/30/96	8000*38000 km,13 deg	[9]
ADEOS	OBC	1536Kbit	SRAM256K	92001	HIT	09/27/96	6/29/97	800 km, 98.6 deg	[9]
CASSINI	SSR	2*2.5Gbit	DRAM 1M*4		OKI	10/15/97		interplanetary	[52]
SAMPEX	SSR	212 Mbit	SRAM32K*8		HIT	9/5/1992	4/19/95*	580*640 km, 82 deg	[1-2]
TOMS/Meteor3	SSR	128Mbit	SRAM32K*8		HIT	9/5/1992	3/11/95*	1200 km, 82 deg	[1-2]
SEASTAR	SSR	2*512Mbit	DRAM4M*1	MDM1400G-120	HIT	1/1/1999		705 km, 98 deg	[53]
XTE	SSR	512 Mbit	SRAM128K*8	HM628128	HIT	1/1/1996		580 km, 23 deg	[53]
CRUX/APEX	EXP	23Mbit	SRAM128K*8	MT5C1008	MICRON	Aug-94	May-96	362*2544 km, 70 deg	[11-13]
CRUX/APEX	EXP	9Mbit	SRAM128K*8	88130L45PC	EDI	Aug-94	May-96	362*2544 km, 70 deg	[11-13]
CRUX/APEX	EXP	16Mbit	SRAM128K*8	628128	HIT	Aug-94	May-96	362*2544 km, 70 deg	[11-13]
CRUX/APEX	EXP	10Mbit	SRAM32K*8	MT5C2568	MICRON	Aug-94	May-96	362*2544 km, 70 deg	[11-13]
CRUX/APEX	EXP	4.5Mbit	SRAM32K*8	8832C12C1	EDI	Aug-94	May-96	362*2544 km, 70 deg	[11-13]
CRUX/APEX	EXP	4.75Mbit	SRAM32K*8	71256L100DB	IDT	Aug-94	May-96	362*2544 km, 70 deg	[11-13]
APEX	SSR	512 Mbit	DRAM4M*1	HM514100	HIT	8/3/1994	5/16/95*	362*2544 km, 70 deg	[7]
HST	SSR	12Gbit	DRAM4M*4	Luna es rev C	IBM	Feb-97		600 km, 29 deg	[54]
S80T	SSR	96Mbit	SRAM128K*8	D431000	NEC	08/10/92	1995?	1305*1325 km, 66 deg	[3-4-5]
S80T	SSR	8Mbit	SRAM32K*8	D43256	NEC	08/10/92	1995?	1305*1325 km, 66 deg	[3-4-5]
S80T	SSR	8Mbit	SRAM32K*8	CXK58257	Sony	08/10/92	1995?	1305*1325 km, 66 deg	[3-4-5]
KITSAT-1	SSR	96Mbit	SRAM128K*8	CXK58001	Sony	08/10/92	1995?	1305*1325 km, 66 deg	[3-4-5]
KITSAT-1	SSR	8Mbit	SRAM32K*8	CXK58257	Sony	08/10/92	1995?	1305*1325 km, 66 deg	[3-4-5]
UOSAT-5	SSR	8Mbit	SRAM32K*8	D43256	NEC	08/10/92	1995?	770 km, 98 deg	[3-4]
UOSAT-5	SSR	64Mbit	SRAM128K*8	D431000	NEC	08/10/92	1995?	770 km, 98 deg	[3-4]
UOSAT-5	SSR	32Mbit	SRAM128K*8	CXK581000	Sony	08/10/92	1995?	770 km, 98 deg	[3-4]
UOSAT-2	OBC	192Kbit	DRAM16K*1	MKB4116	Mostek	Mar-84		672*654 km, 97.8 deg	[4]
UOSAT-2	OBC	384Kbit	DRAM16K*4	TMS4416	TI	Mar-84		672*654 km, 97.8 deg	[4]
UOSAT-3	SSR	24Mbit	SRAM32K*8	HM62256	HIT	Jan-90		801*782, 98.6 deg	[4]
UOSAT-3	SSR	8Mbit	SRAM32K*8	MSM256	MIT	Jan-90		801*782, 98.6 deg	[4]
FaSat-Bravo	SSR	96Mbit	SRAM128K*8	M5M51008	MIT	Aug-98	Sep-99		[6]
ThaiPhutt	SSR	128Mbit	SRAM512K*8	KMC684000	Samsung	Jul-98	Sep-99		[6]
UOSAT-12	SSR	128Mbit	SRAM512K*8	HM628512	HIT	04/21/99		638*654 km, 64.6 deg	[6]
UOSAT-12	SSR	512Mbit	SRAM512K*8	SYS84000	Samsung	04/21/99		638*654 km, 64.6 deg	[6]
UOSAT-12	SSR	512Mbit	SRAM512K*8	SYS84000	Samsung	04/21/99		638*654 km, 64.6 deg	[6]
SPOT1-2-3	OBC	1.4Mbit	SRAM1K*1	HEF4736	Phillips	Feb-86	1995*	800 km, 97 deg	[10]

Table 1: Missions Reporting On-Orbit Data for Radiation Performance of Commercial Memories (2/2).

Spacecraft		size	type of memory	part number	manuf.	Start	End	Orbit	data ref.
MIR/EXEQ	EXP	3Mbit	SRAM32K*8	HM65756	MHS	Jul-92	Jan-94	350 km, 51.6 deg	[14-15-16]
MIR/EXEQII	EXP	512Kbit	SRAM32K*8	HM65756	MHS	Feb-94	Sep-95	350 km, 51.6 deg	[15-16]
MIR/EXEQII	EXP	2Mbit	SRAM128K*8	MT5C1008	MICRON	Feb-94	Sep-95	350 km, 51.6 deg	[15-16]
MIR/EXEQII	EXP	2Mbit	SRAM128K*8	H68128	HIT	Feb-94	Sep-95	350 km, 51.6 deg	[15-16]
MIR/EXEQII	EXP	32Mbit	DRAM4M4	SMJ416400	TI	Feb-94	Sep-95	350 km, 51.6 deg	[15-16]
MIR/EXEQII	EXP	32Mbit	DRAM16M	Luna E	IBM	Feb-94	Sep-95	350 km, 51.6 deg	[15-16]
MIR/EXEQIII	EXP	512Kbit	SRAM32K*8	HM65756	MHS	Oct-95	Mar-97	350 km, 51.6 deg	[15-16]
MIR/EXEQIII	EXP	2Mbit	SRAM128K*8	MT5C1008		Oct-95	Mar-97	350 km, 51.6 deg	[15-16]
MIR/EXEQIII	EXP	128Kbit	SRAM64K		russian	Oct-95	Mar-97	350 km, 51.6 deg	[15-16]
MIR/EXEQIII	EXP	32Mbit	DRAM4M4	SMJ416400	TI	Oct-95	Mar-97	350 km, 51.6 deg	[15-16]
MIR/EXEQIII	EXP	64Mbit	DRAM64M	IBM50G6269	IBM	Oct-95	Mar-97	350 km, 51.6 deg	[15-16]
MIR/EXEQIV	EXP	1Mbit	SRAM128K*8	MT5C1008	MICRON	Jul-98	Aug-99	350 km, 51.6 deg	[16]
MIR/EXEQIV	EXP	8Mbit	SRAM512K*8	HM628512	HIT	Jul-98	Aug-99	350 km, 51.6 deg	[16]
MIR/EXEQIV	EXP	8Mbit	SRAM512K*8	M5M5408		Jul-98	Aug-99	350 km, 51.6 deg	[16]
MIR/EXEQIV	EXP	8Mbit	SRAM512K*8	KMC684000	Samsung	Jul-98	Aug-99	350 km, 51.6 deg	[16]
MIR/EXEQIV	EXP	8Mbit	DRAM1M4	EDI441024		Jul-98	Aug-99	350 km, 51.6 deg	[16]
MIR/EXEQIV	EXP	32Mbit	DRAM4M4	SMJ416400	TI	Jul-98	Aug-99	350 km, 51.6 deg	[16]
SAC_C/ICARE	EXP	32Mbit	DRAM4M4	SMJ416400	TI	Nov-00	Jun-02	707km, 98.2 deg	[22]
SAC_C/ICARE	EXP	512Mbit	DRAM16M*4-3.3V	KM44V16004	Samsung	Nov-00	Jun-02	707km, 98.2 deg	[22]
SAC_C/ICARE	EXP	256Mbit	DRAM16M*4-3.3V	HM516405	HIT	Nov-00	Jun-02	707km, 98.2 deg	[22]
SAC_C/ICARE	EXP	128Mbit	DRAM8M8	0165805	IBM	Nov-00	Jun-02	707km, 98.2 deg	[22]
SAC_C/ICARE	EXP	24Mbit	SRAM512K*8	HM628512	HIT	Nov-00	Jun-02	707km, 98.2 deg	[22]
SAC_C/ICARE	EXP	24Mbit	SRAM512K*8-3.3V	KM684000	Samsung	Nov-00	Jun-02	707km, 98.2 deg	[22]
SAC_C/ICARE	EXP	256Kbit	SRAM32K*8	HM65656	MHS	Nov-00	Jun-02	707km, 98.2 deg	[22]
MPTB/neural b.	EXP	256Kbit	SRAM32K*8	HM62256	HIT	Apr-98	Apr-02	1220*39200km,63.6 deg	[17-18]
MPTB/neural b.	EXP	256Kbit	SRAM32K*8	HM65756	MHS	Apr-98	Apr-02	1220*39200km,63.6 deg	[17-18]
MPTB/DRAM b.	EXP	1Gbit	DRAM4M4	uPD4217800	NEC	Nov-97	8/1/99*	1220*39200km,63.6 deg	[19-20]
MPTB/DPRAM b.	EXP	2Mbit	SRAM32K*8	M65656	MHS	Mar-98	Mar-99	1220*39200km,63.6 deg	[21]
MPTB/DPRAM b.	EXP	1Mbit	DPRAM16K*8	7006	IDT	Mar-98	Mar-99	1220*39200km,63.6 deg	[21]
MPTB/DPRAM b.	EXP	1Mbit	DPRAM8K*16	70V25	IDT	Mar-98	Mar-99	1220*39200km,63.6 deg	[21]

Both SRAMs and DRAMs have been flown, the latest experiments fly 4M SRAMs and 64M DRAMs. Only a few information is available on EEPROMs. No flight data has been published on flash EPROMs and SDRAMs.

2.2 Trends Observed (summary)

2.2.1 Spatial Location of upsets & daily and orbital variation of the upset rates

Most of the data available are on parts that are sensitive to both heavy ion and proton induced upsets. All the data available for all orbits exposed to trapped protons show a high correlation with proton flux contours of standard AP8 models. LEO orbits with high inclination are exposed to GCR and Solar particles in the high latitude regions of the orbit. Low altitude (< 500 km), low inclination (<30 degrees) orbits show a little exposition to GCR and solar particles.

2.2.1.1 Example 1: SEASTAR, LEO polar orbit

Fig. 4 shows the location of upsets accumulated from January 1999 to June 2002 on the SEASTAR spacecraft. We see a high density of trapped proton induced upsets in the SAA, the GCR and solar particle induced upsets are located on high latitude regions of the orbit.

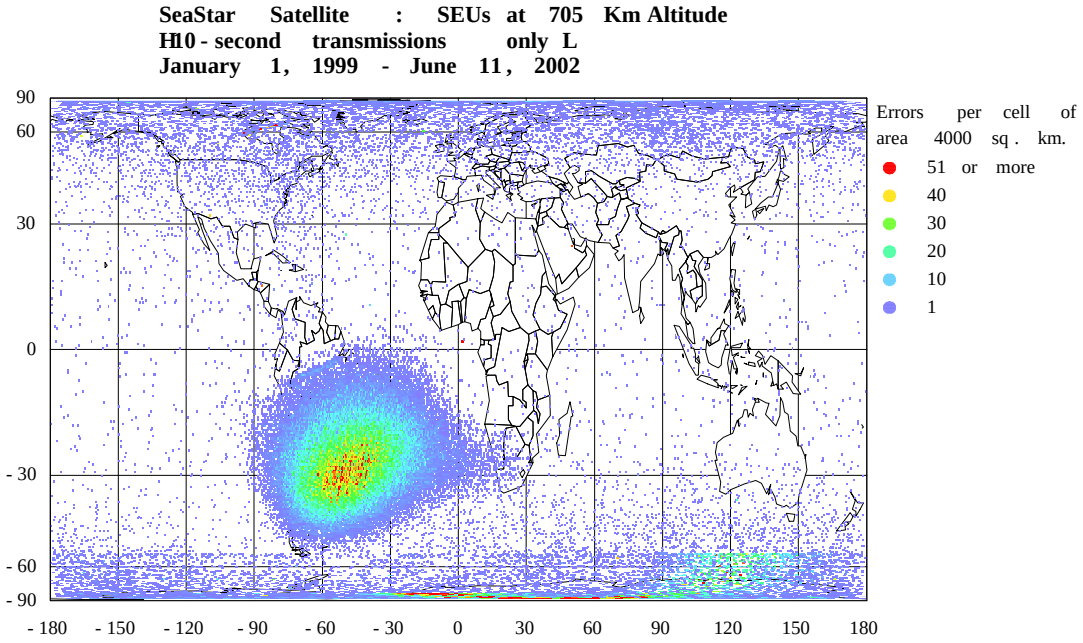

Fig 4: SEU density plot on SEASTAR FDRS from January 1999 to June 2002.[53]

Fig. 5 shows the location of the upsets during a typical day (July 13, 2000). More than 80% of the SEUs occur in the SAA and the others are induced by the Galactic Cosmic Rays in the high latitude regions. We can see that the upsets appear in bursts because 80% of the upsets occur in the SAA where the spacecraft spends only 5% of its time. Fig. 6 shows the location of the SEU on July 13 and July 14, 2000. On July 14, 2000 we observed one of the main solar events of the current solar cycle. We can see in Fig. 6 that the number of SEU that occur in the SAA is similar for the two days, but the number of SEU in the high latitude regions is significantly higher on July 14, 2000.

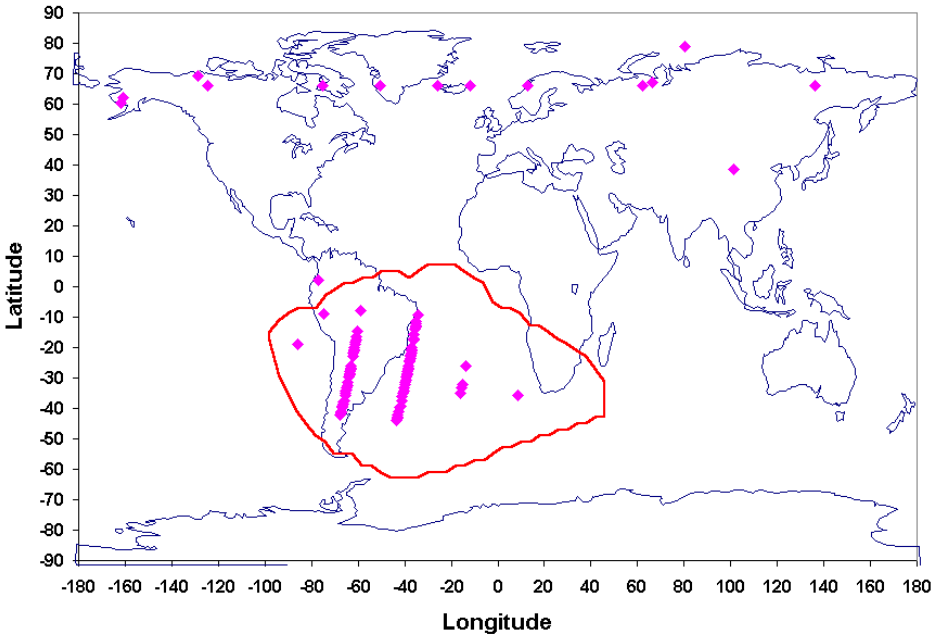

Fig. 5: SEASTAR FDR, SEU location on a typical day (July 13, 2000). [53]

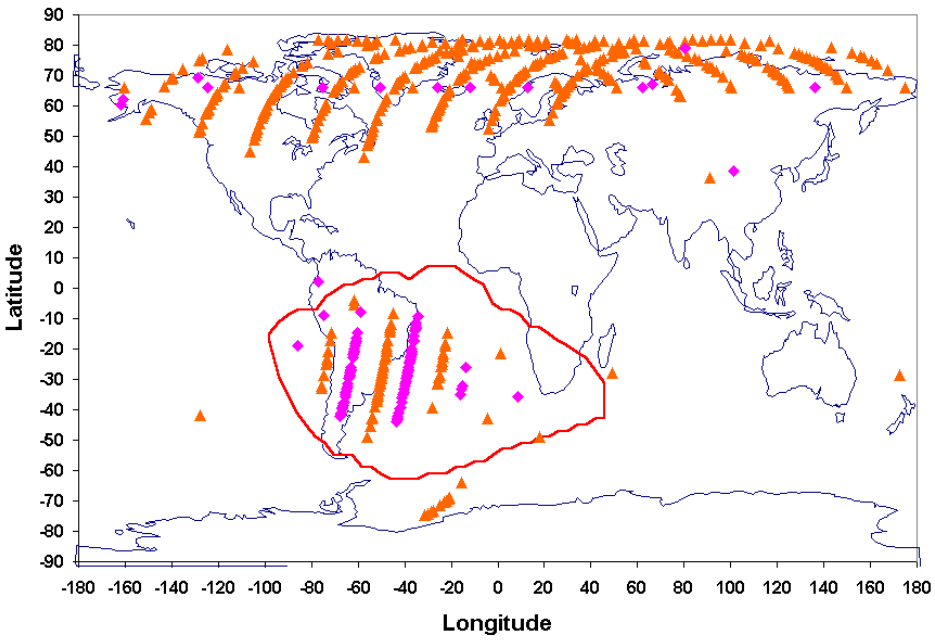

Fig. 6: SEASTAR FDR location of SEU on July 13 (magenta circles) and July 14, 2000 (in orange triangles). [53]

2.2.1.2 Example 2: LEO elliptical orbit APEX/CRUX experiment

The APEX/CRUX orbit with a perigee of 362 km and an apogee of 2544km with an inclination of 70 degrees allowed a mapping of the upset rates in nearly the whole trapped proton belt [11-13]. The SEU rates in the trapped protons belts vary significantly with the altitude as shown in Fig 7 to 9. These figures show the 1M SRAM HITACHI 628128 SEU rates and location for different altitude ranges.

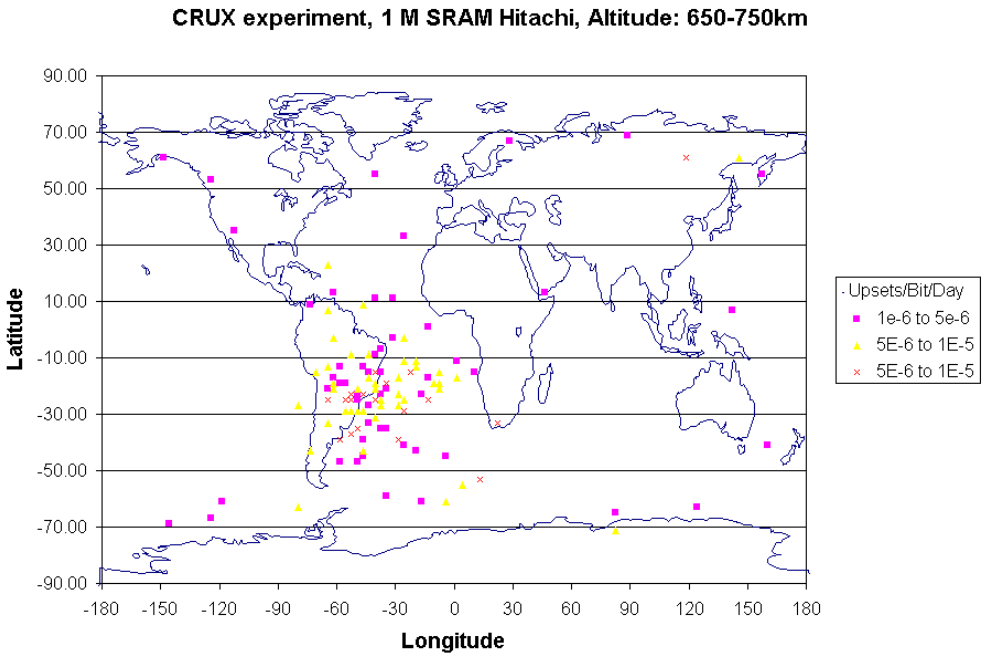

Fig. 7: CRUX experiment SEU location and upset rates for the 1M SRAM HITACHI 628128 and the 650 km to 750 km altitude range.[13]

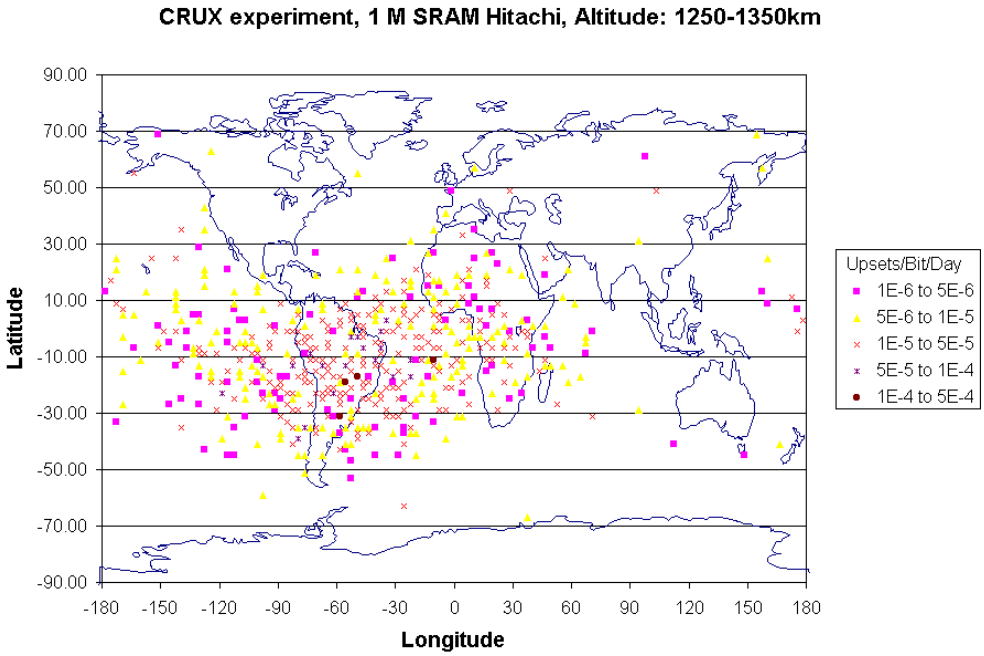

Fig. 8: CRUX experiment SEU location and upset rates for the 1M SRAM HITACHI 628128 and the 1250 km to 1350 km altitude range.[13]

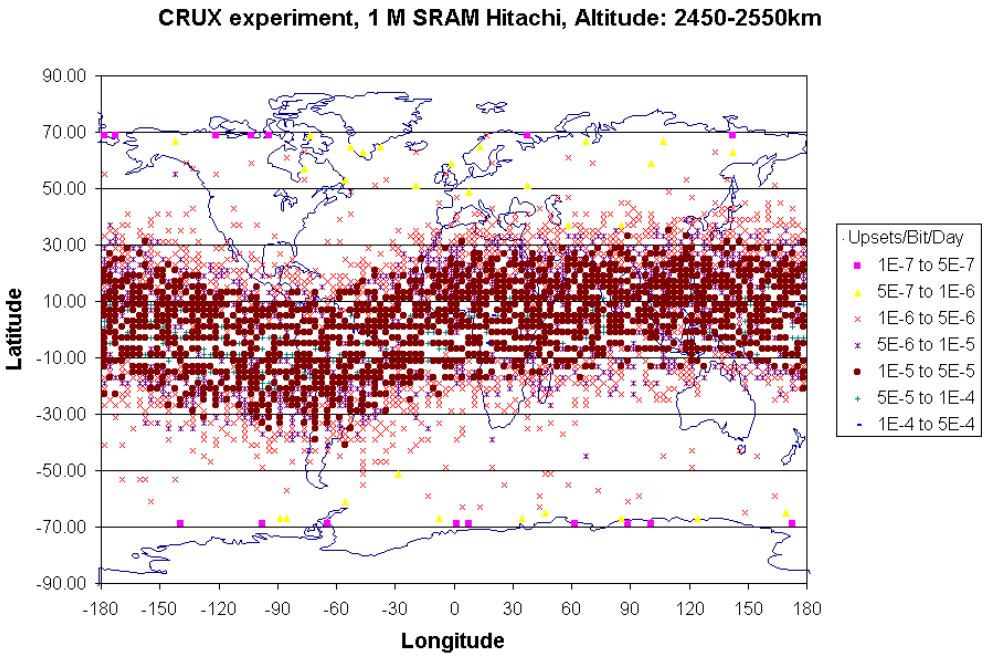

Fig. 9: CRUX experiment SEU location and upset rates for the 1M SRAM HITACHI 628128 and the 2450 km to 2550 km altitude range.[13]

The upset rates at all altitudes show a high correlation with proton flux contours of the standard model AP8. At 700 km, the trapped protons induced SEU are located in the SAA. Then the SEU contours extend with the increasing altitude.

The effect of altitude on SEU rates can be clearly seen from these figures. At 1300 km the SEU rates are eight to eleven times higher than at 700 km. At 2500 km, they are twenty to thirty times higher. The 2500 km altitude is close to the peak of the proton population.

2.2.1.3 Example 3: LEO low altitude, low inclination, X-ray Timing Explorer (XTE)

X-ray Timing Explorer (XTE) is a LEO 573 km altitude, 23 degrees inclination orbit, but is losing altitude as its orbit decays over time. In Fig. 10, the monthly average of the number of SEU/day and the spacecraft altitude are plotted for the period from July 1996 to July 2002. XTE spacecraft is losing altitude with time. We can see in Fig. 10 the decrease of the upset rates with the decreasing altitude. In July 1996, the spacecraft altitude was about 573 km and the average SEU rate was 250 SEU/day. In July 2002, the spacecraft altitude had decreased to about 520 km, and the average SEU rate was 70 SEU/day.

This data illustrate the large variation of the trapped proton fluxes, and therefore the SEU rates, with the altitude in this low altitude range.

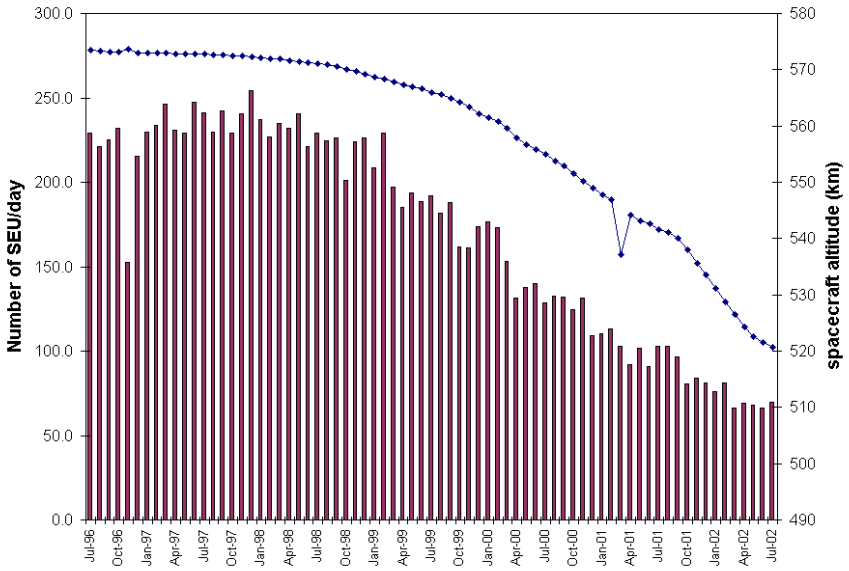

Fig. 10: XTE SSR flight data, plot of the monthly average of the number of SEU/day, and of the spacecraft altitude versus time from July 1996 to July 2002.[53]

2.2.2 Effect of space weather on the SEU Rates

2.2.2.1 Solar Events

Solar Particle Events (SPE) may have a significant impact on the upset rates.

A high sensitivity to high-energy solar particles have been observed on all spacecraft exposed to the solar particles during solar max activity. The impact of SPE varies with the exposition to the solar particles (type of orbit and shielding) and also the type of device.

- LEO polar or high inclination orbits: Argentinean Earth observation satellite, Influence of Space Radiation on Advanced Components (SAC/ICARE) [22], UoSAT satellite [3-4], Solar Anomalous Magnetospheric Particle Explorer (SAMPEX) spacecraft [1-2], Marine Observation Sate1lite-1 (MOS-1) [9], SEASTAR Spacecraft [53]
- GTO: Microelectronics and Photonics Testbed (MPTB) [18,20]
- GEO: ETS-V 64-kbit SRAM [9]
- L2: Solar and Heliospheric Observatory (SOHO) [3]

No sensitivity to SPE was reported on

- low altitude low inclination orbits: MIR space station [14-16], XTE [53]

As an example Fig. 11 shows the daily SEU counts on SEASTAR SSR from January 1999 to June 2002. We can see that 5 solar events have induced an increased SEU number on the SEASTAR SSRs. Other solar events have been observed during this period but only the events with a significant increase of high energy protons (>60-100 MeV) have induced increased SEU rates on SEASTAR SSRs.

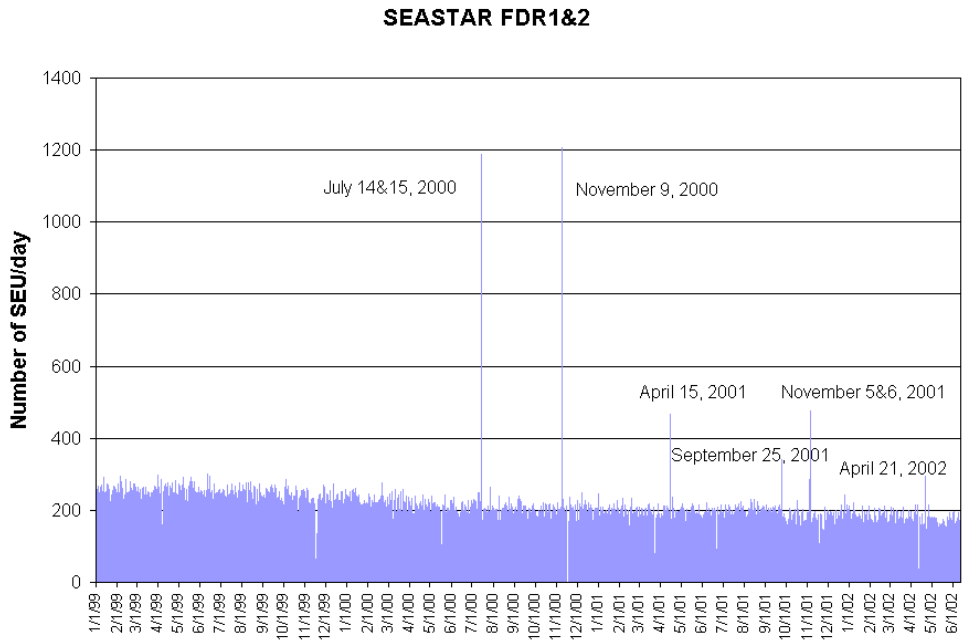

Fig. 11: Daily SEU rates on SEASTAR SSR from January 1999 to June 2002.[53]

Fig. 12 shows the proton spectrum composition of these 5 solar events (July 14 2000, November 9 2000, April 15 2001, September 25 2001, and November 5 2001) as given by the measurement from the GOES spacecraft. Fig. 13 plots the SEU rates and the >100 MeV proton fluxes these days. We can see a good correlation of the SEU rates with the >100MeV proton fluxes.

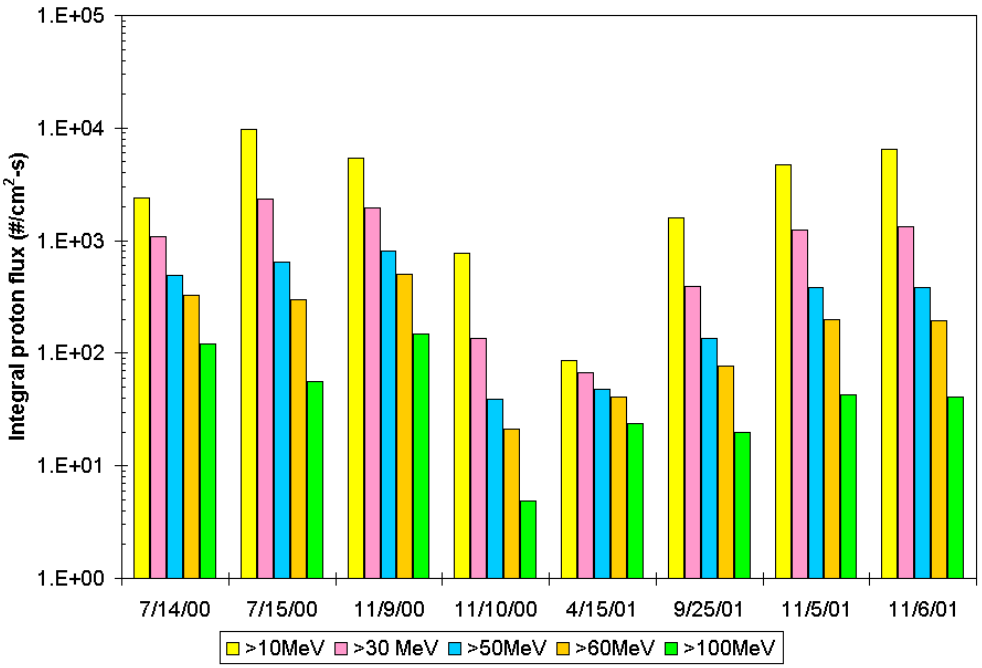

Fig. 12: Proton Spectrum composition of the main solar events of the current solar cycle.[53]

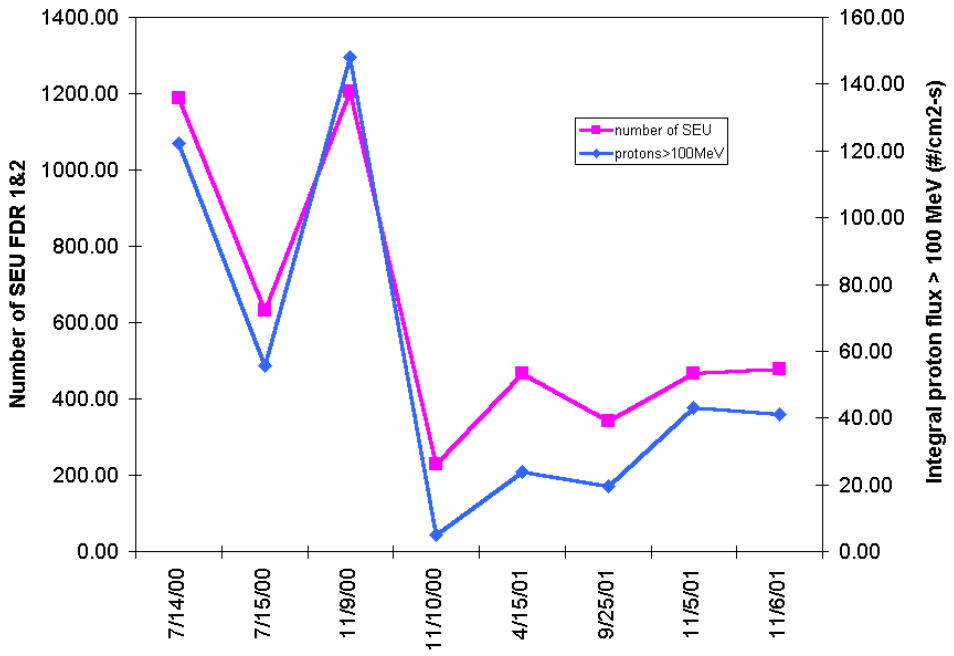

Fig. 13: SEU rates on SEASTAR SSRs and solar proton >100 MeV fluxes during the main solar events of the current solar cycle.[53]

SAC/ICARE flight data has also shown a correlation of the SEU rates during a SPE with the >80 MeV proton fluxes [22]. This illustrates the fact that the solar proton spectrum is much softer than the GCR proton spectrum and therefore an accurate shielding analysis is important to predict accurately the SEU rates during a SPE.

2.2.2.2 Solar cycle modulation

In agreement with the environment models, the data collected on a sufficient number of parts and a sufficient duration shows the modulation of the particle fluxes (GCR and trapped protons) and therefore the SEU rates with the solar activity.

Fig. 14 shows the monthly averages of the daily SEU rates observed on the SEASTAR SSRs and the smoothed sunspot numbers that give an idea of the solar activity. We can see, as expected, the decreasing SEU rates with the increasing solar activity. Another example of the modulation of the trapped proton fluxes is shown in the MOS1 data for the previous solar cycle (cycle 22) [9].

SOHO data [3] illustrates the modulation of the GCR background, with a decline of the SEU rates as solar maximum approaches (solar cycle 23).

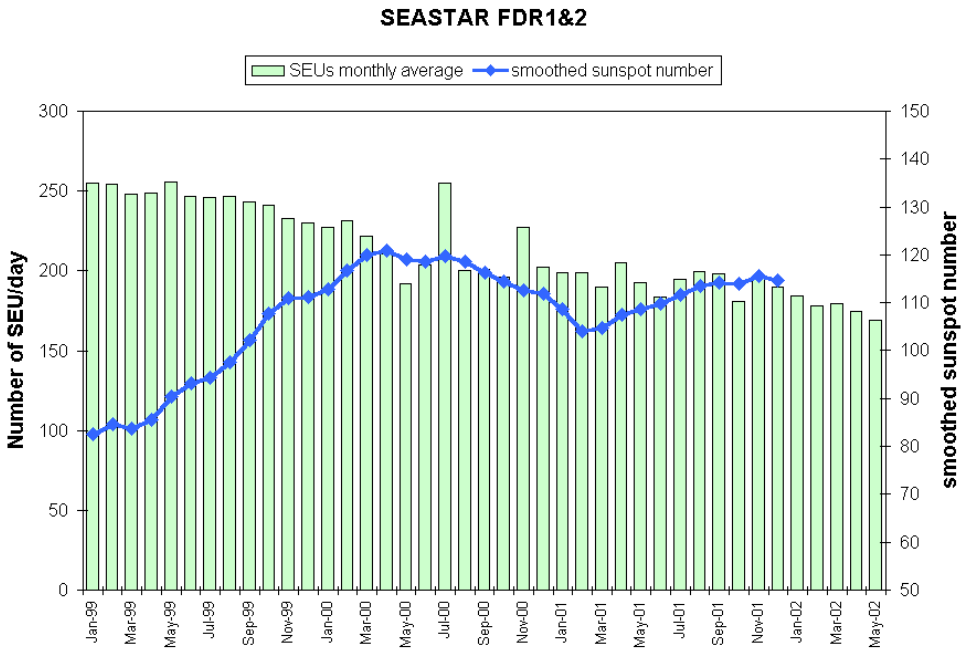

Fig. 14: Monthly averages of the daily SEU rates on SEASTAR SSRs and smoothed sunspot numbers.[53]

2.2.3 Other SEU observations

2.2.3.1 Part to part dispersion

Large part-to-part dispersion of the SEU sensitivity (up to a factor 12) has been observed on several experiments (Cosmic Ray Upsest Experiment, Advanced Photovoltaic and Electronic Experiments (CRUX/APEX), Korean Institute of Technology Satellite (KITSAT), EXEQ experiment flown on the MIR Space station (MIR/EXEQ), EXEQIII experiment flown on the MIR Space station (MIR/EXEQIII)). The main factor is the actual part-to-part dispersion as illustrated by the CRUX analysis [12, 13] and the results of the retest of flight part of MIR/EXEQ flight parts [15, 16]. This illustrates the poor fidelity of a test on 2 or 3 parts.

Another factor that may impact the SEU sensitivity is the exposition to the radiation environment (shielding) [12,13].

2.2.3.2 Pattern sensitivity

Flight data of memory experiments has shown that SRAM cells can have a different SEU sensitivity depending of the cell programmed state. The worst case was observed on the CRUX experiment for the MICRON 1M SRAM where 98% of SEU were bit flips from 1 to 0, and only 2% of SEU were bit flips from 0 to 1. Other devices did not show any effect of the programmed logic state, like the Electronic Designs, Inc. (EDI) SRAM [11-13]. This pattern sensitivity is easily detected during ground testing.

DRAM cells can only be upset when the cell capacitor is in the charged state. The charged state for some cells corresponds to a logic level of 1 and for other cells it corresponds to a logic level of 0. Because of this a memory cell has a bit flip from 1 to 0 when the charged state corresponds to a logic level of 1, and bit flip from 0 to 1 in the other case. Generally half of the memory bits are at a logic level of 1 and the other half at a logic level 0 when the capacitor is charged. In this case no pattern dependence is observed with standard tests pattern. If this is not the case, like in the 4Mbit DRAM from TI, both flight and ground test data show a strong pattern dependence [15].

2.2.4 Other radiation effects

2.2.4.1 MBU

Generally for SSR and OBC memories, only the critical MBUs (for example the Single-word, Multiple-bit Upset, SMU) that caused an uncorrectable error can be identified. On memory experiments because of the fast scrubbing rates, it is generally possible to identify the MBU, and their size [14-19, 22]. When the memory mapping was known, it has also been possible to identify the mechanism that caused the MBU. In the MPTB DRAM experiment, MBU caused by ions impacting a memory device at grazing incidence, and MBU row errors caused by an ion impact in the memory control circuitry have been clearly identified [19]. This MBU flight data is extremely important because it is often very difficult to analyze the ground test data (because of the accelerated flux) and or simulate the space environment during ground testing (for example the effect of ions at grazing incidence).

The ratio MBU versus SEU varies from about 1% to 20% depending on the device type and orbits. As expected, DRAMs are more prone to MBU than SRAMs. The more recent memories (4M SRAM, 16M and 64M DRAM) do not show an increased MBU sensitivity. The most sensitive MBU device is the SMJ416400 16M DRAM from Texas Instruments with a ratio MBU versus SEU of about 20% [15,16,22]. On 64M DRAMs this ratio varies from 2 to 10% [22]. The ratio of MBU to SEU of the 1M SRAM MT5C1008 from MICRON is about 10%. It is less than 5% on three different types of 4M SRAMs [16,22]. However, ground test data shows that the percentage of SMU (that may cause critical errors in systems) seems more important in recent memories [25]. The flight data does not seem to confirm this but statistics is very low.

All flight data show that protons can induce MBU, but the largest clusters of upsets and the highest ratio MBU versus SEU is obtained with heavy ions. For example on the MPTB DRAM experiment, the ratio MBU to SEU is about 20% outside the proton belts and about 8% inside the proton belts.Most of the MBU are double bit upsets [19].

2.2.4.2 SEFI

Sometimes, MBU block errors cannot be cleared by rewriting the locations with new data; they are cleared by cycling the power or resetting the device. This type of error may be viewed as a type of SEFI. This type of event has been observed in flight on the Hubble Space Telescope (HST) SSR. This error has been attributed to a proton-induced error in the internal redundancy latch of each DRAM memory device [54]. This sensitivity was identified during preflight heavy ion testing, but proton testing did not show any sensitivity. Therefore the SEFI problem was considered as a non-issue for the HST mission.

Further proton testing on a large number of devices (100 parts) was performed after the anomaly was detected in flight. The results showed SEFI block errors, and the predicted rates based on the measured cross section and the HST environment were within the same order of magnitude as the observed in-flight rate. This is another interesting example of the poor fidelity of a test on 3 devices for a system that uses 1440 devices.

2.2.4.3 SHE

Stuck bits were reported on SRAM 256K and 1M devices on the CRUX/APEX [11-13], and the MPTB neural board experiments [17,18]. The stuck bits resume normal operations on their own after a period of time ranging from minutes to several months [11-13, 17, 18]. On MPTB, bursts of stuck bits were observed during some solar particle events (November 1998, November 2001). On MPTB the Stuck bit rate has also increased with the increased time, and then the increasing dose [18]. All these observation lead us to the conclusion that these stuck bits are due to micro dose effect mainly induced by heavy ions. No SEGR has been identified in flight.

Other experiments, using SHE sensitive devices, did not show any in-flight sensitivity [3,4,5]. Ground testing data has shown that more recent SRAM and DRAM are less sensitive to SHE. This is confirmed by the flight data [6, 22].

2.2.4.4 SEL

SEL are reported on the 64K SRAM uPD4464 from NEC on the ETS-V spacecraft [9]. 2439 SEL during about 10 years have been observed. SEL ground testing showed this extremely high sensitivity of this part with a SEL LET threshold less than 1 MeVcm^2/mg.. The SEL rates were calculated with Cosmic Ray Effects on Micro-Electronics Code update 96 (CREME96) assuming a shielding thickness of 21mm Al, and a worst case thickness of the sensitive volume of 1 μm. The predictions overestimate the flight rates by a factor 4 for the background

environment. The predictions give accurate estimations of the SEL rates during the solar events with the CREME96 worst week and worst day solar event models.

A proton induced SEL has been reported on the same memory device on an instrument of the ERS-1 satellite [26].

One possible occurrence has been reported on a 256K SRAM from IDT on the CRUX experiment. SEL were observed on this part during ground tests [12-13].
No other SEL occurrence has been observed.

2.2.4.5 TID

No TID induced failure has been reported. After 10 krad(Si) accumulated on the S80 SSR, the current drawn from the 5V supply has doubled [3-5]. On MPTB, the stuck bit rate has also increased with the increased time as the memory cells accumulate dose [18].

2.2.5 Comparison of SEU rates with prediction

2.2.5.1 Introduction

Significant uncertainties are involved in SEU rate prediction:

- The uncertainty in the radiation environment (radiation models and shielding assumptions)
- The uncertainty in the SEU characterization.
- The uncertainty in the sensitive volume thickness.

Considered these large uncertainties in this calculation, it is generally considered that an accurately calculated SEU rates predict the average flight rates over a long period of time within one order of magnitude. Because of the conservative assumptions that are made for these calculations, the calculated rates generally overestimate the actual flight rates, but this is not always the case. In 13 cases out of the 53 cases analyzed, the actual SEU rates have been underestimated.

2.2.5.2 SRAMS

Generally the event rates predict the flight rate within a factor 5. In some cases, large overestimations are observed:

- Proton rate predictions: a factor 55 overestimation on the 256K SRAM from EDI on CRUX, a factor 6 overestimation on the 256K SRAM from IDT on CRUX [11-13], and a factor 15 overestimation on the 256K SRAM from Sony on S80 [3-5] is reported. In these three cases, only partial proton test data was available (only one data point for CRUX memories) and a Bendel fit has been used to calculate the upset rate. This shows the importance of collecting proton test data in addition to heavy ion test data. Inaccurate shielding thickness assumptions may have also played a role in these large overestimations.
- Heavy ion rate predictions: a factor 10 overestimation on the 256K SRAM from Micron, and a factor 100 overestimation on the 256K SRAM from EDI is reported on CRUX data [11-13]. Flight data show a factor 12 device to device variation in the SEU rates on EDI 256K SRAM, a factor 2 on Micron 256K SRAM, and both devices exhibit significant pattern sensitivity. In addition, test data has not been taken on the flight lots. Poor test fidelity seems to be the main cause of these discrepancies.

Table 2 lists the cases where the calculated rates underestimate the actual flight rates. In all but 2 cases, the predictions are within about a factor 5 with the flight rates. Three different missions are concerned: S80, KITSAT, and MIR/EXEQIV. For these three missions, most of the predictions are underestimated. On S80 and KITSAT, trapped protons dominate the radiation environment. One possible cause of the underestimation is an overestimation of shielding thickness. But in the two large cases of underestimation (CXK58001 on KITSAT, CXK58257 on S80), an inaccurate SEU characterization is suspected. Flight data on the CXK58001 show a factor 10 device per device variability. On MIR/EXEQIV, either protons or heavy ions dominate the part response depending on the part type. For proton dominated responses, possible causes of these underestimations are an overestimation of the shielding thickness, and/or an underestimation of the proton fluxes at low altitude by the AP8 solar maximum model [55]. For heavy ion dominated responses, a possible cause of the underestimation is the use of the old CREME model, with the weather index M=1 (average flux) at solar maximum.

Table 2: list of the cases where the calculated SEU rates underestimate the actual flight rates.

Mission	Manufacturer	Function	Device type	Solar activity	ratio predicted/ observed	predominant source of SEU	Comments
S80T/SSR	NEC	SRAM128K*8	D431000	solmin	0.37	protons	protons prediction only
S80T/SSR	Sony	SRAM32K*8	CXK58257	solmin	0.14	protons	protons prediction only
S80T/OBC	Sony	SRAM128K*8	CXK51000	solmin	0.25	protons	protons prediction only
KITSAT-1/SSR	Sony	SRAM128K*8	CXK58001	solmin	0.07	protons	protons prediction only; 10:1 device/device variability
KITSAT-1/OBC	Sony	SRAM128K*8	CXK581000	solmin	0.22	protons	protons prediction only
UOSAT-5/SSR	NEC	SRAM128K*8	D431000	solmin	0.21	protons	protons prediction only
MIR/EXEQIV	MICRON	SRAM128K*8	MT5C1008	solmax	0.59	heavy ions	
MIR/EXEQIV	HIT	SRAM512K*8	HM628512	solmax	0.17	heavy ions	
MIR/EXEQIV		SRAM512K*8	M5M5408	solmax	0.63	heavy ions	
MIR/EXEQIV	Samsung	SRAM512K*8	KMC684000	solmax	0.19	protons	

2.2.5.3 DRAMS

Fewer data is available to compare DRAM flight upsets rates to predictions. We have this information for:

- SOHO SSR [3] and MIR/EXEQ [16] where the heavy ion induced upsets are dominant
- MPTB DRAM experiment [19, 20] and APEX SSR [7] where the proton induced upsets are dominant.

Proton rates predictions give an estimation of the flight rate within a factor 2 [7,20]. In both cases proton test data was available for at least three energy points.

Heavy ion rates give an estimation of the flight rates within a factor 5. But larger discrepancies were reported when the assumption of the sensitive volume (SV) thickness was too conservative. For example, for the 16M DRAM flown on MIR/EXEQ the calculated rate overestimates the actual flight rate by a factor up to 45 when a 2μm thickness of SV is assumed. When a more realistic thickness of SV is assumed (7 μm), the overestimation is reduced to a factor 4 [16]. If the conservative assumption of a "standard" SV thickness of 2 um works well for SRAMs, it may be too conservative for deep SV of DRAMs.

Table 3 lists the cases where the calculated rates underestimate the actual flight rates. In all cases, the predictions are within about a factor 5 with the flight rates. Like for SRAMs flying in the same missions, the main cause of the underestimation is possibly the environment models (proton and heavy ions) and the shielding assumptions. In addition, for the 64M DRAM IBM50G6269 flown flown on MIR/EXEQIII, the flight data statistics is too low to draw definitive conclusions.

Table 3: list of the cases where the calculated SEU rates underestimate the actual flight rates.

Mission	Manufacturer	Function	Device Type	Solar Activity	Ratio Predicted/ Observed	Predominant Source of SEU	Comments
MIR/EXEQIII	IBM	DRAM64M	IBM50G6269	solmin	0.34	protons	low flight data statistics (2 events)
MIR/EXEQIV	EDI	DRAM1M4	EDI441024	solmax	0.30	heavy ions	
MIR/EXEQIV	TI	DRAM4M4	SMJ416400	solmax	0.65	heavy ions	

2.2.5.4 Prediction of SEU rates during SPE

Comparison of calculated rates with actual rates during SPE has only been done for SOHO SSR [8] and MPTB DRAM experiment [20]. Orders of magnitude overestimations of the July 14, 2000 event upset rates are reported when the CREME96 solar event environment models were used.

In both cases the background environment rate has been predicted within a factor 2. The proton spectrum of CREME96 model is based on October 89 solar event and is similar to proton spectrum of July 14, 2000 solar event. One possible explanation is the difference in the heavy ion LET spectrum as shown in Fig 15 that compares the CREDO measurements on MPTB [56] to the CREME96 worst day model LET spectrum. Rates calculated with this measured spectrum are in good agreement with the observed rate on MPTB during the July 14 solar event [20].

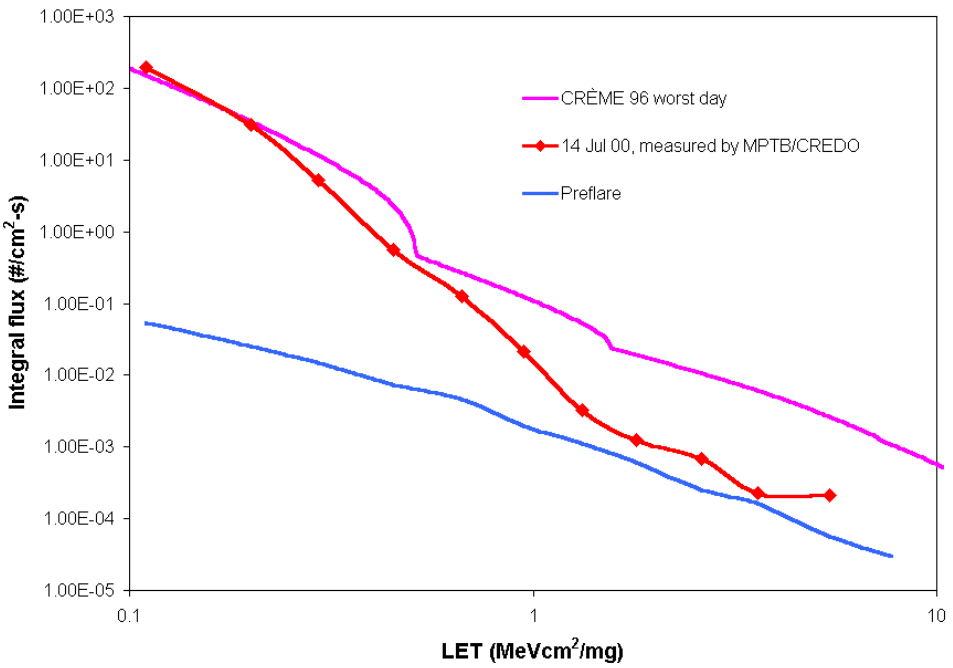

Fig. 15: Comparison of the CREME96 worst day model LET spectrum with the measured LET spectrum on CREDO-3/MPTB on July 14, 2000.[20]

Another cause of error during a solar flare is an inaccurate estimation of the shielding. Generally upset rates are calculated for a conservative value of shielding (100 mils, 1g/cm^2 of Al). This is often sufficient to calculate GCR and trapped protons induced SEU rates, but this could lead to large errors in the calculation of solar particle induced SEU rates, because of the "softer" solar particle spectra. SEASTAR analysis (see Fig 13) shows that only high-energy protons (>80 MeV) create an increased SEU rate; the same conclusion has been reached in SAC/ICARE experiment [22]. The MPTB prediction that gives a good agreement with July 14, 2000 event rates has been made with a reasonably accurate model of the shielding.

2.3 Flight Studies 2002-2012

This period saw only two on-orbit studies of radiation performance of SSRs.[67, 71] Schaefer et al.[71] compared on-orbit SEU rates for three die revisions of a 64-Mbit, a 128-Mbit and a 256-Mbit memory die. Environments considered include Low-Earth Orbit (LEO) and interplanetary (Mars Reconnaissance Orbiter) The study found that the ratio of predicted rates to observed on-orbit rates varied from about 1 to 10, and showed no systematic trend with memory density or feature size. No strong correlation was seen between error rate and solar activity, other than the expected effects of the solar cycle on GCR rates. No data were presented for other error modes (e.g. SEFI, burst errors). Reference 67 compared on-orbit rates for SEU, block errors to rates estimated with laboratory data and placed upper limits on the on-orbit rate for SEFI (zero events observed). This work found that on-orbit and estimated SEU rates agreed within a factor of 3, while rates for block errors deviated by more than an order of magnitude. It is likely that the poor agreement for block errors is mainly due to poor statistics, since control logic generally has a larger feature size than the memory cells. Block errors are disruptive during testing, making it difficult to accumulate statistics, while shortcomings of the IRPP model are most likely to manifest at small feature sizes. Table 4 updates the comparison of on-orbit and predicted rates based on 2 additional years of LRO data. The good agreement (within a factor of 5) between predicted and observed SEU rates persists, but the discrepancy for logic and block errors also remains. In addition, the upper limit based for on-orbit data is now tighter than that based on data from the accelerator, and we have added an upper limit for stuck bits based on one candidate stuck bit in bank 2 of the LRO SSR.

Table 4: On-Orbit SEE Rates vs. Predicted Rates for a 512 Mbit SDRAM

Error Mode	Predicted #/dev-day	Observed #/dev-day
SEU	1.54E-02	3.10E-03
Logic Errors	1.00E-02	1.70E-04
Block Errors	3.50E-03	3.30E-05
SEFI	<0.000008	<6.4E-6
Stuck bits (permanent)		<1E-5

The increased importance of SEFI is also evident in the on-orbit data. For the LRO SSR, 14 events accounted for 90% of the corrupted data words during the first 3 years of the mission (see Fig. 16). As with the data from Reference 71, no strong correlation with solar activity is seen. However, the period of the LRO mission coincided with the end of Solar Cycle 23 and the beginning of the weak Solar Max of Cycle 24.

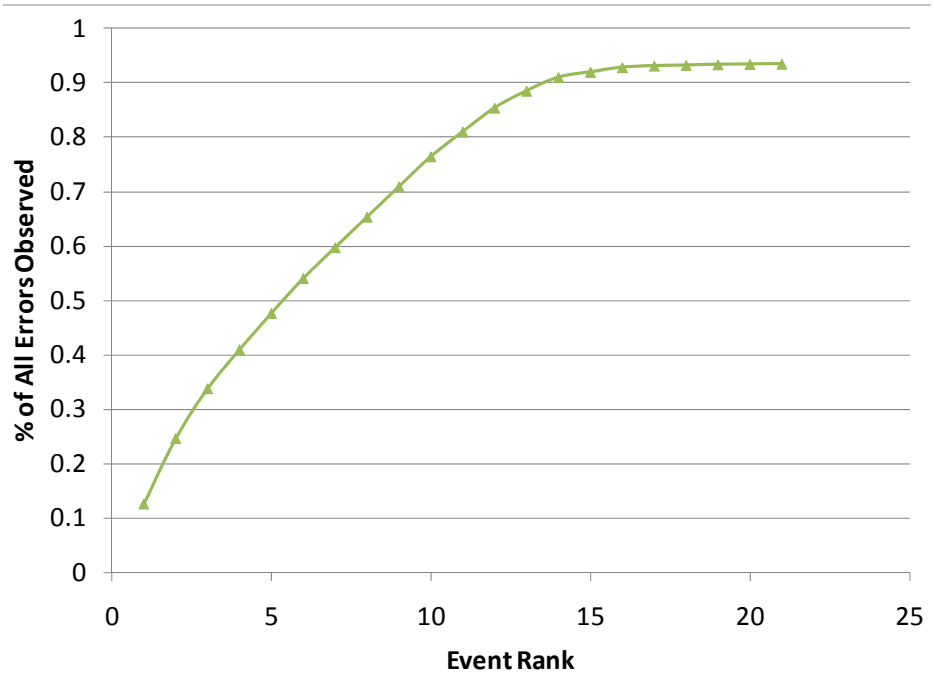

Fig. 16 For the data storage boards, just 14 errors accounted for over 90% of the bit flips observed during two years of operation in lunar orbit.

3 Mitigation techniques utilized

Error Detection and Correction (EDAC) coding schemes are used to protect the memories from the SEU. The memories are regularly scrubbed to prevent the accumulation of bit errors due to SEUs. Their content is read through the EDAC protection circuitry (to correct the errors) and written back, such that the corrected data are restored on a regular cyclical basis. Table 5 lists the different types of codes used in the data analyzed here.

Table 5: EDAC techniques used.

Spacecraft	Subsystem	EDAC code	Data word size (bits)	# code bits	Scrubbing rate (minutes)
SEASTAR	SSR	Hamming	8	4	
SOHO	SSR				29
S80T	OBC				8.5
KITSAT-1	OBC				8.5
UOSAT-5	OBC				8.5
UOSAT-2	OBC				
APEX	SSR		16	6	4
CASSINI	SSR		32	7	
SAMPEX	SSR				5
XTE	SSR				25
TOMS	SSR		64	8	0.27
FaSat-Bravo	OBC	Triple-Modular Redundancy (TMR)	8	16	13
Thai Phutt	OBC				13
UOSAT-12	OBC				13
S80T	SSR	Reed Solomon	252x8	3 x8	222
KITSAT-1	SSR				222
UOSAT-5	SSR				222
UOSAT-3	SSR				222
FaSat-Bravo	SSR				
Thai Phutt	SSR				
UOSAT-12	SSR1				
UOSAT-12	SSR2		252x8	4 x8	
HST	SSR		224x8	31 x8	32

One of the most popular EDAC codes is the Hamming code. This code is capable of single error correction and double error detection (SECDED)—that is, it can detect and correct any single-bit error and detect but not correct double bit errors in a data word. This simple technique has proved its effectiveness as long as a single particle does not cause multiple errors in a data structure, and the scrubbing rate is adequate to avoid coincidental but independent events in a data word. When this occurs the failure rate is virtually negligible. Two occurrences of high uncorrectable SEU rates have been reported. An unexpectedly high rate of uncorrectable double bit errors has been observed on the Cassini spacecraft solid state recorder (SSR) [52]. About two uncorrectable errors per day are observed, while virtually none were expected. An analysis has shown that these uncorrectable errors were due to the unusual architecture: one data word of 39 bits is stored in two passes to the 20-bit-wide memory architecture comprising five 1Mx4 DRAMs. The second pass accesses the very next 4 bit segment in each DRAM device. Unfortunately, each bit in the second segment is physically adjacent to the corresponding bit in the first segment. Thus, an MBU can corrupt 2 bits in the 39 bit word. This example shows that designers of space systems need to carefully consider how parts are being used in system architectures. Fig 17 shows the number of uncorrectable errors that have occured on the XTE SSR [53]. The rate is low and acceptable for the mission, but it is not negligible. The mission average ratio of uncorrectable errors versus SEU is about 0.4%. The cause of these uncorrectable errors is the SMU sensitivity of the HITACHI 1M SRAM device. The same device was flown in the CRUX/APEX experiment, and SMU were also reported [11-13]. This example shows that the risk of SMU needs to be carefully evaluated during ground testing.

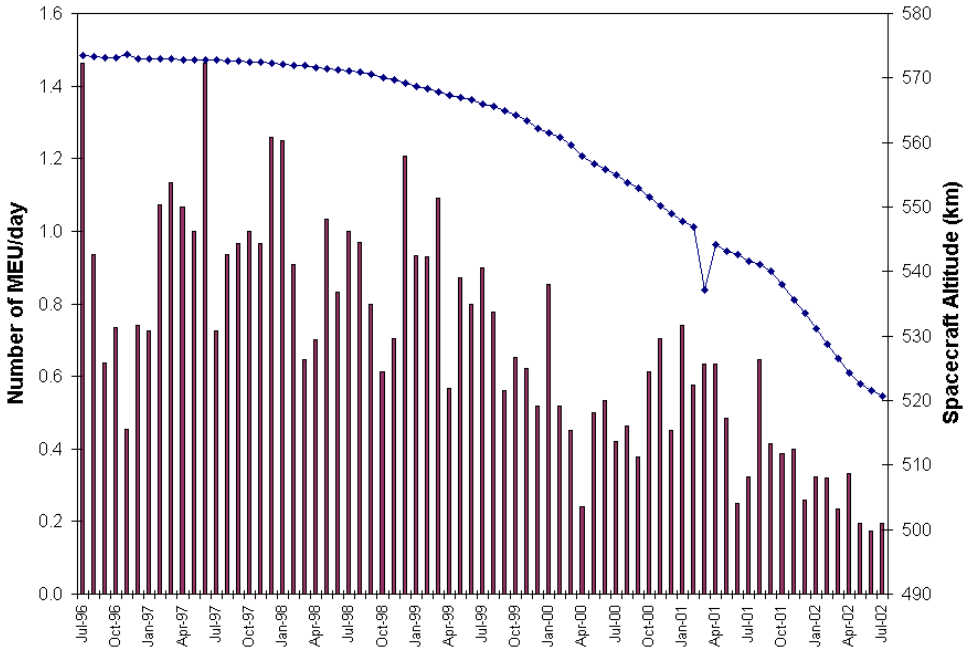

Fig 17: daily number (monthly average) of uncorrectable errors of the XTE SSR.[53]

All Surrey Space Center (SSC) OBCs that used the Hamming (12, 8) code scheme to protect their program storage memories did not have any SEU related problem [3-6]. As the SMU sensitivity has increased in state of the art memory devices, they decided to use a triple modular redundancy (TMR) hardware EDAC scheme to protect the OBC program memory of their most recent micro-satellites FaSat-Bravo, Thai-Phutt, and UOSAT12 [6]. With TMR, all the bits in three independent memory chips are compared and voted, so any number of flipped bits within a word can be corrected. This SEU mitigation scheme is very robust, but triplication represents a 200% storage overhead and is therefore is mainly appropriate for small program storage memories. For future systems, SSC will use a variant of the Hamming code, a (16, 8) code capable of detecting and correcting up to two bit errors per word. Based on their experience, they consider that this code will cope with the vast majority of SEU with only 50% memory overhead. The APEX/CRUX data on the Hitachi 1M SRAM indicated that all SMU were double bit errors [13]. The implementation of such a variant of Hamming code would have suppressed all the uncorrectable errors.

Reed Solomon (RS) EDAC codes are very powerful. NASA has developed a hardware RS (255,223) encoder that is able to correct up to 16 consecutive bytes in error [57]. The particular version used for the HST SSR is a RS (255, 224), which can correct up to 10 bytes in error in the 224-byte data structure. The large multiple bit errors observed on HST were fully correctable with this RS EDAC [54]. The old SSC spacecraft [3-6] used a less powerful version, RS(255,252) which involved less coding overhead for their SSRs. This version could correct 1 byte in error and detect 2 bytes in errors. These double byte uncorrectable errors are reported as severe errors in their data. Data shows a significant number of uncorrectable errors ranging from 1E-10 to 6E-10 per byte day [3-5]. In all cases the ratio of severe errors to correctable errors is less than 1%. In their last generation of micro satellites, Thai-Phutt and UOSAT12, SSC has implemented a RS(256,252) capable of double byte correction. Three or more bytes would have to be affected to cause a severe error under this scheme. With this new scheme the number of uncorrectable errors on UOSAT12 has been reduced from 2E-9 per bit day to 1E-10 per bit day. This represents a twenty fold improvement [6].

3.1 Mitigation 2002-2012

Radiation performance of the underlying memory drives SSR design. Table 6 illustrates the possible effects a memory can suffer, the mitigations used and the impact implementation of these mitigations on SSR design. In general, errors that severely affect SSR design cannot be accommodated, so it is essential to find a memory that has a sufficiently low rate for destructive SEL and for nondestructive SEL or SEFIs that would require a power cycle of the affected die for recovery. As indicated in the previous section, EDAC remains the key mitigation, with most additional mitigation measures (scrubbing, SSR architecture, bit interleaving, etc.) designed to ensure that errors do

not overwhelm the capability of the EDAC. One development in this regard has been that the increased importance of block errors and SEFI has necessitated greater use of EDAC with multi-bit correction capability. The decreasing availability of memory die organized in a ×4 configuration in favor of ×8 and ×16 configurations exerts pressure toward greater corrective capability as well.

The most important aspect of radiation performance to understand is that a single-event effect affects bits only on a single memory die. Thus, as long as data words have bits interleaved across different die such that a worst-case error mode that corrupts every bit on a given memory chip does not cause an error uncorrectable by EDAC, the SRR will be hard to any single SEE. If the bit error rate—that is the rate of data errors due to all SEE modes— is R then the rate of data loss will be proportional to the square of the (hopefully small) bit error rate, R. If the interleaving is such that the EDAC can correct two worst-case errors in two independent die, the SSR data loss rate will be proportional to R^3. EDAC can also be overwhelmed if errors accumulate over time. To avoid this, memory contents are scrubbed periodically, with the scrub period determined such that the probability of accumulating more than a single error during the period is negligible.

Errors that require a power cycle for recovery (e.g. nondestructive SEL or some SEFI) pose a special challenge for SSR design. Often, it is not possible to cycle power at the level of a single memory chip, a single stack of chips or even a single memory board. If this is the case, then in spite of the mitigations in place to deal with data errors, all data on the power-cycled parts can be lost. Mitigating this data loss can be very difficult—involving either the ability to cycle power to a single die or the use of spare memory to store and correct data while functionality of the affected block of memory is restored by power cycling. Such measures are costly in terms of power, space and potentially reliability. As such, it is highly desirable to base the SSR on a memory that is effectively immune to such disruptive errors on timescales relative to the mission duration.

Table 6: Consequences and Mitigation of Various Single-Event Effects

Radiation Risk	Consequence	Remediation	Impact to design
Destructive Single-Event Latchup (SEL)	Permanent loss of 1 die in memory array	Redundant die in array such that probability of meeting End-of-Life (EOL) requirements is high	Severe
Nondestructive SEL	Loss of all data on affected die/stack	Requires power cycle of affected die/stack for recovery	Moderate to severe
Single-Event Functional Interrupt (SEFI) requiring power cycle	Loss of functionality on affected die; Loss of most or all data on affected die/stacks	Requires power cycle of affected die/stack for recovery; EDAC may	Moderate to severe
Recoverable SEFI	Temporary loss of functionality; Loss of large amounts up to all data on affected die.	EDAC + Organzation of data words across independent die; FPGA programmed w/ ability to refresh mode registers/reset device	Moderate
Stuck Bits	Uncorrectable loss of data integrity in affected bits/symbols	EDAC can correct incorrect bit, but capability permanently degraded	Minor
Multi-Bit Single-Event Upset (SEU)	Correctable loss of data for multiple bits in same word	EDAC must have sufficient power to correct w/c MBU (usually no worse than w/c SEFI)	Moderate
Multi-Cell SEU	Multiple bits upset, but in different words	EDAC	Minor
SEU	single-bit upset	EDAC	Minor

4 Lessons learned

4.1 SEU rate

The main lesson learned is that there is large SEU sensitivity range from device to device type, and part to part for the same device type. There is also a large variation of sensitivity depending on the environment. When the flown device has been characterized both to heavy ion and protons, the calculated SEU rate is generally in good agreement with the observed average flight rate (within an order of magnitude) for the background environment. However, the standard assumption of a thin sensitive volume thickness of 2 μm is too conservative for some devices, especially DRAMs. It should also be noted that, despite all the conservative assumptions made for the predictions, these predictions are not always pessimistic. This is generally the result of inaccurate test data, or inaccurate modelization of the radiation environment.

The SPE CREME96 standard models (peak event, worst day, and worst week) give generally very conservative values of the upset rates during a SPE.

4.1.1 SEU rate: 2002-2012

The ever-shrinking geometries of DRAM cells have more than made up for the decrease in critical charge needed to cause SEU, resulting in per-bit SEU rates on the order of 10^{-13} to 10^{-11} per day. Reference 67 showed that with reasonable statistics, it was possible to estimate error rates within a factor of 5 of observed on-orbit rates. Unfortunately, for DDR2 and DDR3 device the DRAM cell sensitive volume deviates from a rectangular parallelepiped, so the cross section vs. LET curve does not follow the expected effective LET dependence. As such, rates estimated using CREME96 will be conservative. However, since SEU rates do not drive data corruption, these errors are not critical.

4.2 MBU

Flight data shows that the MBU rate is significant (up to 20% of the total event rate). SMU are generally detected during ground testing, but it is generally difficult to quantify accurately the risk because of the large anisotropy of the mechanisms involved [19, 39].

4.2.1 MBU:2002-2012

Although the small size of DRAM memory cells virtually guarantees that a single ion will cause multiple upsets, the interleaving of bits continues to provide significant immunity to multiple upsets in the same address. Even for ions incident at near grazing incidence, multi-bit errors due to upsets in memory are rare.[72] On the other hand, the increasing importance of block errors and SEFI means that most of the addresses with errors will have multiple bits flipped.

4.3 SEFI

SEFI events have been observed on flight on memories. Because of the low (but not negligible) sensitivity, these types of events can be incorrectly characterized during ground testing of a small number of parts.

4.3.1 SEFI: 2002-2012

As mentioned previously, SEFI and block errors (often also grouped with SEFI) have continued to increase in variety and rate as the control logic and functionality of SDRAMs has increased from single data rate through third generation double data rate. Even though their rates are relatively low (typically on the order of 10^{-5} per day), they can corrupt massive quantities of data, in many cases dominating the overall bit error rate for the memory, and in some cases resulting in loss of functionality that may require disruptive measures, such as refreshing control logic settings, resetting the part, resynching the clock and phase lock loop or even cycling power to the affected memory die. The need to accommodate such measures can drive the design of the SRR, so often it is advantageous to test several parts and select the one with the lowest SEFI rate—especially for SEFI that require a power cycle for recovery. Unfortunately, the rarity of these events, coupled with the disruptive measures needed for recovery also poses issues for SEE testing and rate estimation, since the statistics on which cross section estimations will be based will necessarily be small. In some cases only a single instance of a particularly disruptive SEFI mode may be seen—sufficient to alert one to the modes potential occurrence, but insufficient to estimate its rate. In the case of such rare but important error modes, single-event testing with a laser can supplement the data from heavy-ion testing

to facilitate understanding of how rare the error mode is and whether it is truly due to a single ion and not an accumulation of control logic errors. This knowledge can make the difference in some cases of whether the project lives with a small probability of a very costly error or decides to implement a costly and complicated mitigation scheme based on a necessarily conservative error rate estimate.

4.4 SHE

SHEs due to microdose deposition have been observed in flight. SHE can be detected during ground testing, but again it is very difficult to accurately quantify the risk.

No SHE due to SEGR has been identified. This risk can be detected during ground testing.

4.4.1 SHE: 2002-2012

SHE due to SEGR still have not been observed in ground testing or on orbit. However SHE due to microdose, also referred to as stuck bits, have been seen for most tests of SDRAMs up to and including DDR3. Thus far, the rate has not been so high as to pose a barrier to use of a memory in an SRR. SHE typically affect only a single bit, and this is easily handled by EDAC. The only effect of such errors is to degrade error correction capability for the affected address. If necessary, additional mitigation can be implemented for the affected address—e.g. not storing critical data at that address. Moreover, in many cases, stuck bits will subsequently anneal and perform normally after a few hours to a few days. In 2012, one stuck bit was observed on orbit for the LRO Data Storage Boards (DSB)

4.5 SEL

Only a few part types are sensitive to SEL, but one part has shown an extremely high heavy ion and proton induced SEL sensitivity [26]. This risk can be detected during ground testing.

4.5.1 SEL: 2002-2012

Beginning with the 256 Mbit generation of SDRAMs, SEL performance became a significant hurdle. All of the parts tested in this generation exhibited some susceptibility to SEL. The best option from this generation was a part from Hitachi/ElpidaHM5225405B. Although this part was SEL susceptible, the SEL mode was not destructive, and it also exhibited no evidence of damage under microscopic examination or after a 1000-hour post-SEL burn-in regime. This memory was the basis for the Mars Reconnaissance Orbiter SSR, the on-orbit performance of which is detailed in reference 71. The subsequent 512 Mbit part from Elpida was immune to SEL, and has been the dominant choice for SDRAM based SSRs since 2005. This includes the data recorder used on the Lunar Reconnaissance Orbiter (LRO), the on-orbit radiation performance of which is detailed in reference 67. No on-orbit SELs have been observed for these parts.

Subsequent generations of SDRAMs (DDR through DDR3) have seemed to show a decreasing tendency toward SEL susceptibility. DDR and/or DDR2 memories from both Elpida and Micron exhibited SEL susceptibility, while to date no DDR3 device has latched up under heavy-ion irradiation. While decreasing supply voltages may account for some of this increased immunity, it remains to be seen whether it will persist into future generations—or indeed even into future die revisions.

4.6 SEE mitigation schemes

The coding techniques have shown their efficiency to mitigate SEUs as long as the use of the parts has been carefully considered and the risk of SMU evaluated during ground testing.

Scrubbing rates are generally calculated on the basis of daily average SEU rates. This is adequate for GEO or interplanetary orbits in the absence of SPE. For LEO the data shows that the SEUs occur in burst when the spacecraft goes through the trapped proton belts. For example, on a LEO polar orbit, 80% of the SEU occur in the SAA in bursts lasting for 5 to 10 minutes per orbit. The scrubbing rate needs to be calculated for these high SEU rates.

Only a few SEL and SEFI occurrences have been observed in flight. The memories have recovered full functionality after a power cycling and reinitialisation.

SHEs due to microdose effects disappeared by themselves after a period ranging from seconds to months. As long as the SHE rate (microdose and or SEGR) is low, they can be corrected by the SEU correction codes.

4.6.1 SEE mitigation schemes: 2002-2012

Although the radiation performance for the SDRAMs considered for this period (ranging from 64 Mbit SDRAMs to 2 Gbit DDR3 SDRAMs) has changed dramatically—with the majority of bit flips attributable to SEFI and block errors—the basic mitigations schemes for hardening SSRs remain the same. The core of these schemes is a multi-bit EDAC code with sufficient power to correct a worst-case SEFI/block error in which every bit on a single memory die is corrupted. Memory is organized with bits/symbols in a logical data word interleaved across multiple die so that no single error can overwhelm the corrective power of the EDAC. The scrub rate is set so that multiple errors do not accumulate.The fact that no data were lost for any of the SSRs in the on-orbit studies for this period[67,71] illustrates that these scheme remain adequate at least up through the 512 Mbit SDRAM.

Future SSRs using DDR2/3 devices face additional challenges. If the SSR is to be operated with memory chips at full DDR speeds, the Delay-Lock-Loop would have to be enabled. This means that if the DLL upsets, the affected die must have its clock re-synched with the system clock—either by stopping the clock to the die and restarting it or by stopping and restarting the clock for the entire board. Other trends also pose challenges. Memories organized in a ×4 configuration are becoming more scarce from DRAM manufacturers, being much less common than ×8 and ×16 organizations. This requires the use of more complicated EDAC schemes if corrective power is not to be lost or memory organization made more complicated. In order to save space on memory boards, parts are being stacked with as many as 8 die in a package. These multi-chip packages do not have independent supply voltages, so if power must be cycled in the event of a SEFI, all the data on the entire stack will be lost. Additional mitigation may be required to accommodate this added complication.

5 Recommendations

5.1 Ground testing

An accurate heavy ion and proton SEE characterization is essential to assess the in flight SEE risk. The best accuracy is obtained when testing is done on parts coming from the flight lot. The sample size is also an important factor. Generally, because of the cost of particle accelerators, the SEE tests are performed on 2 to 3 parts. This gives poor test fidelity. Assuming that SEE sensitivity on memory device follows a binomial law, it is necessary to test 23 parts to get a sensitivity which will not be exceeded with a probability of 90% and a confidence level of 90%. It is important to test the parts not only for SEU, but for all the other potential sensitivities: SMU, SHE, SEFI, and SEL. Generally the statistics, and therefore the accuracy of these tests is poor.

An accurate TID characterization is also important, when the sensitivity is evaluated, the mission dose levels on memories should be kept to a level where no significant degradation is observed. It is essentially important for SSRs applications where a small increase of power supply current on a large number of devices may lead to a significant increase of the SSR supply current.

5.1.1 Ground testing: 2002-2012

Heavy-ion and proton SEE characterization remain essential to bounding risk of data loss due to SEE, and as before, characterizing all SEE error modes is crucial to predicting on-orbit performance of memories. However, ground testing of SDRAMs has become a more complicated endeavor since 2002. The high cross section for block errors and SEFI means that nearly all data will have multiple error modes. What this means is that multiple runs for each test condition may be needed to accumulate enough statistics for accurate rate estimation. As mentioned above, accumulating sufficient statistics at all LETs may be especially difficult for very disruptive errors—e.g. SEFI requiring a power cycle—especially if they are much rarer than other SEFI modes. The concerns about part-to-part and lot-to-lot variation in SEE susceptibility—especially for SEL and SHE--have not diminished in the last decade. Unfortunately, DRAMs are still commercial parts with limited lot traceability, and budgetary concerns still preclude testing a sufficiently large sample size to measure these variabilities. In the absence of such information, it is essential to estimate error rates conservatively. On the other hand, the relatively good agreement between estimated and on-orbit rates seen in references 67 and 71 argues that usually rates can be estimated accurately as long as the cross section vs. LET curve is based on sufficient statistics.

5.2 SEE error rate calculation

With an accurate heavy-ion and proton characterization, use of the adequate environment models, reasonable assumptions on the sensitive volume thickness, the flight SEU rates will be estimated within an order of magnitude for the background radiation environment.

As shown by the flight data, an orbit average rate does not correspond to the reality where the majority of SEUs occur in bursts (very high rate during a short period of time). These maximum rates need to be calculated.

The SPE environment models will give conservative estimates of the SEU rates during solar events.

For the other events such as SEL, SEFI, SEGR, etc., the accuracy of the prediction will be very poor. SEL and SEFI rate calculation assuming only one sensitive volume of area the device SEL cross section and a thickness of 2 um will give a conservative estimate of the flight rates. For SMU rates calculations these assumptions will lead to unrealistically high estimations of the SMU rates and considering every memory cell as a sensitive volume will underestimate the SMU rate. For these events we recommend to apply a higher design margin than for SEU.

5.2.1 SEE error rate calculation: 2002-2012

Rate estimation for SEE in DRAMs is at an interesting juncture. The 512 Mbit single-data-rate SDRAM generation was the last one where the standard assumptions of the rectangular parallelepiped assumed by, e.g., CREME96 applied for SEU as well as errors in control logic. This indicates that while the device geometries and feature sizes for control logic have more-or-less RPP sensitive volumes, the sensitive volumes of the individual memory cells do not. Because control logic feature sizes usually lag behind those of memory cells by roughly a couple of generations, we will also start seeing deviations from RPP for SEFIs block errors, etc. Reference 67 illustrates that up to the 512 Mbit generation, the key to accurate rate estimation was adequate error counts for each SEE mode. However, as pointed out previously, this is usually only feasible for SEU. For future generations, it is likely that SEU rates will either be estimated using Monte Carlo techniques (e.g. CRÈME-MC,[72] which is also new since 2002) or the rates will be very conservative.

The difficulties cited in Section 5.2 with regard to estimating rates for other SEE modes—especially destructive effects such as SEL and SEGR and disruptive events such as SEFI still apply. Moreover, the fact that SEFI and block errors now account for the vast majority of data corrupted has increased the importance of these errors—the errors that drive the data loss and/or mitigation must be estimated with limited statistics, leading to large uncertainties.

5.3 SEE mitigation scheme

5.3.1 SEU and MBU

EDAC techniques work well to mitigate SEU. Hamming codes will fail in cases of SMU. The obvious and well-known solution to deal with SMU on single bit correction codes is to simply rearrange the memory so that it is constructed from devices with a “x1 bit” architecture. With such an architecture multiple bit flips within a device will be spread across several data words, thus causing no difficulty with the Hamming code EDAC system. Unfortunately recent memories are not available with x1 bit architecture, therefore using only one bit per memory device to form a data word will require a large memory overhead or a complex design. Another solution is the use of a modified Hamming code capable of correcting 2 bits in a data word.

For LEO orbits the data shows that the SEU occur in bursts when the spacecraft goes through the trapped proton belts. For example, on a LEO polar orbit, 80% of the SEU occur in the SAA in bursts lasting for 5 to 10 minutes per orbit. The scrubbing rate needs to be calculated for this high SEU rate. On the other hand, in the absence of SPE, the number of SEUs that occur outside the SAA are so small that they can be ignored. If the scrubbing rate is longer than the time taken to pass through the trapped proton belt, it would be just as effective to make the scrubbing rate equal to the orbital period. If the scrubbing rate is substantially shorter than the time taken to pass through the trapped proton belt, the scrubbing may be suspended for the rest of the orbit where the spacecraft is outside the trapped proton belt. However, in case of large SPE the SEU rate may also be very high outside the SAA.

5.3.1.1 SEU and MBU mitigation: 2002-2012

Since the consequences of SEU and MBU (also referred to above as single-event multibit upset or SMU), the same mitigations apply for current SSRs as applied prior to 2002. A sufficiently powerful EDAC combined with a memory architecture (e.g. interleaving bits or symbols in a data word so that the EDAC is not overwhelmed by any single error and using scrubbing so that errors do not accumulate over time remains a robust architecture against

SEU and MBU. Moreover, the rate for scrubbing must be set in consideration of the worst-case SEU/MBU rate, likely to occur during passage of the spacecraft through the proton belts or during solar particle events. This is true, even though most of the errors in the memory will occur as a result of SEFI. Multiple SEFI will be rare, while SEU and possibly MBU will be daily occurrences. It is notable that recent tests of DDR2 and DDR3 devices have shown that MBUs (multiple bits upset in the same logical data word) are rare, even under irradiation at 70 degrees to the normal.[73]

5.3.2 Other single events

Use of devices not sensitive to SEL, SEFI, SEGR and SHE is recommended. In SSR applications, because of the large number of devices used, there is always the risk of such an event. It is recommended to use a flexible design, with current limitations, and the possibility to power cycle and reinitialize. The use of spare memory is also useful in case of permanent failure of some parts of the memory array due to SEGR or destructive SEL.

5.3.2.1 Mitigation for other SEE: 2002-2012

Although the advice given in section 5.3.2 still holds, it has become increasingly difficult to find an SDRAM or DDR device that is immune to SEFI and SHE. This has meant that most SSRs have had to be hardened against block errors and SEFI by using EDAC with multibit or even multisymbol correction and interleaving bits/symbols across multiple die. The power of the EDAC should be such that even if the memory is susceptible to SHE (stuck bits), the SSR requirements can be met at end of life. Scrub rates again need to be determined using worst-case SEE rates (proton-belt or solar particle event).

One additional challenge for mitigating SEFI arises from the tendency of DRAM organization to become wider as density increases and of data words to also widen (e.g. from 32 to 64 bits) as computing power improves. The width of the die is a natural choice for the width of a symbol. This has increased the need for more powerful EDAC codes.

The tendency of many SDRAMs, regardless of generation, to be susceptible to SEFI modes requiring power cycling for recovery makes this ability every bit as valuable as it was during the first decade of SSRs. As noted above, such errors are usually rare, but much more probable modes can mask the susceptibility, so it is prudent to retain this flexibility even if susceptibility to these modes is not demonstrated during testing.

On the positive side, SEL susceptibility has decreased since 2008, and SEGR susceptibility has yet to be seen for DRAMs.

5.4 Additional Guidelines and Trends: 2002-2012

In addition to the observations and guidelines given above, it is useful to examine trends that have emerged since 2002—either because they had not yet developed or because they could not be clearly seen given the limited history of SSRs at that time.

One trend that has continued has been the consolidation of SDRAM/DDR manufacturers. The bankruptcy of Elpida in 2012 meant that one of the more consistent performers in the industry would no longer be an option for new systems. Likewise, the short lifecycle of these parts—barely 18 months between generations places temporal pressures on potential users in the space community to identify, test an procure parts in short order.

Scaling of SDRAMs has also continued during this period—albeit at a somewhat slower pace than during the 1990s. Minimum feature sizes in 2002 were roughly 130 nm, while in 2012, state of the art DDR2/3 SDRAMs had minimum feature sizes of 40-50 nm. The minimum feature size is generally used only in the DRAM cells, which has led to SEU cross section vs. effective LET curves departing from the conventional Weibull form for ions incident off normal to the die, while upsets of control logic (e.g. SEFI) still follow the conventional form. This complicates error estimation for SEU.

The most significant radiation trend in DRAM technologies for applications in bulk memory and SSRs has been the rising susceptibility to SEFI and large block errors. This has meant that most of the data errors that occur in a memory chip involve multiple bits and occur in cluster, resulting in increasing use of error correction codes with multi-bit and/or multi-symbol correction capability. While this trend is evident for the 512 Mbit SDRAM generation, it is likely to continue and perhaps accelerate when DDR2 and DDR3 memories come into use in space.

The increasing width and density of memories also places pressure on current. Increasing width means that error correction must increase in power so that a worst-case error, corrupting bits across the die width can be corrected. Larger memory chips mean more data words will require correction as a result of a SEFI. Limited space on electronics boards has created demand for stacked memory die/chips. Die in these stacked parts typically share a common power supply, so if power must be cycled to recover from a SEFI or nondestructive SEL, all data on the

stack will be lost. This increases the importance of either finding a memory not susceptible to SEFIs requiring a power cycle for recovery or of increasing the interleaving between bits in a single word.

During the past decade, mitigation of data loss has also not stood still. Error correction codes have continued to improve in efficiency, and additional options continue to appear. Depending on the memory organization, data word width and desired hardness, low-density parity codes, turbo codes or other Bose-Chaudhuri-Hocquenghem (BCH) could rival Reed-Solomon codes as the best option. Moreover, FLASH memories have improved in terms of radiation hardness, endurance and retention to the point where they could compete with SDRAM in applications that can tolerate the slower speed of FLASH memory. The nonvolatile nature of FLASH allows data to be stored in unpowered chips until it is needed, reducing vulnerability to SEFI and SEU, reducing data loss when power is cycled to restore functionality in the event of a SEFI and simplifying memory organization.

6 Conclusions

COTS memories have been flown with success now for more than twenty years. Memory experiments have been very useful to check the behavior of these parts in space. It is very important because the MBU sensitivity is difficult to test accurately at ground.

State-of-the-art memories, like SDRAMs and FLASH continue to become more complex, and therefore more difficult to test and more sensitive to radiation effects. New flight experiments on these devices are essential to "secure" the use of these devices in future applications. Indeed, as the experience with LRO shows, even analysis of flight data on error occurrence and correction can provide useful validation of ground-based testing and increase confidence in the use of these memories for space flight applications. The flight data has shown that is important to have accurate information about the shielding, and the solar particle flux to study the effects of SPE. As no information is available for solar heavy ions, it is useful to fly a detector with the experiments.

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