NASA Electronic Parts and Packaging Program

Part I: Surge Step Stress Testing of Tantalum Capacitors

NEPP FY12 Report
NEPP Task 390-007

Parts Packaging and Assembly Technologies Branch Code 562
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The research described in this report was carried out at Goddard Space Flight Center, under a contract with National Aeronautics and Space Administration.

Abstract

Surge step stress testing (SSST) is a useful and important practice that has been applied to determine the voltage de-rating for tantalum capacitors. This report summarizes the verification results for SSST of three different tantalum capacitors.

Three different types of tantalum (Ta) capacitors (MnO_2, 220 μF, 6.3V solid tantalum; reactive-polymerized 220 μF, 6.3V; and pre-polymerized 22 μF, 25V) were tested under three different transient surge conditions: under damp, critical damp, and over damp. The results are summarized briefly as follows:

For MnO_2, 220 μF, 6.3V solid tantalum capacitors, all failures are either catastrophically burned or severely damaged (chip out). Damp conditions did not have a noticeable effect on the breakdown voltages of the capacitors. Weibull analysis of the breakdown voltage at a 100 ppm failure rate suggests a voltage de-rating of 46-50%, consistent with previous reports.

For reactive-polymerized 220 μF, 6.3V Ta capacitors, no impact of surge transient change on the breakdown voltage was observed. All units failed with minor chip out or smoke. There were no catastrophic failures. The breakdown voltage, estimated at a 100 ppm failure rate, indicates that no voltage de-rating is necessary for these 6.3V polymer Ta capacitors, a finding that is in agreement with a previously published paper for low-voltage polymer Ta capacitors.

For pre-polymerized 22 μF, 25V Ta capacitors, the results are very interesting. The failure patterns are highly dependent on the transient conditions; all units were catastrophically burned when they underwent SSST in the underdamp condition. All units showed benign failure patterns when tested under overdamp conditions. The failure patterns were mixed in between when tested under critical damp conditions.

It seems evident that SSST breakdown voltage is dependent on the percentage of SSST voltage transient overshoot. When the percentage of voltage overshoot is less than 10% of the surge voltage, the current practical voltage de-rating of tantalum capacitors is adequate. It is important to watch for the possible surge voltage overshoot when tantalum capacitors are used for circuit tuning.

It recommended, based on this study, that SSST shall be used for quality conformance inspection (QCI) of tantalum capacitors when they are used for critical NASA flight projects, in order to verify the actual percentage of voltage de-rating.

Acknowledgement

The author appreciates the NASA Electronic Parts and Packaging (NEPP) program's support for this study. The author is also thankful to the Code 562 Parts Analysis Laboratory for support in performance of electrical testing.

1. Introduction

A surge step stress test was used to identify the critical stress level of a capacitor batch in order to predict the power-on failure mechanism and to quantify the probability of capacitor failure at the first circuit turn on after reflow soldering.

The SSST consists of rapidly charging the capacitor with incremental voltage increases, through a low resistance in series, until the capacitor under test is electrically shorted. Because it is a destructive testing method, SSST can only be used for qualifying capacitor products. It cannot be used for screening processes.

From a reliability standpoint, SSST can be considered as a means of testing the short-term survivability under a time varying stress. This test is of equal importance with long-term reliability testing, such as the commonly used highly accelerated life testing (HALT). However, the two tests reveal quite different failure mechanisms for capacitors. In general, HALT is used to reveal the dielectric wearout failure mechanism, and SSST is used to reveal the overstress failure mechanism.

To date, SSST has been widely used and thoroughly practiced by tantalum manufacturers. It has been reported that SSST has been successfully used to determine the de-rating of tantalum capacitors and aluminum polymer capacitors. The results are consistent with most of the application cases for tantalum capacitors, indicating that SSST is a credible testing approach [1].

A two-year study at GSFC has incorporated a typical SSST profile, as a time-varying stress, into the Weibull model to reveal the failure mechanism in different types of capacitors [7]. The time-to-failure data, rather than the breakdown voltage, has been characterized in a 2-parameter Weibull model, and the failure modes of various capacitors can be characterized. The results indicate that failure modes appear to be associated with dielectric materials and appear to be independent of other factors, such as capacitor values, capacitor constructions, and manufacturer processing.

The breakdown voltage at a 100 ppm failure level, when calculated from the Weibull results, suggests a voltage de-rating of more than 50% for MnO_2-based tantalum capacitors. These results caused some amount of controversy when presented at the Capacitors and Resistors Technology Symposium (CARTS) 2011 Conference [7]. The controversial issues are discussed in detail below. But the controversy also indicates the need to re-test the tantalum capacitors with better-defined SSST conditions.

Controversy 1: SSST and Damping Parameters:

A typical inductor-resistor-capacitor (LRC) circuit for testing a capacitor's capability to withstand a surge current stress is shown in Figure 1. The input to each capacitor is isolated and buffered with a capacitor bank C_{bank} to ensure high charge currents.

When a test circuit such as that shown in Figure 1 is used, the transient current and voltage can be divided into three cases based on the value of a characteristic damping parameter ξ, where

$$\xi = \frac{R}{2}\sqrt{\frac{C}{L}}. \quad (1)$$

Based on the values of ξ, the transient conditions can be sorted into three patterns, i.e., underdamped (ξ <1), critically damped (ξ =1) and overdamped (ξ >1), where R, C, and L are the

sum of all equivalent parameters in the circuit shown in Figure 1. When tested under different transient patterns, the surge breakdown voltages for tantalum capacitors can significantly differ.

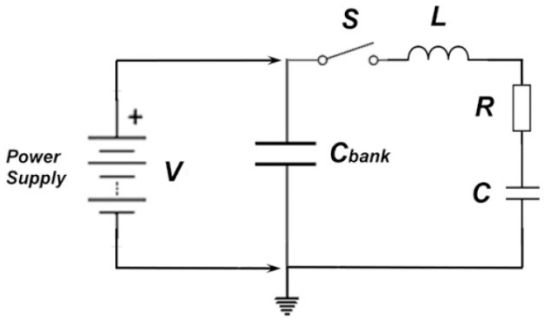


Figure 1. A typical SSST testing circuit.

Specifically, if a waveform that causes a failure is underdamped and has overshoot that is 10% higher than the target voltage (the initial charge voltage of the capacitor bank before the surge), the surge breakdown voltage should be reported as the actual peak voltage (target voltage + 10%), not the target voltage.

As shown in Eq. (1), due to a usually high capacitance, an overdamped test condition is readily attainable for tantalum capacitors if one can keep the very low circuit inductance ***L*** in the circuit. For ceramic capacitors, the relatively small capacitance often results in an underdamped SSST condition.

In general, tantalum capacitors should not be surge tested under any underdamped conditions. The underdamped condition provides a harsh ringing transient waveform that may allow tantalum capacitors to overshoot or to undershoot, resulting in a reverse bias application. Tantalum capacitors are not designed to be used under any underdamped, overshoot, or reverse bias conditions.

On the other hand, however, some tantalum capacitors failed at a voltage that was significantly below the rated voltage. In many cases, the failure cannot be explained, but a suspected cause is the exposure to unexpected underdamped conditions. This indicates that the failure mechanism may be understandable if the tantalum capacitors were surge tested in underdamped conditions.

A possible compromise is to subject tantalum capacitors to SSST with a maximum ±10% variation of damping parameter ξ. An oscilloscope could be used to closely monitor the transient overshooting to make sure that no more than 10% voltage overshoot (underdamped) or voltage undershoot (the peak negative-going excursion of an underdamped transient waveform) will be applied to any tantalum capacitor under the proposed SSST.

In addition, during SSST, the target voltage is incrementally increased until device failure. The actual reverse voltage seen during voltage undershoot becomes increasingly large as the target voltage is incrementally increased. So while some manufacturers may claim that tantalum capacitors can withstand up to 10% reverse bias exposure for short periods, the actual exposure during underdamped SSST can easily exceed this guideline as the SSST voltage is incrementally increased well above the rated voltage. It is hard to tell whether it was the peak positive voltage alone that killed the capacitor or whether it was the repetitive exposure to significant reverse bias that reduced the capacitor's tolerance to high peak positive voltages.

Controversy 2: SSST Protocol:

A typical SSST profile is shown in Figure 2. When testing begins, the capacitor is charged to a set voltage, held at that voltage for ½ second, and then discharged through a low resistance for ½ second. This sequence is repeated four times. After the fourth pulse, the voltage setting is increased slightly for the next set of pulses. This four-pulse cycle is repeated at incrementally higher voltages until the capacitor breaks down.

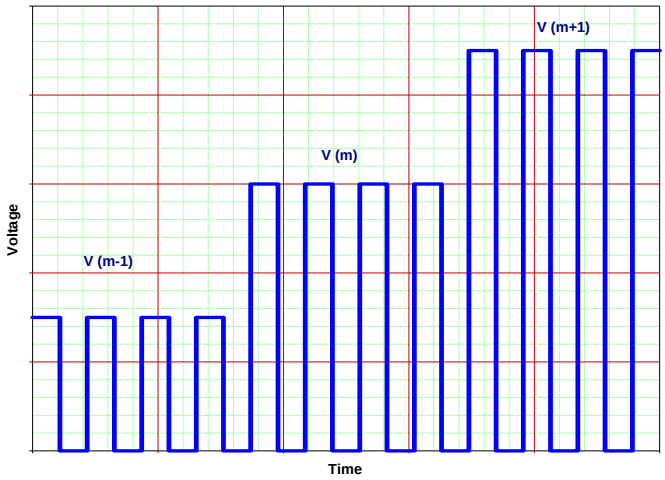


Figure 2. Illustration of a surge step voltage profile with an incremental voltage pulse.

Although SSST is not a military test and is not associated with qualification of any military-grade capacitors under Defense Logistics Agency-Land and Maritime (DLA-LAM) requirements, it is relevant to military-specified surge current testing as defined in MIL-PRF-55365, paragraph 4.7.18. The relevance between SSST and military-specified surge current testing is shown by the following: (1) each pulse cycle shown in Figure 2 is a surge current test, and the testing continues at higher voltages until the capacitor breaks down; and (2) SSST and military-specified surge current testing share similar testing circuits, like the one shown in Figure 2.

MIL-PRF-55365H (released on February 4, 2011) significantly modified the surge current test conditions. This makes it appropriate for MIL-PRF-55365 part users to modify the SSST protocol accordingly, particularly for the following specs:

1. An individual test circuit is required for each capacitor under test. Since capacitors always undergo SSST one at a time at GSFC, this is not a problem.
2. The capacitor bank should be at least 20 times the value of the capacitor under test, instead of 50,000 µF minimum. In practice, the value of the capacitor bank as shown in Figure 1 was found to have an impact on the damping conditions. The lower the C_{bank} value, the more easily an underdamped condition may be achieved. A higher C_{bank} value, such as 50 times that of the capacitor under test, is preferred from the capacitor manufacturer. In this proposed test, a capacitor bank of 20-50 times the value of the capacitor under test will be applied for the proposed SSST. This capacitor bank variation will be practiced as an alternative for altering the damping conditions.
3. The charge/discharge cycle is reduced to 1 second from 4 seconds. The SSST profile specified in Figure 2 will continue to be used.
4. The total DC resistance as shown in Figure 1 (excluding the capacitor) should be a maximum of 1.0 Ω. This change was made only to improve the test by ensuring that each

tested capacitor would be exposed to a quantifiable minimum peak current during the test. However, a range of DC resistance between 0 and 1.0 Ω will be practiced to modify the damping conditions within a maximum 10% overshoot.

The objectives of the proposed NEPP work for SSST of various tantalum capacitors are summarized below:

1. Full use of the SSST method to characterize the capacitor failure mechanism under a time varying stress (time-to-failure) and to differentiate the performance of different capacitor technologies;
2. Re-test various tantalum capacitors under different transient conditions (including slightly underdamped) to verify earlier SSST results for tantalum capacitors at GSFC;
3. Incorporate some modifications from the recent modification of MIL-PRF-55365 for surge current testing, and make necessary changes for future SSST of capacitors.

2. SSST Experimental Setup and Test Procedure

A total of 900 tantalum capacitor samples from two different manufacturers, with three different part types (group 495: solid MnO_2, 6.3V, group 520: reactive-polymerized, 6.3V, and group 521: pre-polymerized high voltage, 25V), will be electrically tested to breakdown, one by one, using an SSST protocol.

The test circuit setup is shown in Figure 3, where a power supply (AMETEK XFR300-9GMA) will charge a capacitor bank and the capacitor bank will discharge and electrically break the capacitor under test. A few minutes will be required to destroy one capacitor at a time. A non-destructive, low-voltage pre-test at 5V will be performed prior to the actual test in order to verify the test circuit setup and the transient conditions.

All Ta capacitors are in a D case package with an EIA 7343 footprint. The actual part size is about 7.3 mm × 4.3 mm × 3.1 mm, typically. All capacitors have been solder-attached to custom Printed Circuit Boards (PCB) testing circuit board, each of which contains 20 capacitor units.

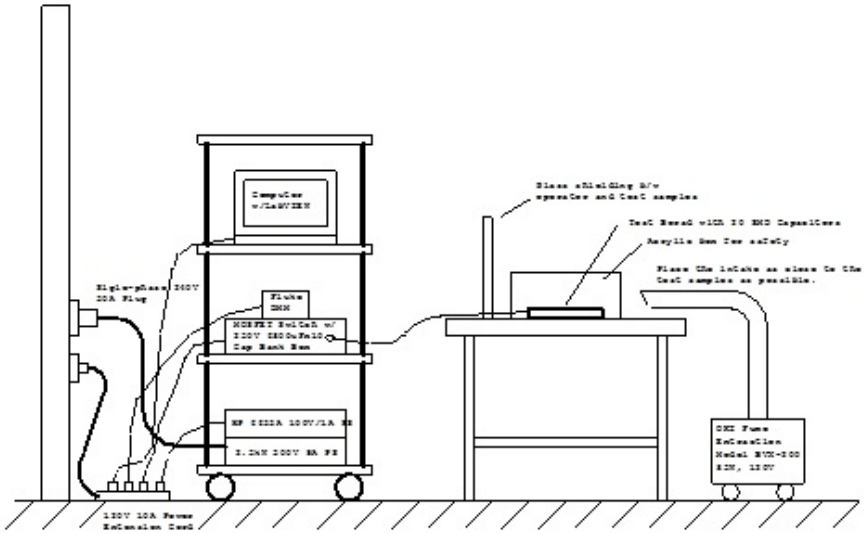


Figure 3. Illustration of the SSST setup to be used for this study.

As illustrated in Figure 3, the PCB with 20 capacitors will be placed on top of a piece of high-temperature rubber material. A suitably large Pyrex glass container with a minimum thickness of ¼" will be used to completely cover the entire PCB during testing. If any flying chips are generated during testing, they will be blocked and confined inside the Pyrex container.

A fume extraction unit will be operating during the testing to collect possible fumes generated from catastrophic breakdown. Any broken chips will be collected and disposed of in a hazardous waste container after complete testing of a circuit board.

As shown in Figure 1, the input to each capacitor is isolated and buffered with a capacitor bank C_{bank} to ensure high charge currents. The actual capacitance of C_{bank} must be at least 20 times that of the tantalum capacitors under test for surge testing, according to MIL-PRF-55365. The current limit resistor R, which consists of line resistance, the equivalent series resistance (ESR) of the test capacitors is typically set between 0.001 and 0.5 Ohms.

As has been noted, when the LRC circuit shown in Figure 1 is used for surge testing capacitors, a different test setup may give different test results due to differing characteristic inductances that may change the surge current waveform [1]. The inductance L in Figure 1 is composed of the inductance of the switch device, the lead wires of the test circuit setup, and the equivalent series inductance (ESL) in the test capacitors.

The bank capacitor is charged to a preset test voltage level V before the switch is closed. After the switch is closed, the charges stored in capacitor bank C_{bank} are dumped into test capacitor C. Assuming that the capacitance of the test capacitor is not changed during the charging cycle, then the charge in the test capacitor as a function of time, $\Delta C(t)$, can be easily derived from Kirchhoff's voltage law:

$$\frac{d^2\Delta C(t)}{dt^2} + \frac{R}{L}\cdot\frac{d\Delta C(t)}{dt} + LC\cdot\Delta C(t) = \frac{V}{L} \tag{2}$$

This is a typical 2nd-order non-homogeneous differential equation, and its solution can be found easily in a circuit analysis textbook [3].

The general solutions of Eq. (2) can be divided into three cases, based on the value of a characteristic parameter ξ. All three possible solutions for Eq. (2) have been summarized in Table I, where the critical resistance $R_{cr} = 2\sqrt{L/C}$, the dumping ratio $\xi = R/R_{cr}$, and the characteristic frequency $\omega_n = 1/\sqrt{LC}$.

Based on previous studies [4, 5], the underdamped circuit condition ($\xi < 1$) represents the most severe test among all three cases, so all of the capacitors should be surge tested with ($\xi < 1$). In this underdamped case, assuming that the capacitance in transient voltage is independent, the transient voltage built up in the capacitor can then be expressed as $V(t) = \frac{\Delta C(t)}{C}$, and the current that flows into the capacitor is $I(t) = \frac{d\Delta C(t)}{dt}$, the transient voltage and current generated by the capacitor during surge test can be further expressed as:

$$\begin{cases} V(t) = \dfrac{\Delta C(t)}{C} = V[1 - \dfrac{e^{-\frac{t}{\tau}}}{\sqrt{1-\frac{LC}{\tau^2}}} \sin\left(\sqrt{\dfrac{1}{LC} - \dfrac{1}{\tau^2}} \cdot t + \theta\right)] \\ I(t) = \dfrac{d\Delta C(t)}{dt} = \dfrac{V}{L} \cdot \dfrac{e^{-\frac{t}{\tau}}}{\sqrt{1-\frac{LC}{\tau^2}}} \sin\left(\sqrt{\dfrac{1}{LC} - \dfrac{1}{\tau^2}} \cdot t\right) \end{cases} \quad (3)$$

where $\tau = 2L/R$ and $\theta = tan^{-1}\frac{\sqrt{1-\xi^2}}{\xi}$ are related to circuit elements *L*, *R*, and *C* only.

According to Table I, in order to surge test the capacitors in an underdamped condition, the values of *L*, *R*, and *C* must be estimated carefully. Since each test circuit may have different values for the circuit elements, different test setups may give different results. Methods to calculate circuit elements, particularly the circuit inductance *L*, to ensure that the testing is underdamped, have been widely reported previously [5, 6].

Table I. General Solutions for Differential Equation (10) Based on Three Case Circuit Parameters.

Testing Conditions	$\xi = 0.5R/\sqrt{L/C}$	Solutions of Eq. (2) $\Delta C(t) =$
Overdamped	$\xi > 1$	$CV + e^{-\xi\omega_n t}[K_1 cosh(\omega_n\sqrt{\xi^2-1}\cdot t) + K_2 sinh(\omega_n\sqrt{\xi^2-1}\cdot t)]$
Critically damped	$\xi = 1$	$CV + (K_1 + K_2 t)e^{-\omega_n t}$
Underdamped	$\xi < 1$	$CV + e^{-\xi w_n t}[K_1 cos(\omega_n\sqrt{\xi^2-1}\cdot t) + K_2 sin(\omega_n\sqrt{\xi^2-1}\cdot t)]$

In the actual surge testing of capacitors, the determination of an underdamped condition can be performed relatively easily. As shown in Table I, only $V(t)$ and $I(t)$ exhibit a unique ringing waveform in underdamped testing conditions. Therefore, an oscilloscope (Agilent MSO9254A, a mixed signal oscilloscope) is used to constantly monitor the transient voltage and current during the surge testing. Figure 4 shows an example of how to determine the SSST breakdown voltage as a function of SSST cycles.

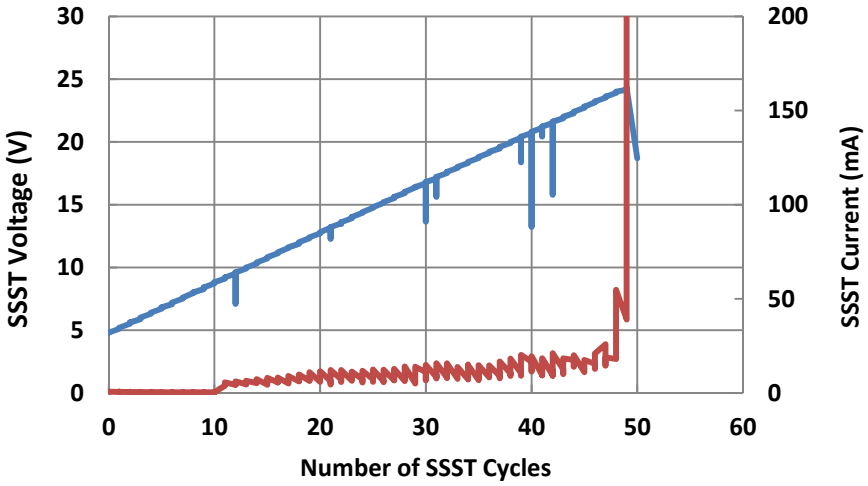


Figure 4. Surge voltage and current as a function of SSST cycles for MnO_2-based solid tantalum capacitors (6.3V) under underdamped conditions.

3. SSST Results and Discussion

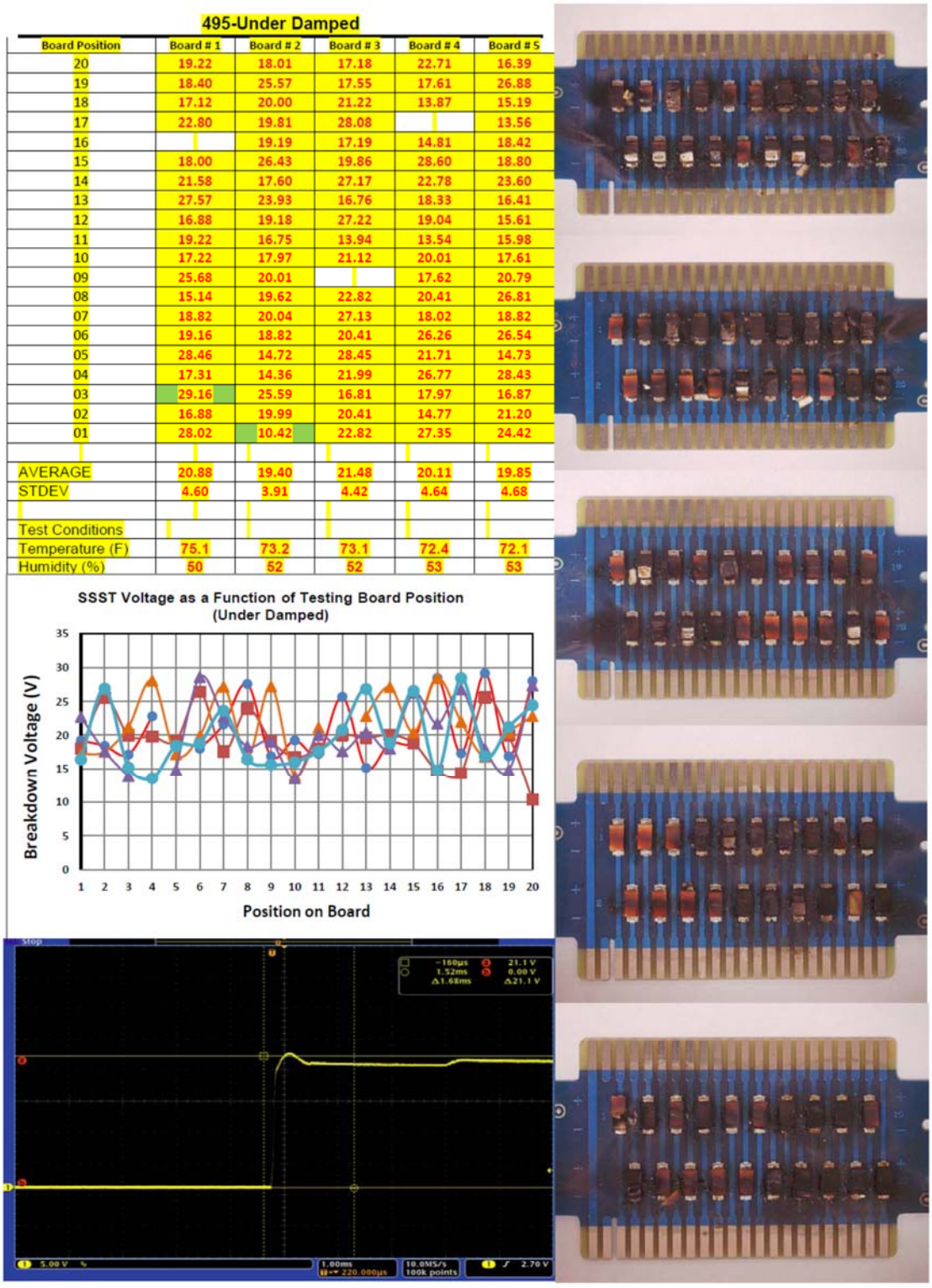
SSST breakdown voltage data for the three damping conditions for all three types of tantalum capacitors are shown in Figures 5-7. A total of 900 capacitor samples was tested, with 300 each for every part number product. Of the 300 samples for each part number, 100 were tested under each of the three damping conditions. The damping conditions are defined in Table I and are set according to Eq. (1).

The data in Figures 5-7 were labeled for each circuit board and at a specific position on the board so that each unit can be traced per its SSST breakdown voltage. Since the performance of tantalum is sensitive to the history of chip assembly, the SSST voltage as a function of board location was also presented. Although some scattering readings can be identified, most tantalum capacitors did not show any SSST voltage changes with respect to their position on the boards, which indicates that all manufacturers' assembled boards were processed uniformly well. Occasionally, some capacitor samples were read short or open even before the SSST began. These units were left open in Figures 5-7.

The photos of each circuit board after SSST were also included in each figure. They are arranged by board numbers, with #1 at the top and #5 at the bottom. The ambient temperature and relative humidity were also recorded for each board during SSST. The transient voltage for each damping condition was also recorded and presented; the voltage overshoot was strictly limited to a level less than 10% of the applied voltage value.

The failure mode depends on the capacitor type and on the damping conditions. For MnO_2-based solid tantalums, all failures were catastrophic, generating flames and smoke that resulted in severe burning of the capacitor body after SSST. On the other hand, most low-voltage reactive-polymerized capacitors showed a benign failure mode without any noticeable damages. Some of the tantalum capacitors in this group revealed smoking and partial discoloration, but no failure was catastrophic.

The group of 25V, pre-polymerized high-voltage tantalum capacitors reveals failure modes that are highly dependent on the damping condition: catastrophic when underdamp, benign when overdamp, and a mixture of both when critically damp. However, the average SSST breakdown voltage does not change much with each failure mode, indicating that the SSST breakdown voltage is irrelevant to the failure mode for this group of polymer capacitors.



495-Under Damped

Board Position	Board # 1	Board # 2	Board # 3	Board # 4	Board # 5
20	19.22	18.01	17.18	22.71	16.39
19	18.40	25.57	17.55	17.61	26.88
18	17.12	20.00	21.22	13.87	15.19
17	22.80	19.81	28.08		13.56
16		19.19	17.19	14.81	18.42
15	18.00	26.43	19.86	28.60	18.80
14	21.58	17.60	27.17	22.78	23.60
13	27.57	23.93	16.76	18.33	16.41
12	16.88	19.18	27.22	19.04	15.61
11	19.22	16.75	13.94	13.54	15.98
10	17.22	17.97	21.12	20.01	17.61
09	25.68	20.01		17.62	20.79
08	15.14	19.62	22.82	20.41	26.81
07	18.82	20.04	27.13	18.02	18.82
06	19.16	18.82	20.41	26.26	26.54
05	28.46	14.72	28.45	21.71	14.73
04	17.31	14.36	21.99	26.77	28.43
03	29.16	25.59	16.81	17.97	16.87
02	16.88	19.99	20.41	14.77	21.20
01	28.02	10.42	22.82	27.35	24.42
AVERAGE	20.88	19.40	21.48	20.11	19.85
STDEV	4.60	3.91	4.42	4.64	4.68
Test Conditions					
Temperature (F)	75.1	73.2	73.1	72.4	72.1
Humidity (%)	50	52	52	53	53

Figure 5a. SSST results for five PCBs for group 495 - MnO_2 220 µF, 6.3V solid tantalums: Underdamped conditions.

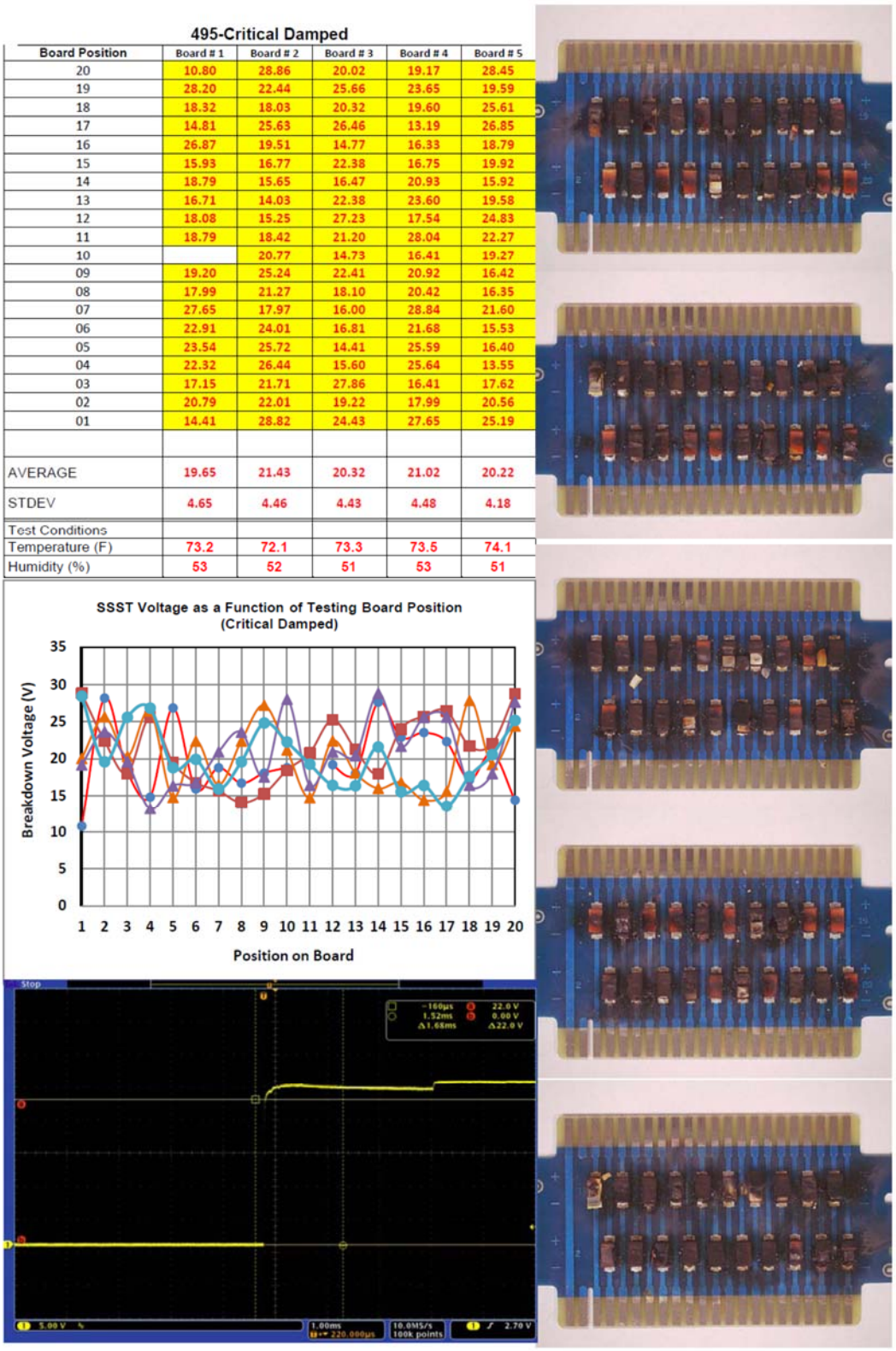
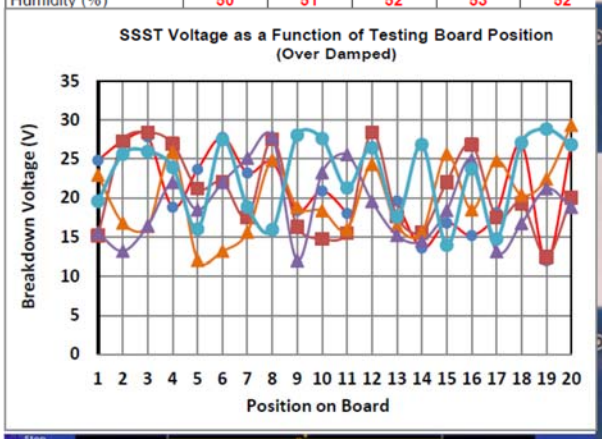
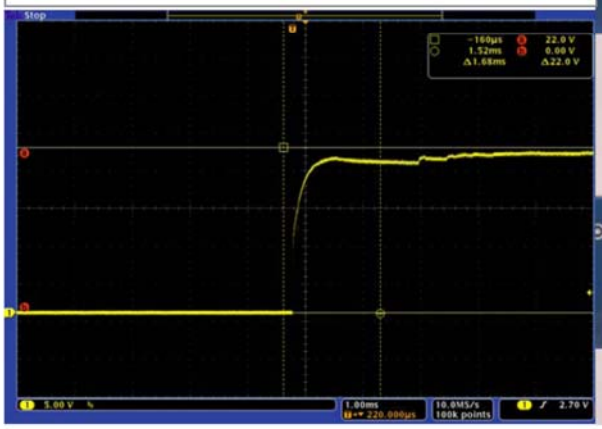


Figure 5b. SSST results for five PCBs for group 495 - MnO_2 220 µF, 6.3V solid tantalums: Critical damp conditions.

495-Over Damped

Board Position	Board # 1	Board # 2	Board # 3	Board # 4	Board # 5
20	24.83	15.19	22.94	15.52	19.57
19	27.26	27.29	16.78	13.18	25.61
18	27.84	28.44	16.36	16.44	25.97
17	18.82	26.96	25.90	22.00	23.93
16	23.67	21.20	12.06	18.47	16.01
15	27.78	22.05	13.18	22.01	27.48
14	23.21	17.52	15.60	25.11	18.86
13	24.58	27.54	24.88	27.88	15.94
12	18.37	16.31	18.83	12.01	28.06
11	20.90	14.74	18.38	23.25	27.62
10	18.01	15.52	15.97	25.56	21.29
09		28.41	24.31	19.56	26.44
08	19.61	17.62	16.41	15.20	17.6
07	13.58	15.55	15.56	14.45	26.86
06	16.78	22.04	25.63	18.39	13.93
05	15.18	26.85	18.49	24.86	23.73
04	18.11	17.50	24.79	13.13	14.74
03	26.88	19.31	20.40	16.74	27.1
02	12.03	12.47	22.42	21.19	28.84
01	26.86	20.00	29.31	18.81	26.84
AVERAGE	21.28	20.63	19.91	19.19	22.82
STDEV	5.04	5.28	4.82	4.65	5.06
Test Conditions					
Temperature (F)	73.1	72.5	72.5	73.2	72.5
Humidity (%)	50	51	52	53	52





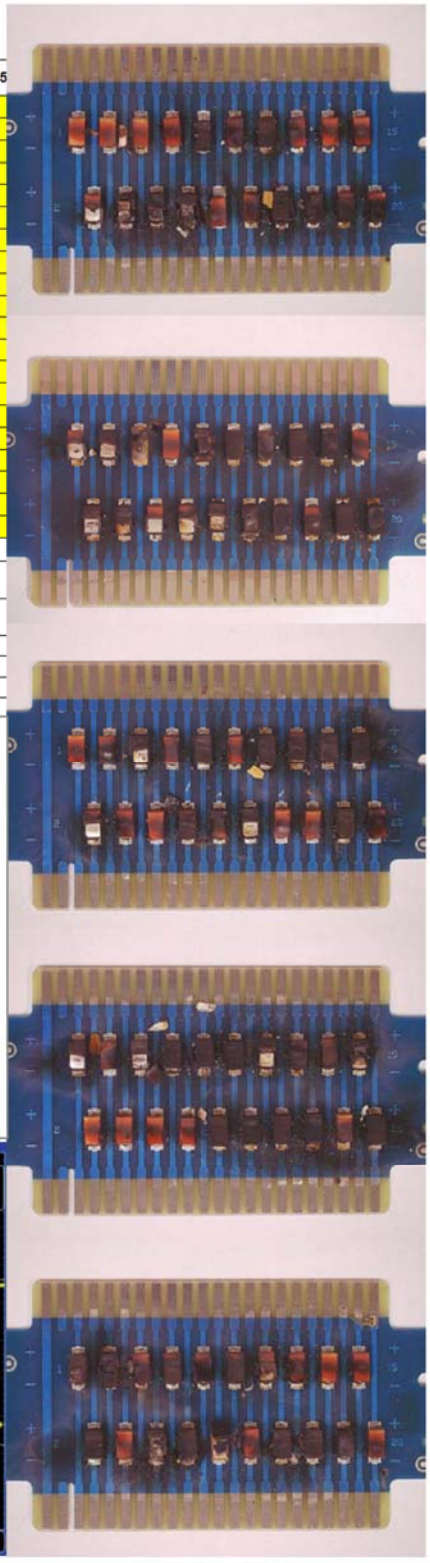
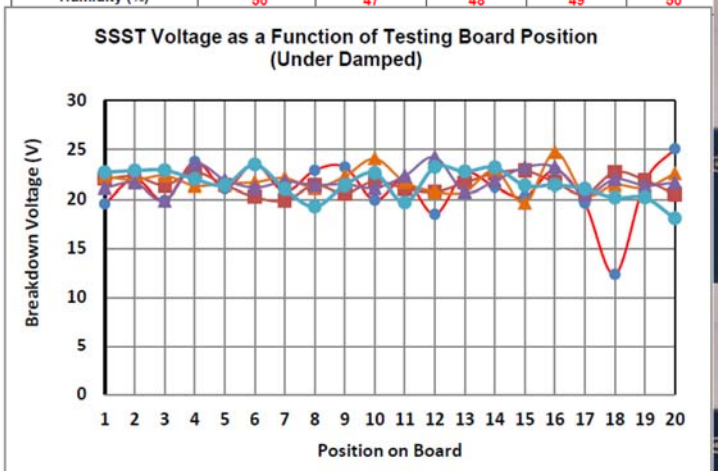
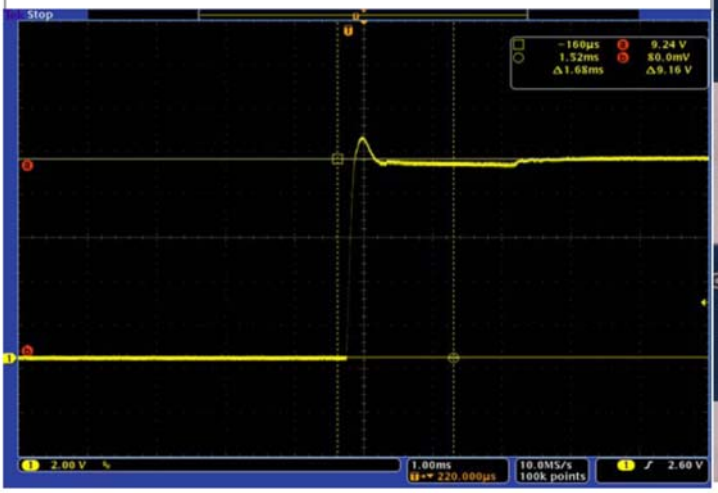


Figure 5c. SSST results for five PCBs for group 495 - MnO_2 220 µF, 6.3V solid tantalums: Overdamp conditions.

520-Under Damped

Board Position	Board # 1	Board # 2	Board # 3	Board # 4	Board # 5
20	19.54	22.02	22.28	21.11	22.70
19	22.02	22.30	21.93	21.63	22.88
18	19.89	21.40	22.36	19.83	22.90
17	23.79	22.71	21.34	23.53	22.02
16	21.08	21.43	21.55	21.93	21.41
15	23.51	20.24	21.69	21.14	23.49
14	20.75	19.87	22.11	21.74	21.03
13	22.89	21.39	21.12	21.41	19.25
12	23.22	20.59	22.28	21.49	21.40
11	19.91	21.80	24.08	21.11	22.62
10	22.00	21.07	21.70	22.32	19.67
09	18.47	20.74	20.75	24.22	23.23
08	22.57	21.65	20.75	20.74	22.78
07	21.22	22.60	22.89	21.84	23.20
06	20.22	22.87	19.61	23.20	21.37
05	22.91	21.69	24.74	23.22	21.42
04	19.61	20.50	20.45	20.46	21.03
03	12.35	22.72	21.41	21.99	20.15
02	21.69	21.91	21.11	21.37	20.17
01	25.08	20.49	22.57	21.64	18.06
AVERAGE	21.14	21.50	21.84	21.80	21.54
STDEV	2.67	0.89	1.19	1.07	1.50
Test Conditions					
Temperature (F)	73.1	72	71.9	72	71.8
Humidity (%)	50	47	48	49	50





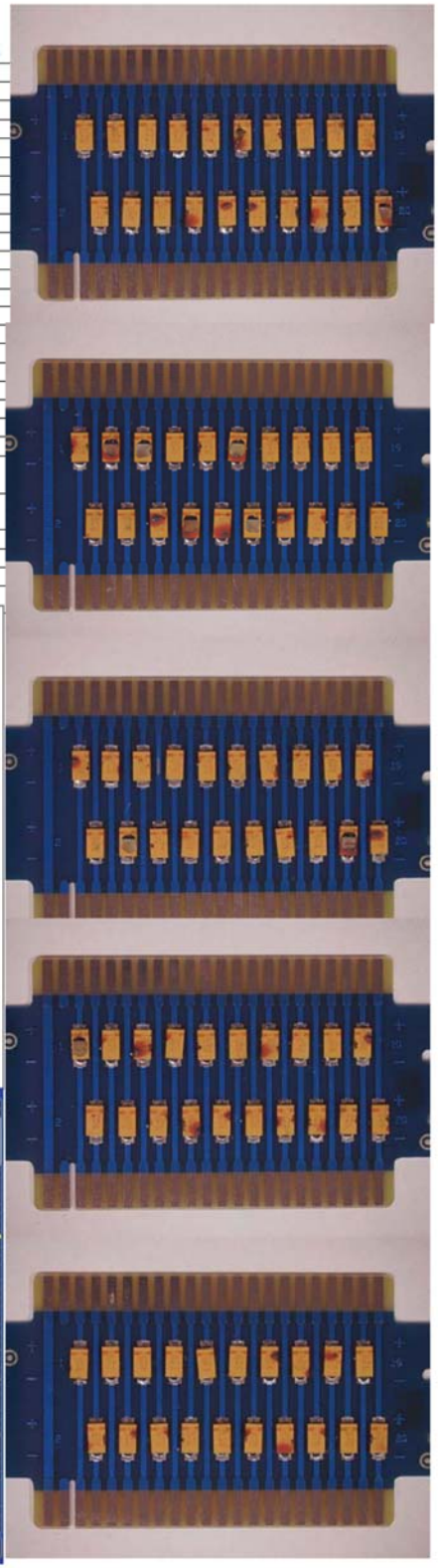
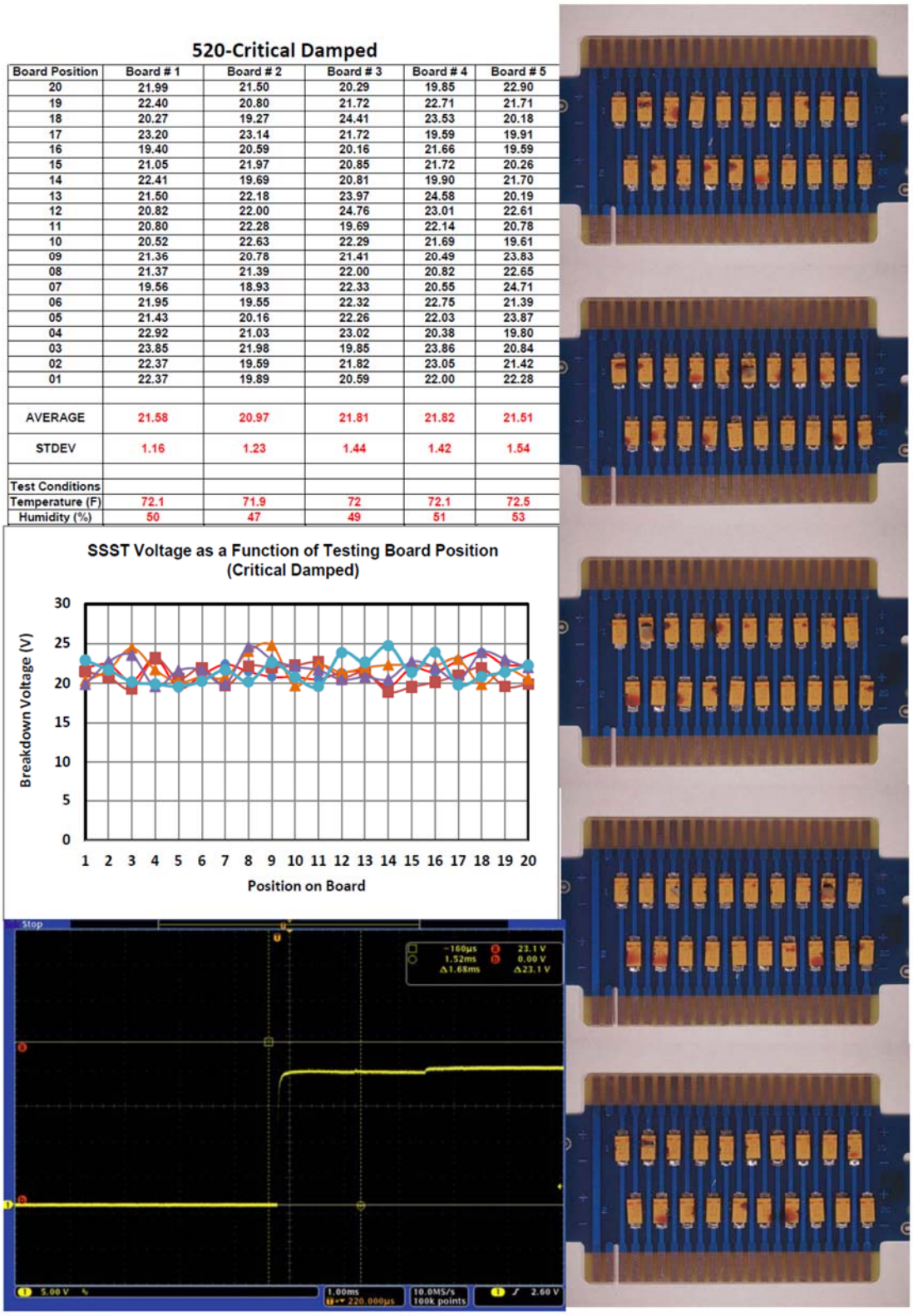


Figure 6a. SSST results for five PCBs for group 520 - reactive-polymerized 220 µF, 6.3V tantalums: Underdamped conditions.



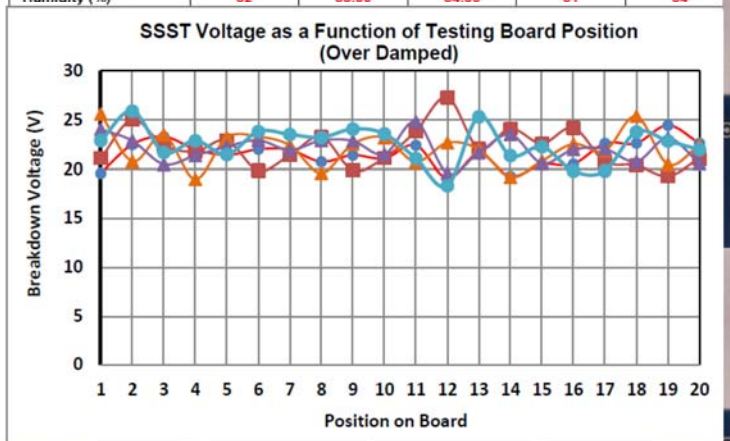
520-Critical Damped

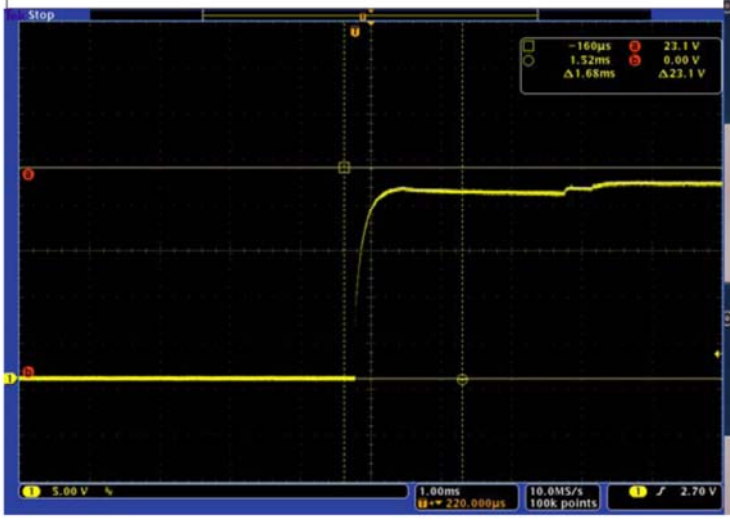
Board Position	Board # 1	Board # 2	Board # 3	Board # 4	Board # 5
20	21.99	21.50	20.29	19.85	22.90
19	22.40	20.80	21.72	22.71	21.71
18	20.27	19.27	24.41	23.53	20.18
17	23.20	23.14	21.72	19.59	19.91
16	19.40	20.59	20.16	21.66	19.59
15	21.05	21.97	20.85	21.72	20.26
14	22.41	19.69	20.81	19.90	21.70
13	21.50	22.18	23.97	24.58	20.19
12	20.82	22.00	24.76	23.01	22.61
11	20.80	22.28	19.69	22.14	20.78
10	20.52	22.63	22.29	21.69	19.61
09	21.36	20.78	21.41	20.49	23.83
08	21.37	21.39	22.00	20.82	22.65
07	19.56	18.93	22.33	20.55	24.71
06	21.95	19.55	22.32	22.75	21.39
05	21.43	20.16	22.26	22.03	23.87
04	22.92	21.03	23.02	20.38	19.80
03	23.85	21.98	19.85	23.86	20.84
02	22.37	19.59	21.82	23.05	21.42
01	22.37	19.89	20.59	22.00	22.28
AVERAGE	21.58	20.97	21.81	21.82	21.51
STDEV	1.16	1.23	1.44	1.42	1.54
Test Conditions					
Temperature (F)	72.1	71.9	72	72.1	72.5
Humidity (%)	50	47	49	51	53

Figure 6b. SSST results for five PCBs for group 520 - reactive-polymerized 220 µF, 6.3V tantalums: Critical damp conditions.

520-Over Damped

Board Position	Board # 1	Board # 2	Board # 3	Board # 4	Board # 5
20	19.60	21.11	25.60	24.05	22.91
19	22.49	25.01	20.80	22.89	25.90
18	23.30	22.40	23.47	20.50	21.69
17	22.01	21.78	19.01	21.38	22.88
16	21.41	22.91	23.19	22.29	21.47
15	22.01	19.85	23.29	22.93	23.81
14	21.95	21.39	22.41	21.95	23.52
13	20.74	23.27	19.62	22.91	23.21
12	21.41	19.89	22.55	22.87	24.07
11	21.07	21.12	23.18	21.51	23.58
10	22.42	23.86	20.73	24.83	21.08
09	19.07	27.30	22.68	19.62	18.34
08	21.56	22.07	22.00	21.66	25.32
07	19.30	24.10	19.22	23.52	21.37
06	20.47	22.60	20.81	20.60	22.27
05	20.51	24.18	22.56	22.00	19.83
04	22.61	20.76	21.85	22.05	19.83
03	22.63	20.39	25.38	20.77	23.78
02	24.45	19.30	20.49	23.17	22.85
01	22.62	21.06	22.41	20.59	21.98
AVERAGE	21.58	22.22	22.06	22.10	22.48
STDEV	1.36	1.99	1.80	1.32	1.85
Test Conditions					
Temperature (F)	72.5	72.50	72.80	73.9	73.8
Humidity (%)	52	55.00	54.00	51	54





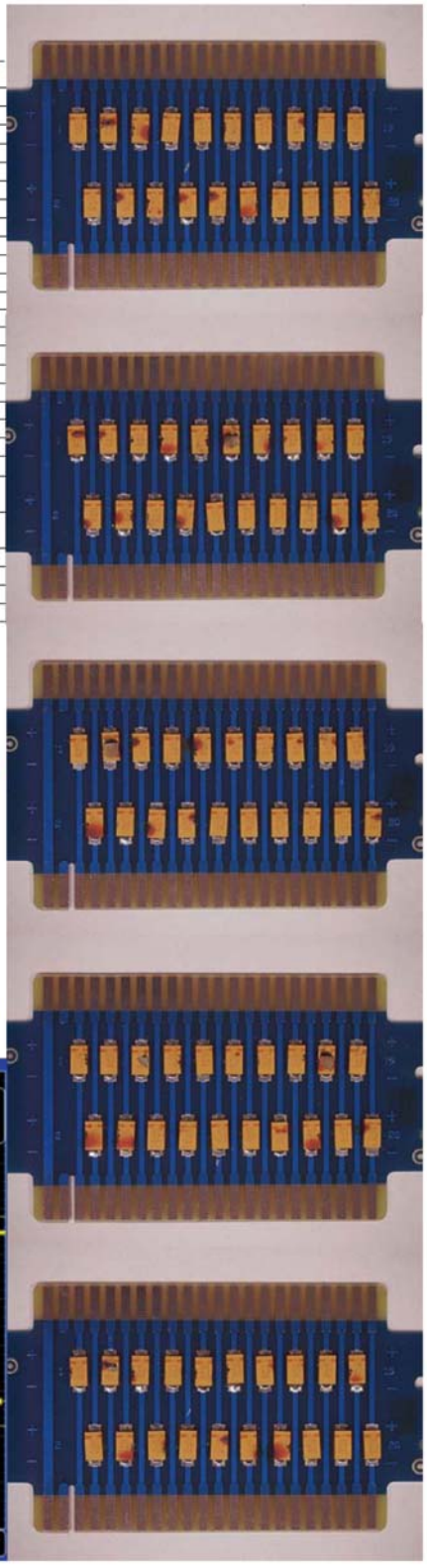
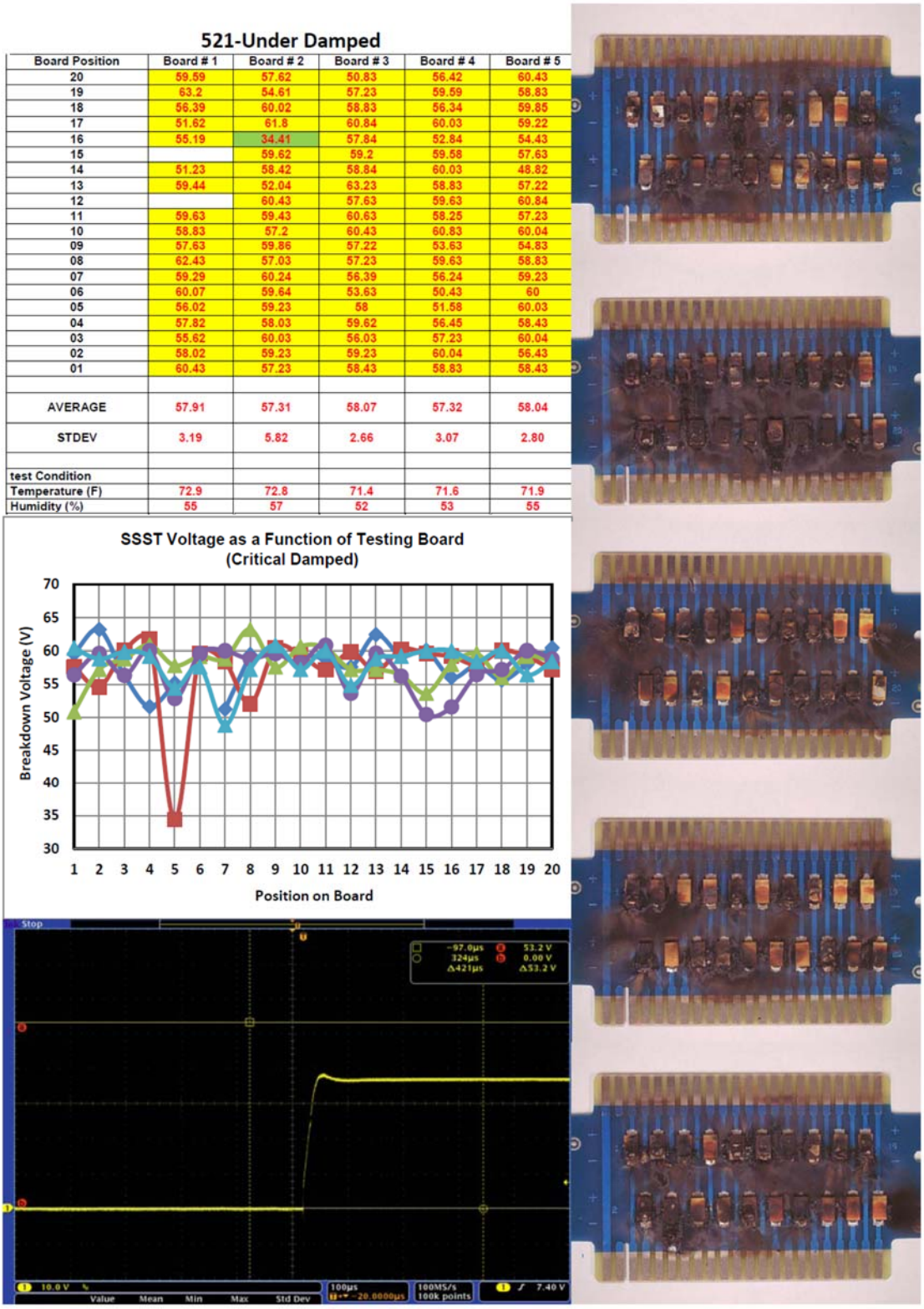


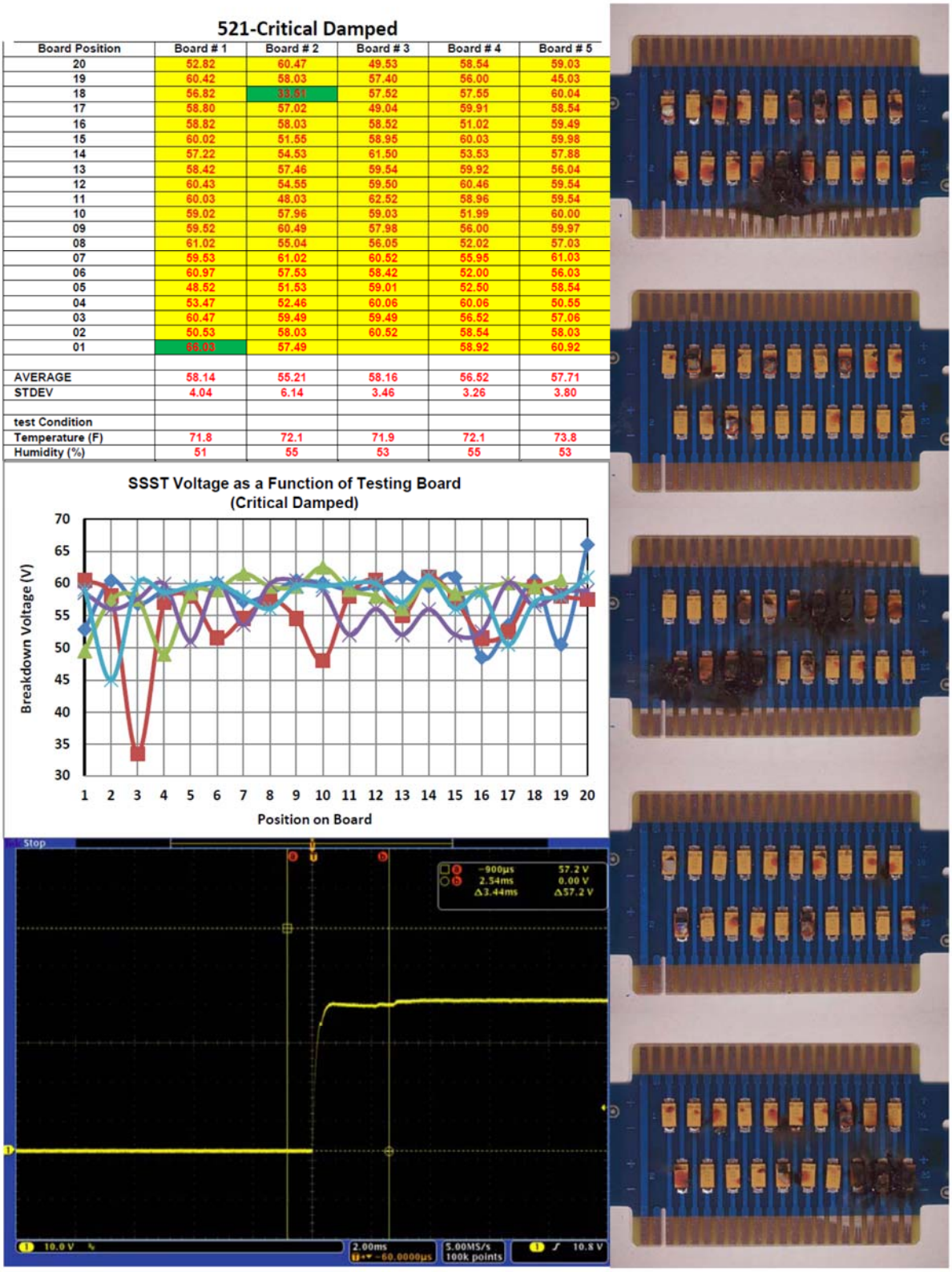
Figure 6c. SSST results for five PCBs for group 520 - reactive-polymerized 220 µF, 6.3V tantalums: Overdamped conditions.



521-Under Damped

Board Position	Board # 1	Board # 2	Board # 3	Board # 4	Board # 5
20	59.59	57.62	50.83	56.42	60.43
19	63.2	54.61	57.23	59.59	58.83
18	56.39	60.02	58.83	56.34	59.85
17	51.62	61.8	60.84	60.03	59.22
16	55.19	34.41	57.84	52.84	54.43
15		59.62	59.2	59.58	57.63
14	51.23	58.42	58.84	60.03	48.82
13	59.44	52.04	63.23	58.83	57.22
12		60.43	57.63	59.63	60.84
11	59.63	59.43	60.63	58.25	57.23
10	58.83	57.2	60.43	60.83	60.04
09	57.63	59.86	57.22	53.63	54.83
08	62.43	57.03	57.23	59.63	58.83
07	59.29	60.24	56.39	56.24	59.23
06	60.07	59.64	53.63	50.43	60
05	56.02	59.23	58	51.58	60.03
04	57.82	58.03	59.62	56.45	58.43
03	55.62	60.03	56.03	57.23	60.04
02	58.02	59.23	59.23	60.04	56.43
01	60.43	57.23	58.43	58.83	58.43
AVERAGE	57.91	57.31	58.07	57.32	58.04
STDEV	3.19	5.82	2.66	3.07	2.80
test Condition					
Temperature (F)	72.9	72.8	71.4	71.6	71.9
Humidity (%)	55	57	52	53	55

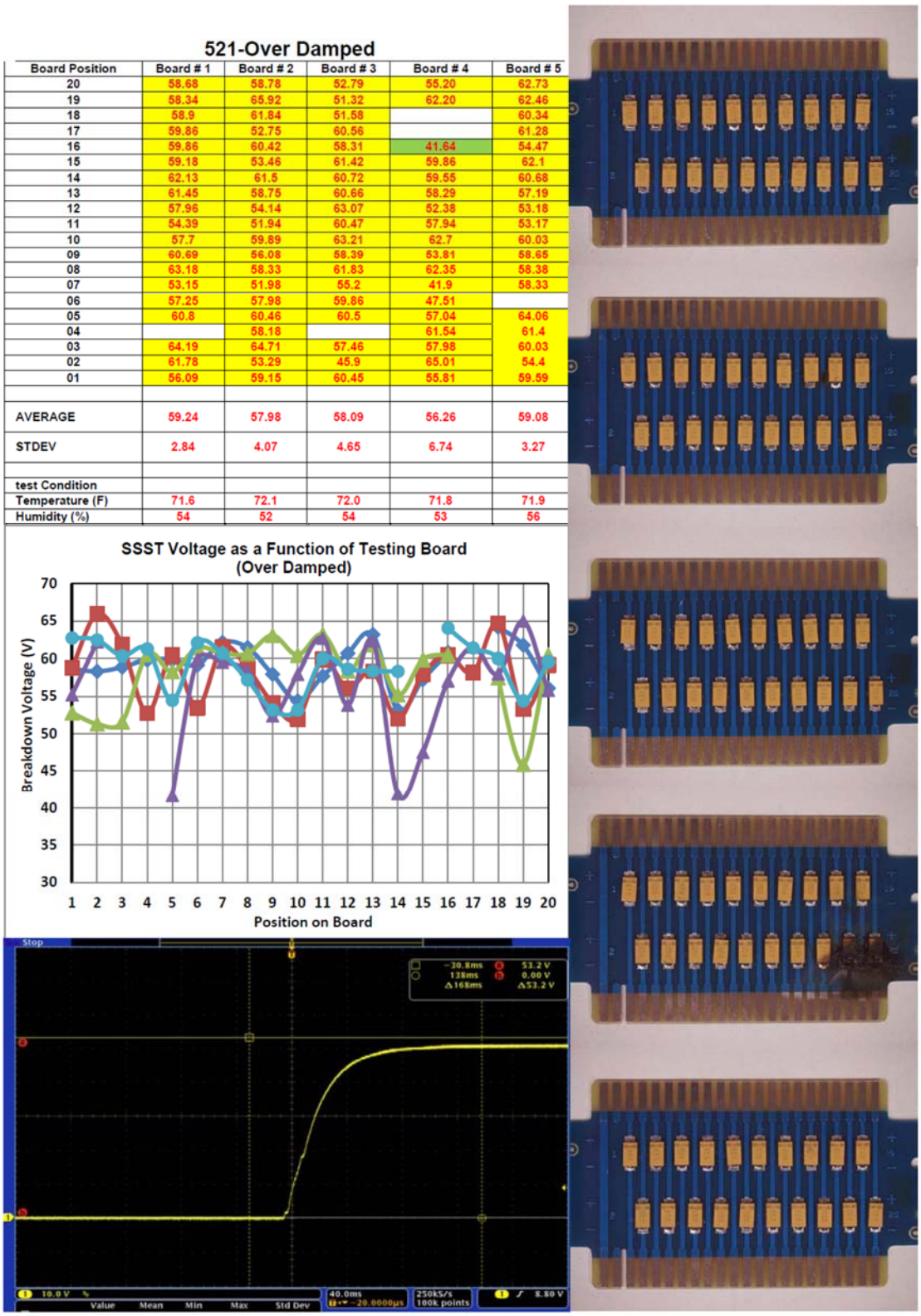
Figure 7a. SSST results for five PCBs for group 521 - pre-polymerized 22 µF, 25V tantalums: Underdamped conditions.



521-Critical Damped

Board Position	Board # 1	Board # 2	Board # 3	Board # 4	Board # 5
20	52.82	60.47	49.53	58.54	59.03
19	60.42	58.03	57.40	56.00	45.03
18	56.82	33.61	57.52	57.55	60.04
17	58.80	57.02	49.04	59.91	58.54
16	58.82	58.03	58.52	51.02	59.49
15	60.02	51.55	58.95	60.03	59.98
14	57.22	54.53	61.50	53.53	57.88
13	58.42	57.46	59.54	59.92	56.04
12	60.43	54.55	59.50	60.46	59.54
11	60.03	48.03	62.52	58.96	59.54
10	59.02	57.96	59.03	51.99	60.00
09	59.52	60.49	57.98	56.00	59.97
08	61.02	55.04	56.05	52.02	57.03
07	59.53	61.02	60.52	55.95	61.03
06	60.97	57.53	58.42	52.00	56.03
05	48.52	51.53	59.01	52.50	58.54
04	53.47	52.46	60.06	60.06	50.55
03	60.47	59.49	59.49	56.52	57.06
02	50.53	58.03	60.52	58.54	58.03
01	66.03	57.49		58.92	60.92
AVERAGE	58.14	55.21	58.16	56.52	57.71
STDEV	4.04	6.14	3.46	3.26	3.80
test Condition					
Temperature (F)	71.8	72.1	71.9	72.1	73.8
Humidity (%)	51	55	53	55	53

Figure 7b. SSST results for five PCBs for group 521 - pre-polymerized 22 µF, 25V tantalums: Critical damped conditions.



521-Over Damped

Board Position	Board # 1	Board # 2	Board # 3	Board # 4	Board # 5
20	58.68	58.78	52.79	55.20	62.73
19	58.34	65.92	51.32	62.20	62.46
18	58.9	61.84	51.58		60.34
17	59.86	52.75	60.56		61.28
16	59.86	60.42	58.31	41.64	54.47
15	59.18	53.46	61.42	59.86	62.1
14	62.13	61.5	60.72	59.55	60.68
13	61.45	58.75	60.66	58.29	57.19
12	57.96	54.14	63.07	52.38	53.18
11	54.39	51.94	60.47	57.94	53.17
10	57.7	59.89	63.21	62.7	60.03
09	60.69	56.08	58.39	53.81	58.65
08	63.18	58.33	61.83	62.35	58.38
07	53.15	51.98	55.2	41.9	58.33
06	57.25	57.98	59.86	47.51	
05	60.8	60.46	60.5	57.04	64.06
04		58.18		61.54	61.4
03	64.19	64.71	57.46	57.98	60.03
02	61.78	53.29	45.9	65.01	54.4
01	56.09	59.15	60.45	55.81	59.59
AVERAGE	59.24	57.98	58.09	56.26	59.08
STDEV	2.84	4.07	4.65	6.74	3.27
test Condition					
Temperature (F)	71.6	72.1	72.0	71.8	71.9
Humidity (%)	54	52	54	53	56

Figure 7c. SSST results for five PCBs for group 521 - pre-polymerized 22 µF, 25V tantalums: Overdamped conditions.

Figure 8 shows the Weibull failure percentage as a function of SSST breakdown voltage (V_{br}) for groups 495 and 521. Similar behavior was observed for group 520 (not shown). It is interesting that V_{br} appears not to be dependent on the damping condition.

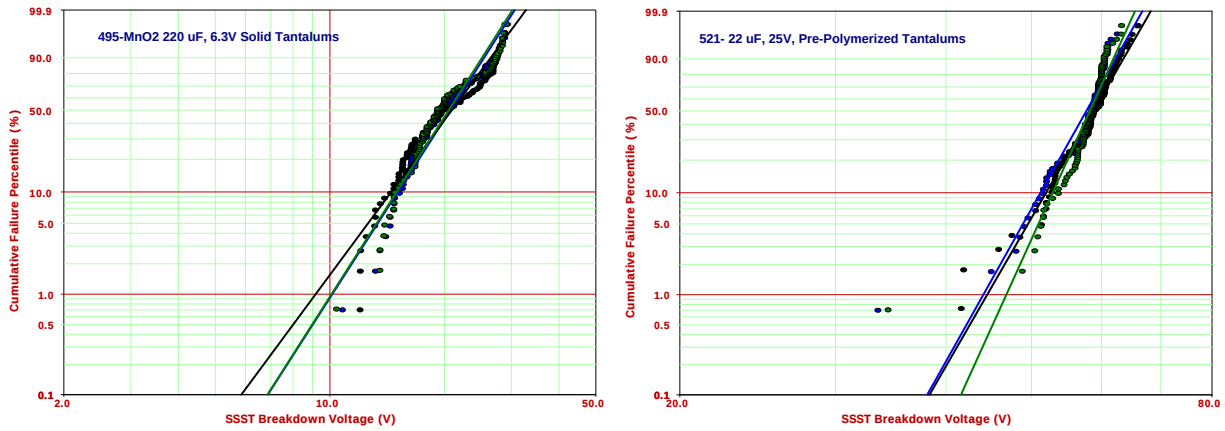


Figure 8. Weibull cumulative failure percentage of SSST breakdown voltage of tantalum capacitors under different damping conditions: group 495 - MnO_2 220 µF, 6.3V, solid tantalums (left); group 521 - pre-polymerized 22 µF, 25V tantalums (right).

The V_{br} at a 100 ppm failure level can be calculated from the data points in Figure 8. The corresponding results are summarized in Table II. Again, the V_{br} *(100 ppm)* did not change significantly with the damping condition. The V_{br} *(100 ppm)* results have been used for the determination of voltage de-rating for various tantalum and aluminum capacitors in the capacitor industry for many years [1]. The approach is very simple: when calculated values of V_{br} *(100 ppm)* / V_{rated} as shown in Table II are greater than 1, there is normally no need for voltage de-rating. If V_{br} *(100 ppm)* / V_{rated} are less than 1, the actual percentage will be the value for de-rating. For example, the V_{br} *(100 ppm)* / V_{rated} values in Table II are all greater than 1 for both types of polymer capacitors, indicating that the voltage de-rating is not necessary "engineeringly" for these capacitors. However, a 20% voltage de-rating is still practiced for most low-voltage polymer tantalum capacitors. This simply adds some extra reliability margins for the applications of these polymer capacitors.

On the other hand, the smallest V_{br} *(100 ppm)* / V_{rated} percentage for MnO_2 solid tantalum capacitors in Table II is 0.59. This suggests a 59% voltage de-rating that must be required for this capacitor group, which is close to the 50% voltage de-rating that has been practiced for years for MnO_2 solid tantalum capacitors. Finally, it is important to point out that the actual values of V_{br} *(100 ppm)* are highly dependent on the percentage of surge voltage overshooting (the transient that exceeds the setting value of V_{br}). In a previous report, 82% of voltage de-rating was reported for 6.3V MnO_2 solid tantalum capacitors [7].

This voltage de-rating percentage was determined when a nearly 20% transient voltage overshoot was observed when the capacitors underwent SSST. This clearly shows that a rapid reduction in V_{br} can be reached if the percentage of transient voltage overshoot occurred. As a result, most tantalum capacitor manufacturers require the surge voltage overshoot to be limited to no greater than 10%. However, in some applications, the tantalum capacitors may see more than 10% voltage overshoot, e.g., the inrush in pulse-width-modulated (PWM) DC/DC converters.

Table II. Calculated SSST Breakdown Voltage at 100ppm Failure Level.

Part ID	V_{br} *(100 ppm)* Under Various Damp Conditions			V_{br}*(100 ppm)* / V_{rated}		
	Underdamped	Critical Damped	Overdamped	Underdamped	Critical Damped	Overdamped
495-Solid Ta, 6.3V	4.66	4.66	3.74	0.74	0.74	0.59
520-Polymer Ta, 6.3V	14.17	14.14	13.24	2.25	2.24	2.10
521-Polymer Ta, 25 V	36.98	32.93	32.99	1.48	1.32	1.32

4. Summary and Recommendations

All tantalum (Ta) capacitors are sensitive to surge current testing. A surge step stress test (SSST) is a surge current test with step-increase stress levels. It is a destructive test that will eventually cause an electrical breakdown for all capacitors being tested. It is also a critical test that will determine the de-rating of a tantalum capacitor when used for high-reliability applications.

A total of 900 Ta capacitors of three types were tested under three transient surge conditions. The test results revealed the following:

1. For solid Ta capacitors, all failures were catastrophic. When less than 12% voltage overshoot occurred, the breakdown voltage at a 100 ppm failure rate suggests a voltage de-rating of 46-52%, consistent with previous reports. If the surge overshoot was more than 12%, a voltage de-rating of greater than 50% was expected.
2. For low-voltage (6.3V) reactive-polymerized Ta capacitors, no impact of surge transient change on the breakdown voltage was observed. All failures were benign. No voltage de-rating is necessary for these polymer Ta capacitors.
3. For high-voltage (25V) pre-polymerized Ta capacitors, the failure patterns are highly dependent on the transient conditions: all units failed catastrophically when surge tested in underdamp conditions, and all units failed benignly when tested in overdamp conditions. Results were mixed when units were tested under critical damp conditions.

Based on this study, it is highly recommended that SSST shall be used for qualify conformance inspection (QCI) of tantalum capacitors when used for critical NASA flight projects, in order to verify the actual percentage of voltage de-rating.

References

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[7] D. Liu, "Failure modes in capacitors when tested under a time-varying stress," *CARTS Proceedings*, Jacksonville, FL, March 28-31, 2011, pp. 210-223.