DERATING OF SURGE CURRENTS FOR TANTALUM CAPACITORS

Alexander Teverovsky

Dell Services Federal Government, Inc.
NASA/GSFC Greenbelt, MD20771, USA
Alexander.A.Teverovsky@nasa.gov

INTRODUCTION

Tantalum capacitors are typically used for reducing noise and stabilizing DC voltage in the power supply lines. When the power is turning-on, high inrush currents through the capacitor can cause so-called surge current failures. For solid tantalum capacitors with manganese oxide cathodes these failures result not only in a short circuit in the system, but can also cause ignition due to the exothermic reaction of tantalum with oxygen generated by the overheated MnO_2 cathode layer. Examples of tantalum capacitors burnt after surge current testing are shown in Fig.1.

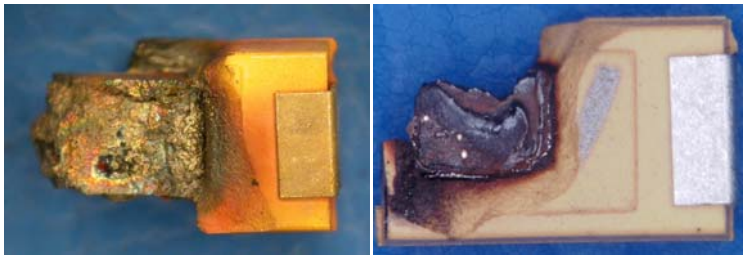

Fig.1. Solid tantalum capacitors with manganese cathodes after surge current testing failure.

The reason for first turn-on failures has not been understood completely, and different hypotheses are discussed in the literature. These include a sustained scintillation breakdown model [1-3]; electrical oscillations in circuits with a relatively high inductance [4-6]; local overheating of the cathode [5, 7-8]; mechanical damage to tantalum pentoxide dielectric caused by the impact of MnO_2 crystals [1, 9-10]; or stress-induced-generation of electron traps caused by electromagnetic forces developed during current spikes [11]. The first turn-on failures are often attributed to damage in the tantalum pentoxide dielectric caused by the soldering-induced stresses.

When the voltage applied to a tantalum capacitor increases gradually, so that no high surge currents develop, a so-called scintillation or local momentary breakdown in the dielectric occurs. This breakdown results in current spikes that are terminated by the self-healing if available current is limited. The self-healing is due to increased local temperature (to ~500 ºC [12])of the manganese cathode in areas of breakdown that results in conversion of the conductive MnO_2 (~1 Ohm×cm) into a high-resistive Mn_2O_3 (~10^4 Ohm×cm). This conversion insulates the damaged area of the dielectric, reduces breakdown currents, and prevents short-circuit failures. In the case of high in-rush currents, self-healing does not have time to develop, and a catastrophic failure of the capacitor occurs.

Our previous analysis [13] showed that when the voltage across the capacitor increases slowly, at a rate ~1 to 5 V/sec, the breakdown voltage (VBR) is substantially, on average by 50%, greater than for the surge current testing, when the rate of voltage increase is in the range from 10^5 to 10^6 V/sec. The effect was attributed to electron trapping in the dielectric that changes the electric field at the interface MnO_2/Ta_2O_5. During surge current breakdown events, the voltage raises rapidly so no trapping of electrons at the energy states in the bandgap of the Ta_2O_5 dielectric occurs. This event is possible only with a fast delivery of charge, and the necessary high currents can be provided by the power supply system. The post-avalanche thermal breakdown is sustained and the failure develops into an explosion due to the exothermic reaction of oxidation of the tantalum pellet.

To assure that the parts operate reliably at high inrush current conditions, tantalum capacitors are screened during manufacturing using surge current testing (SCT). This testing is considered one of the most important techniques to screen out potentially defective tantalum capacitors for low impedance applications and is a must for capacitors used for space applications. Some deficiencies of this test have been discussed before [14], and now we'll consider problems related to derating of tantalum capacitors.

Derating is a means for designers of space systems to further reduce the probability of failures by limiting the level of stresses to capacitors during application. Typical derating requirements for solid tantalum capacitors limit the

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maximum applied voltage to 50% of the rated voltage (VR) and the inrush currents are bounded by additional resistors used in series with the capacitors. First, in the 1960s, the requirement for resistors was 3 Ω per each volt of operating voltage, but by the 1980s, due to improvements in the reliability of the parts and a strong need to increase the efficiency of power supply systems, this requirement was reduced to 1 Ω, and in the 1990s even to 0.1 Ω per volt [6, 15] or 1 Ω, whichever is greater.

The practice of parts engineering for space projects shows that designers often request to relax derating requirements even further, and in many cases even eliminate limiting resistors. Although most guidelines for selection of components for space systems contain requirements for the resistance that should be used in series with tantalum capacitors to limit surge currents, it is not clear how these requirements should be used in conjunction with the voltage derating of the parts. To justify derating requirements a closer look at how the parts are tested at rated conditions is needed. This work analyzes the existing requirements for SCT and suggests a methodology to calculate the value of the limiting resistor if necessary. The basis of the methodology is straightforward; a part cannot be used at conditions that are not guaranteed by testing.

SURGE CURRENT TESTING

The capability of tantalum capacitors to withstand high current transients is evaluated during surge current testing described in the MIL-PRF-55365 standard. A simplified schematic of a PC-based set-up used for SCT that is in compliance with the existing requirements is shown in Fig.2. The source measurement unit, SMU Keithley 2400, allows for setting test voltages (up to 200 V) and measurement of currents through the device under test (DUT) after the stress. The bank capacitor, CB, was 100 time greater than C_{DUT}, and the limiting resistor RB = 100 Ohm. PG is a programmable pulse generator that provides 10 V pulses to the gate of the field effect transistor (FET) with a slew rate of 10 ns and duration of more than 100 μs. Four power L2910 FETs connected in parallel were used as a switch to initiate surge current. A current probe with an amplifier, and an oscilloscope were used to control current spikes during SCT.

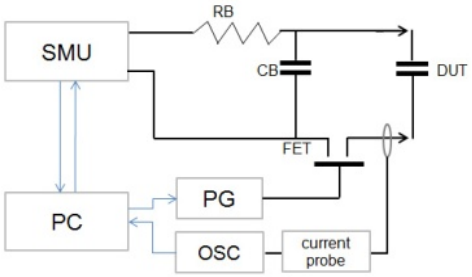


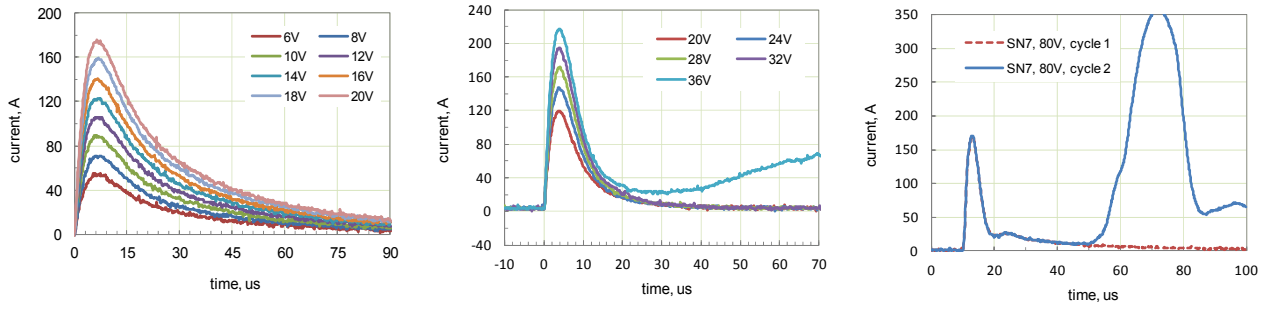
Fig.2. A simplified schematic of the surge current testing.

According to the latest version of MIL-PRF-55365, during SCT the part is subjected to 4 surge cycles (10 cycles was required before December 2012). Each cycle includes charging of CB to the rated voltage for t_{ch} = 1 sec minimum and then discharging it to the device under test for t_{disch} = 1 sec minimum (both times were 4 sec. in the previous version of the specification). The purpose of the bank capacitor, which is required to be not less than 20 times the capacitor under test (not less than 50,000 μF was required before December 2012), is to simulate a power supply with low impedance. The standard requires that the total direct current (DC) resistance of the test circuit, R_{tc}, including the wiring, fixturing, and output impedance of the power supply, shall be a maximum of 1 Ω (R_{tc} =1.2 Ω was required before December 2012).

The minimum peak charge/discharge current value shall be $I_{test} = VR/(R_{tc} + ESR_{CAP})$ where R_{tc} = 1 Ω, ESR_{CAP} is equal to the specified value of the equivalent series resistance (ESR), ESR_{spec}, at +25 ºC and +85 ºC, and 2×ESR_{spec} at -55 ºC. However, no specifics on the method of the I_{test} verification are given. A failure of the capacitor is specified at a level of 1 A after the appropriate time passed since the surge initiation. This time is 1 ms for $C_{DUT} \leq$ 330 μF, 10 ms for 330 μF < $C_{DUT} \leq$ 3300 μF, and 100 ms for C_{DUT} > 3300 μF.

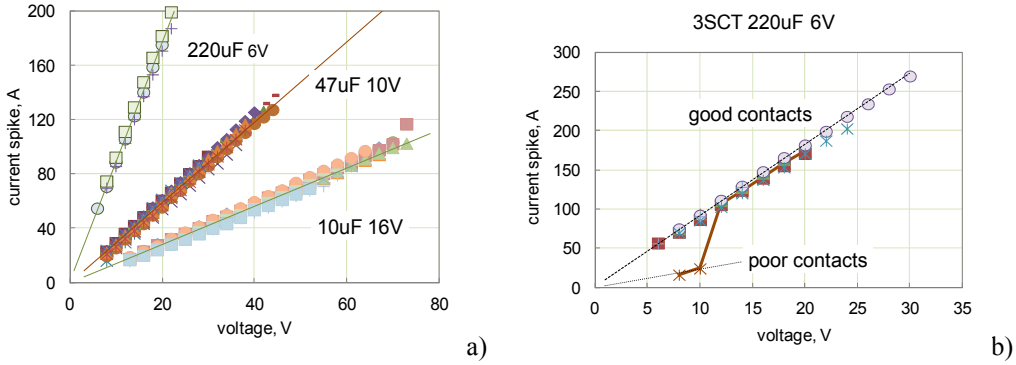
Examples of current spikes observed during the step stress surge current testing (3SCT), when the test voltage increased incrementally after each surge cycle until the moment of failure, are shown in Fig.3. Current spike amplitudes, I_{sp}, are reproducible and increase linearly with the applied voltage (see Fig.4) allowing for calculations of the effective resistance of the circuit, R_{eff}.

The concept of, R_{eff} is useful for the assessment of the quality of contacts during the testing. As an example, Fig.4b shows variations of I_{sp} with voltage for a group of 220 µF 6 V capacitors, for which a typical value of R_{eff} was 0.12 Ω. One sample showed a much higher value of R_{eff} initially, ~0.4 Ω due to a poor (oxidized) contact in the fixture. After cleaning of the contact, the test was continued at normal stress conditions.



a) b) c)

Fig.3. Current spikes during surge current testing. (a) Testing of a 220 µF 6 V capacitor at increasing voltages. (b) Testing of a 47 µF 20V capacitor that failed at 36V. (c) Testing of a 15 µF 50 V capacitor that failed during the second cycle at 80 V.

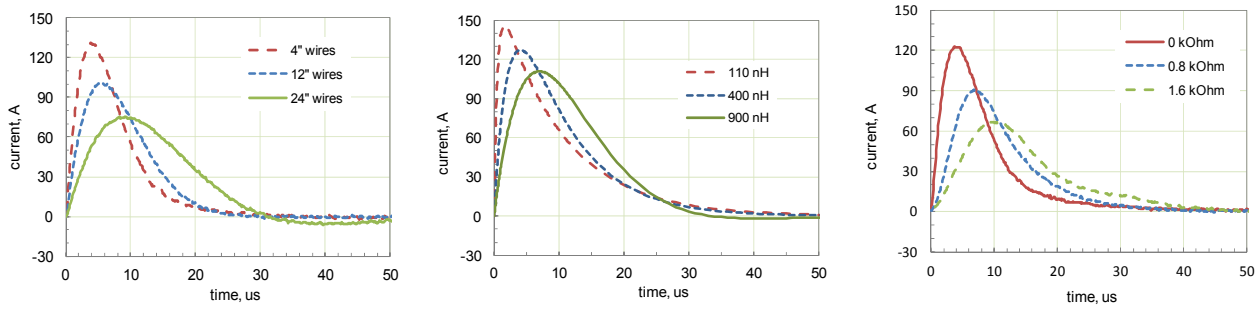


a) b)

Fig.4. Variations of surge current spike amplitudes with applied voltage. (a) Reproducibility of current spikes for three types of capacitors with 4 to 7 samples in each group. (b) A lot of 220 µF 6 V capacitors with one sample having a poor contact initially. After testing at 10 V, the contacts were cleaned.

FACTORS AFFECTING SURGE CURRENT TESTING

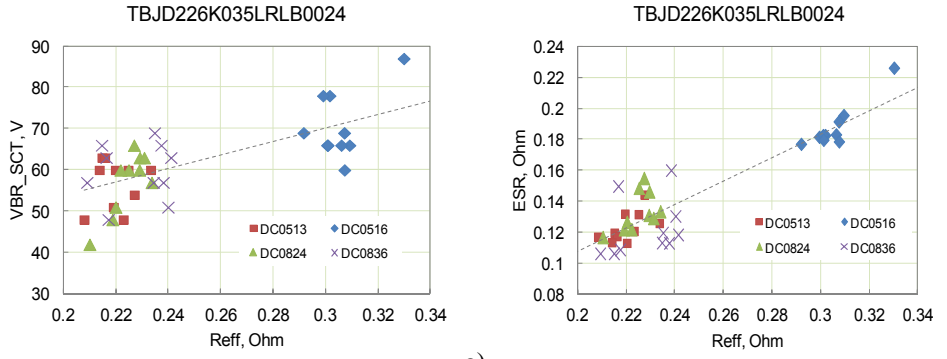
It has been shown previously [16] that the inductance of the test circuit and the type of the switch might substantially affect results of SCT. Experimental evidences of the effect of the wire length and the rate of voltage increase at the gate of the FET are shown in Fig.5. An increase in the wires connecting DUT with the test circuit from 4" to 24" reduces the current spike during testing of 47 µF 20 V capacitors from 135 A to 75 A and increases the duration of the spike from ~ 10 µs to ~ 20 µs. These results are in close agreement with the calculations of transients in an R-L-C circuit [16] shown in Fig. 5.b. Fig.5c shows experimental data for SCT carried out with resistors of 0.8 kΩ and 1.6 kΩ connected between the pulse generator (see Fig.2) and the gate of FET. Introduction of these resistors slowed the rate of voltage increase at the gate and resulted in a substantial decrease in the current amplitude and increase in the pulse width (~ 2 times).



a) b) c)

Fig.5. Experimental (a, c) and calculated (b) current spikes for 47 µF 20V capacitors. The resistance of the circuit used for simulations was 0.25 Ω. Figure (c) shows the effect of the gate resistors on current spikes.

The value of the effective resistance of the test circuit, R_{eff}, has a direct effect on the results of the testing. Fig.6a shows correlation between VBR and R_{eff} for four lots of 22 µF 35 V capacitors. Additional analysis (see Fig. 6.b) showed that variation of R_{eff} were mostly due to the variations of ESR. Although the spread of the data is large, there is a clear trend of increasing VBR with R_{eff}. On average, increasing R_{eff} from 0.22 Ω to 0.32 Ω resulted in increasing breakdown voltages of ~ 20%, from 60 V to 70 V.



a) b)

Fig.6. Correlation between breakdown voltages and the effective resistance of the circuit (a) and between R_{eff} and ESR for 22 µF 35 V capacitors from four different lots.

Variations of VBR and R_{eff} with temperature for two types of capacitors, 47 µF 20 V and 220 µF 6 V, measured in the range from -55 °C to +85 °C are displayed in Fig.7. Both parameters, R_{eff} and VBR, are decreasing with temperature. It is quite possible that increasing of VBR with decreasing temperature is partially due to rising ESR, hence R_{eff}, caused by the increased resistance of the manganese layer at low temperatures.

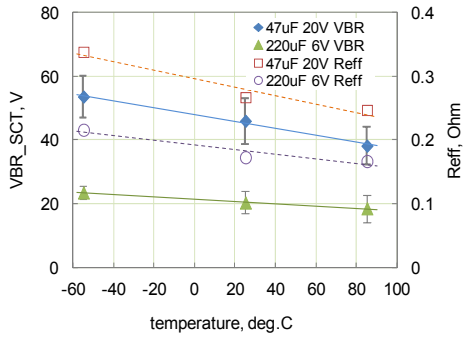


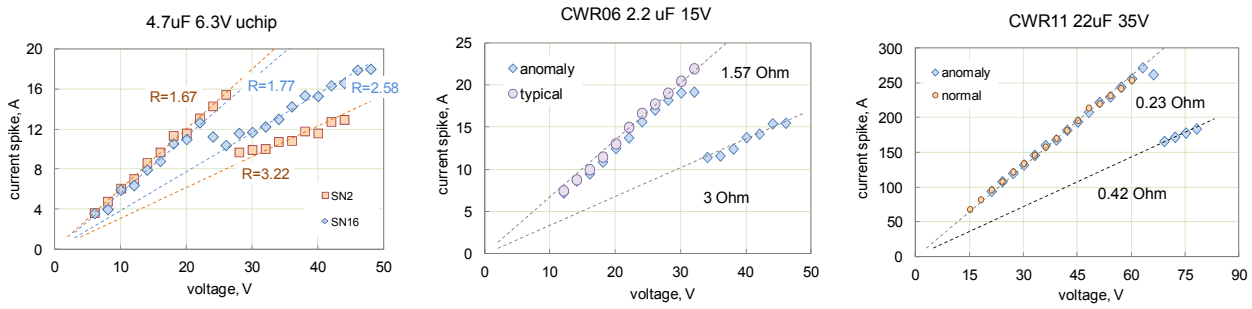
Fig.7. Temperature dependence of VBR and R_{eff} for 47 µF 20 V and 220 µF 6 V capacitors.

Experiments showed [14] that in some cases SCT can degrade ESR in tantalum capacitors. This phenomenon happens more often for small-size capacitors and is likely due to development of substantial mechanical stresses in the parts

associated with surge currents. These stresses might cause formation of microcracks and delaminations between the cathode layers (manganese oxide – carbon - silver epoxy 1 – silver epoxy 2 – metal lead frame). The effect is, for relatively small-size parts, likely due to a thin plastic package that does not create large enough compressive stresses that would suppress tensile stresses caused by surge currents. As a result of this damage, ESR of the capacitor is increasing, which limits the rate of voltage increase and the amplitude of current spikes.

Fig.8 shows examples of variations of I_{sp} with voltage during 3SCT for three types of capacitors. In all cases, a linear relationship $I_{sp}(V)$, which is typical for the majority of parts, changes after a certain voltage to a linear relationship with a lesser slope. In all cases, the capacitors with increased ESR (and so R_{eff}) had greater breakdown voltages.

Erik Reed studied the effect of series resistance, R, used during 3SCT on the breakdown voltage of solid tantalum capacitors [15]. At R in the range from ~0.1 to ~10 Ω, average values of VBR increased with R according to a power law: VBR = $a \times R^{\beta}$, where a is the constant, and $\beta \sim 0.2$. Using this equation, an increase of R_{eff} from 0.22 Ω to 0.32 Ω should have increased VBR by ~ 8%, which is in a reasonable agreement with our results.



a) b) c)

Fig.8. Anomalies in variations of current spike amplitudes with voltage caused by formation of microcracks for 4.7 µF 6.3 V microchip capacitors (a), 2.2 µF 15 V CWR06 capacitors (b), and 22 µF 35 V CWR11 capacitors. Note that last points on the curves correspond to breakdown voltages.

A close correlation between R_{eff} and ESR (see Fig.9) is always observed during 3SCT when a set-up is optimized to achieve maximum current spikes: no limiting resistors, use of a proper switch, good quality of contacts, minimal length of wires, etc. In the optimized set-up, the difference between R_{eff} and ESR can be made low, typically in the range from 0.1 Ω to 0.2 Ω.

One of the methods used to demonstrate adequate SCT conditions is the measurement of voltage across the capacitor under test at some time after the surge current initiation. The presence of a voltage that exceeds 0.9×VR is considered evidence of normal test conditions. However, the moment of measurements is critical: by waiting long enough the voltage would increase close to VR even at relatively large values of R_{eff}. Fig.10 shows an example of calculations of the currents and voltages during surge current testing for 220 µF 6 V capacitors at different values of the contact resistance, from 0.1 Ω, which can be considered as a "good" contact, to 0.7 Ω, which might be due to a contaminated or oxidized fixture. Results show that, independent of the contact resistance, the voltage after 400 µs will increase above 0.9×VR. Typically, the testing time for voltage is set to 1 to 10 ms. Even at 1 ms, 220 µF capacitors with contact resistance of more than 2 Ω would pass the test. The less the capacitance, the greater contact resistance would be accepted: for example, 22 µF capacitors might have circuit resistance up to 20 Ω, but still the voltage after 1 ms would reach ~ 90% of the test voltage.

Contrary to the voltage measurements, current spike amplitudes decrease almost four times, from ~ 4.5 A per V at R = 0.1 Ω to ~ 1.2 A per V at R = 0.7 Ω. This example shows that measurements of I_{sp} can immediately reveal parts with increased contact resistances. If not detected, these parts would pass the screening without experiencing the required level of stress.

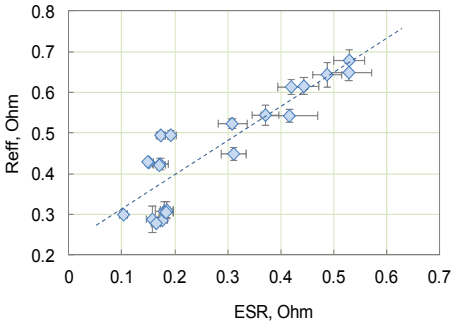


Fig.9. Correlation between Reff and ESR measured at 100 kHz for 23 lots of tantalum capacitors.

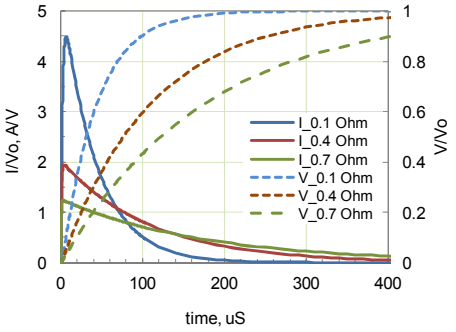


Fig.10. Simulation of current and voltage spikes in 220 μF 6.3Vcapacitors that have ESR = 0.1 Ω and are tested in a circuit with inductance 400 nH and contact resistances of 0.1, 0.4, and 0.7 Ω

To verify adequate SCT conditions, direct measurements of I_{sp} and the assessment of $R_{eff} = VR/I_{sp}$ should be made. If R_{eff} – ESR is below 0.5 Ω, the conditions of SCT are acceptable. This verification should be made for each tested part at each cycle of the testing.

EXPERIMENTAL AND SPECIFIED VALUES OF ESR.

During SCT per MIL-PRF-55365, the current spike is verified based on the specified values of ESR for the part. Because ESR_{spec} indicates a maximum acceptable level, real ESR values and, respectively, current spikes during application, might be much greater. Let us consider an example of a CWR06 15 μF, 10 V capacitor used in a low-impedance, 5 V power supply line. The specified value of ESR for this part is ESR_{spec} = 2.5 Ω, but an actual ESR is 0.5 Ω. After assembly onto a board, the part can experience a spike I_{appl} = 5/0.5 = 10 A, whereas during the testing it will be verified to the "rated" current spike $I_{test} \geq VR/(R_{tc} + ESR_{spec})$ = 10/(1 + 2.5) = 2.8 A, which is much less than the current during application. This example shows that a substantial difference in the level of surge current stress might exist between the testing and application conditions and indicates a need for a closer look on the relationship between the specified and actual ESR values.

Analysis shows that ESR distributions can be accurately enough described with a normal function with relatively small standard deviations, σ. For example, based on measurements of 18 lots of 50 V capacitors, σ varies from 6 mΩ to 44 mΩ and the ratio of σ to the mean value is small, from 1.6% to 6.6%.

Measurements showed that for capacitors rated to the same values of C and VR, but to different maximum values of ESR_{spec}, the actual values of ESR are not necessarily less for the parts rated to lower values. For example, capacitors rated to 0.3 Ω had mean ESR value of 0.19 Ω, whereas capacitors rated to 0.7 Ω had a close mean value of 0.17 Ω. This indicates that, contrary to the specified nominal capacitance which is close to the actual values, ESR_{spec} indicates a maximum to which the parts were screened, their real values might be much lower, and there is a rather poor correlation between the specified and actual values. This situation might complicate a selection of correct part types.

Fig. 11 shows that capacitors with different lot date codes might have significantly different ESR, but still remain within the specified limits. Analysis of different part types showed that the specified values might exceed the actual ESR values up to 10 times (see Fig.12). Although the spread of the data is large, mean values for low-ESR CWR29 type capacitors are closer to the limit than for CWR06 capacitors. Table 1 shows average ratios of ESR_{spec}/ESR_{mean}, the relevant standard deviations, and the number of tested lots for three types of military-grade tantalum capacitors. Maximum ratio, ~7, for CWR06 and minimal, ~2, for CWR29 type capacitors.

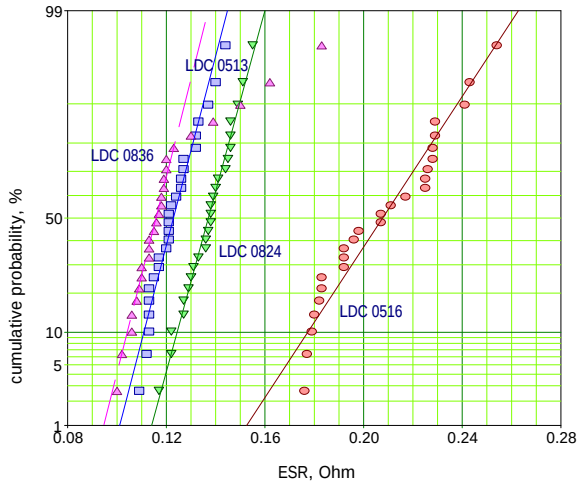


Fig.11. Example of ESR distributions for four lots of 22 µF 35 V capacitors with different lot date codes. Note that the specified maximum ESR for these parts is 0.4 Ω.

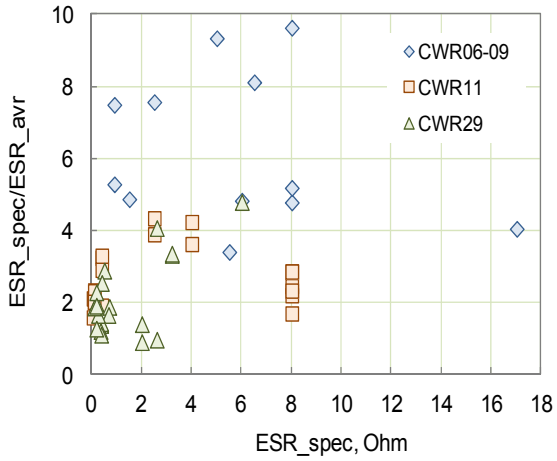


Fig.12. Correlation between the ratio of the specified and average ESR values and specified ESR for different types of capacitors.

Table 1. Ratio of the specified and average ESR values for different part types.

	CWR06	CWR11	CWR29
ESR_{spec}/ESR_{mean}	6.92	2.72	2.04
STD	2.64	0.83	1.02
Lots QTY	14	20	23

DISCUSSION

At typical application conditions, the capacitor is soldered onto a board and the contact resistance and inductance of the circuit are minimal. In this case, for low-impedance circuits, surge currents are limited mostly by the ESR of the capacitor. Contrary to that, during testing per MIL-PRF-55365, the contact resistance and the length of the wires are not specified, and there might be a limiting resistor, up to 1 Ω. This, as well as the difference between ESR_{spec} and the actual ESR values might result in a situation when the amplitude of surge current spikes during application is greater that during the testing. To avoid similar situations, a limiting resistor should be used.

During surge current testing according to MIL-PRF-55365, the minimum current spike amplitude is verified to the level:

$$I_{test} = \frac{VR}{R_{tc} + ESR_{spec}}, \quad (1)$$

where the resistance of the test circuit, R_{tc}, should be less than 1 Ω.

This level can be considered as a rated surge current for tantalum capacitors. Although the actual current spike during SCT might be greater than I_{test}, the testing assures surge currents to the verifiable level, so the value per Eq.(1) will be used for the following analysis.

If the maximum current of the power supply (PS), I_{PS}, is below the level of current spike during surge current testing, I_{test}, no additional resistors are required. Note that in the case of PS with current compliance, to avoid high currents during transients, the clamping time of PS should be less than the typical width of the SCT spikes. For relatively low-value capacitors, the spike width is ~ 10 µs, and this time can be used for an assessment of the required clamping time.

Let us assume that the current during applications is limited by a resistor R_{ac}. Due to voltage derating, maximum voltage V_a across the capacitor is $V_a = \alpha \times VR$, where α is the voltage derating factor, $\alpha = 0.5$. For the part to be used at conditions, which are guaranteed by testing, the current during applications should be less than the testing current: $I_a < I_{test}$.

The current spike during applications is:

$$I_a = \frac{\alpha \times VR}{R_{ac} + ESR}. \quad (2)$$

If we want to be extremely cautious, we might limit the current spike to the level $\beta \times I_{test}$, where β is the current derating factor. In this case:

$$I_a < \beta \times I_{test}, \quad (3)$$

$$\text{or} \quad \frac{\alpha \times VR}{R_{ac} + ESR} < \frac{\beta \times VR}{R_{test} + ESR}.$$

This gives the requirement for a resistor that should limit current spikes during applications:

$$R_{ac} > \frac{\alpha}{\beta} \times R_{tc} + \frac{\alpha}{\beta} \times ESR_{spec} - ESR \quad (4)$$

Assuming derating factors of 50%, $\alpha = \beta = 0.5$. In this case, R_{ac} always exceeds R_{test} and the limiting resistors are always necessary. However, derating of the maximum current spike on the top of the voltage derating is not necessary. Experiments show that solid tantalum capacitors can tolerate discharge currents at much higher levels of voltage (typically, close to the scintillation breakdown) than the charge currents, so current spikes are much more "dangerous" in combination with the increasing voltage that happens during charging. This indicates that a fast voltage increase to sufficiently high level is critical for surge current failures, and high current spikes are byproducts of the fast voltage increase rather than the prime cause of failures. For this reason, we can assume $\beta = 1$ and the requirement for additional resistance during applications is:

$$R_{ac} > \alpha \times R_{tc} + \alpha \times ESR_{spec} - ESR, \quad (5)$$

Obviously, if $R_{ac} < 0$ (practically, below 0.05 Ω), no additional resistors are required. An algorithm for surge current derating and making a decision on the need for the limiting resistor is described below.

First, the current spike amplitude during standard SCT is estimated based on the specified value of ESR and Eq.(1). If $I_{PS} < I_{test}$, no resistor is required. Otherwise, the additional resistor should be in compliance with the requirement per Eq.(5). If the latter is not acceptable for the performance of the circuit, additional testing and analysis are required: (i) the value of ESR should be determined experimentally, and (ii) SCT should be carried out at the optimized conditions with the effective resistance of the test circuit below 0.5 Ω. In this case, Eq.(5) can be replaced with the following requirement:

$$R_{ac} > \alpha \times R_{tc} + (1 - \alpha) \times ESR, \quad (6)$$

where $\alpha = 0.5$, $R_{tc} = 0.5$ Ω. Note that for conservative estimations, the value of ESR can be determined as ESR_{spec}/N, where $N = 10$, 5, and 3 for CWR06, CWR11, and CWR29 types of capacitors respectively. If $R_{ac} > 0.05$ Ω, further analysis requires obtaining of the actual worst case voltage during application, V_a. Calculations per Eq.(6) should be repeated at $\alpha = V_a/VR$. For example, if a 35 V capacitor with ESR = 0.25 Ω has been tested in a circuit with $R_{tc} < 0.5$ Ω, and is planned to be used in a 12 V line, the required resistance $R_{ac} = 12/35 \times 0.5 - (1 - 12/35) \times 0.2 = 0.005$ Ω. This resistance is comparable with the resistance of circuit interconnections, so there is no need in the additional limiting resistor. If the result is still not satisfactory, SCT at conditions with a reduced R_{tc} values (less than 0.5 Ω) and/or at voltages greater than VR (e.g. 1.1VR) might be necessary.

It is known that the capability of tantalum capacitors to sustain surge currents can be impaired by thermo-mechanical stresses associated with soldering. If soldering conditions deviate from the one recommended by the manufacturer, and especially, if manual soldering is used, additional qualification testing is required. For this testing, a group of 10 capacitors, minimum, should be stressed by conditions that closely simulate actual soldering conditions. For example, manual soldering can be simulated by the terminal solder dip testing [17]. Surge current testing, leakage current and ESR measurements should be made before and after the soldering stress simulations. No failures or any substantial degradation of parameters are allowed.

Although soldering-related first turn-on failures are possible, it is also possible that the failures are due to non-adequate test conditions during SCT. To reduce the probability of failures, both optimization of conditions for surge current testing and additional verification of the robustness of tantalum capacitors to soldering stresses are needed.

CONCLUSION

1. Measurements of current spike amplitudes during SCT allow for estimations of the effective resistance of the test circuit, R_{eff}, and should be used to assure that the parts are properly stressed during the testing. Acceptable test conditions can be determined as $R_{eff} \leq 0.5 + ESR$.
2. Tantalum capacitors manufactured per MIL-PRF-55365 might fail because the surge current test conditions during manufacturing are less stressful compared to the application conditions.
3. An algorithm and procedures necessary for selection of limiting resistors to derate surge currents or for making a decision to use tantalum capacitors without additional resistors are suggested.

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