RTAX-S Single Event Effects (SEE) High-Speed Test Results - Update

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This work was sponsored by the NASA Electronic Parts and Packaging (NEPP) Program

Outline

- Introduction
- Devices Under Test (DUTs) Description
- Test Approach
- Test Results
  - Heavy Ion
  - Proton
- Summary

Introduction

- Some preliminary single event effect (SEE) data existed on the RTAX-S devices
  - Lots during device development
  - Low-speed tests
  - Data showed fairly good single event upset (SEU) tolerance, but further data required
  - Previous Katz Quarterly (1/06) preliminary high-speed test results were presented
    - *This presentation provides an update to that data*
- NEPP objectives for testing were to evaluate frequency, fanout, and combinatorial logic effects for both heavy ion and proton SEE
  - Testing performed at Texas A&M University (TAMU) Cyclotron: 11/2005, 02/2006, and 04/2006
  - Testing performed at Crocker Nuclear Laboratory (CNL) at the University of California at Davis (UCD) on 12/2005 for protons
  - Testing performed at the Indiana University Cyclotron Facility (IUCF) on 03/2006 for protons
- All testing performed in collaboration with Actel

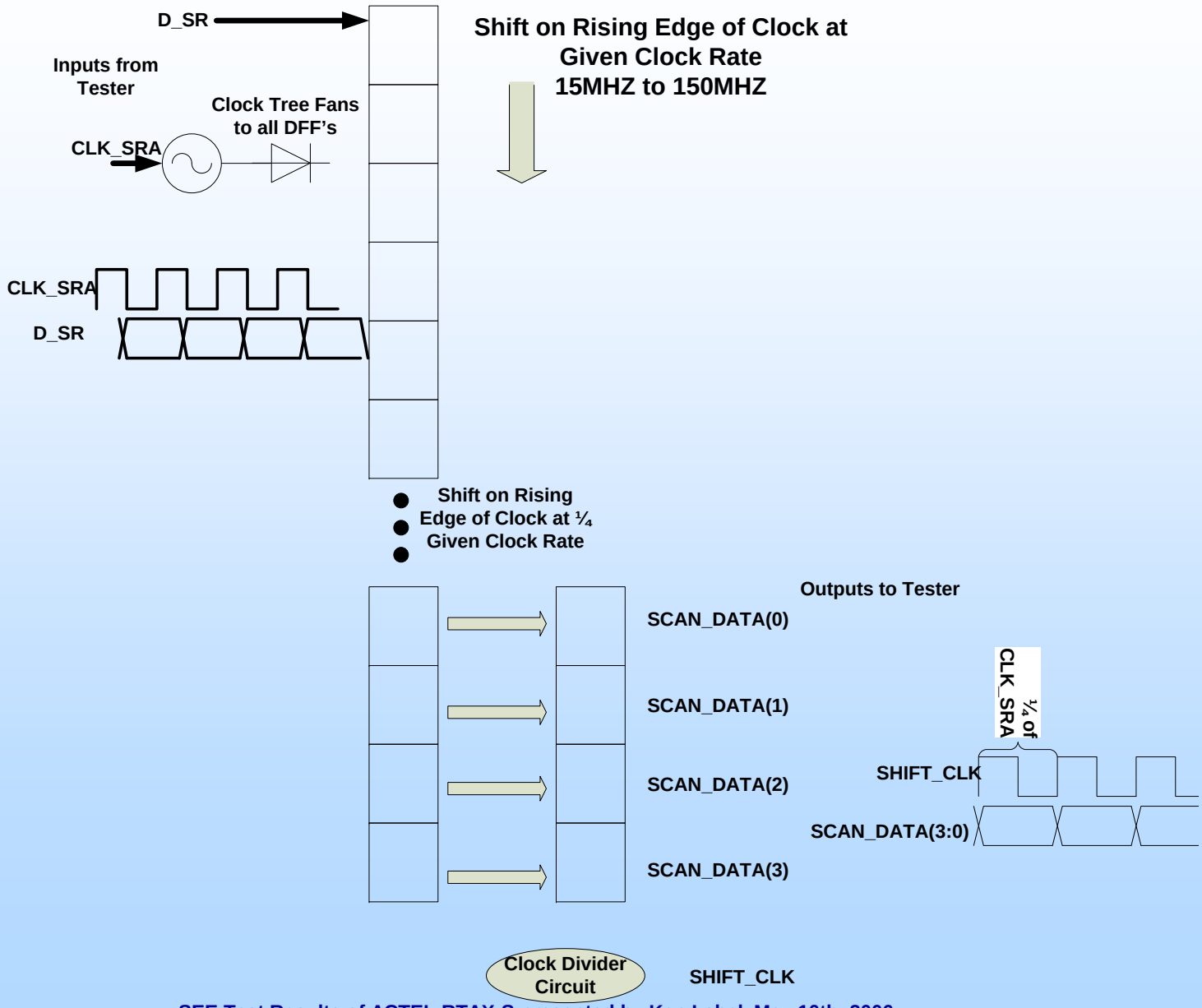
DUTs

- Purpose: To investigate SEUs/SETs and their dependencies concerning:
  - Frequency
  - Data Pattern
  - Architectural (combinatorial logic vs. sequential)
- Frequency ranged from 15 MHz to 150 MHz
- Data Patterns varied from all zeroes, all ones, and checkerboard
- 6 different architectures tested
  - Architectures chosen to examine hardened characteristics of the RTAXS series
  - Sample size of 2 parts each per architecture
- DUTs were
  - RTAX2000S and RTAX1000S
    - Label of 1000E used for “special” DUT architecture configuration

Test Approach:
DUT Architectures - Overview

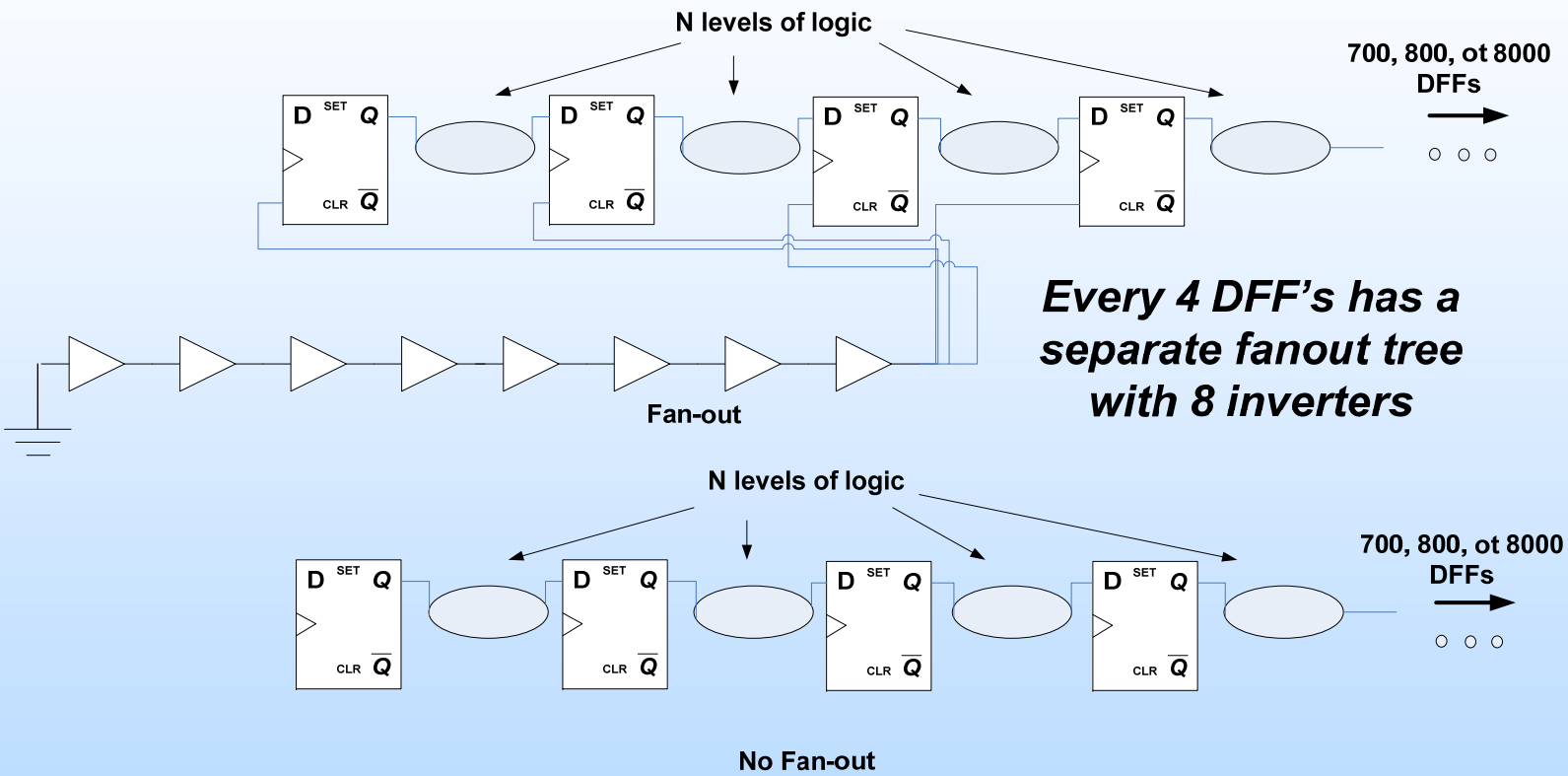
- **The Principle Test Structure is a shift register string (700 to 8000 DFF's) with:**
  - **varying levels of combinatorial logic (0, 4 or 8 inverters between DFF's) and**
  - **Fanout options to the Enable inputs.**
- **Data Capture**
  - **A By-4 clock divider circuit is implemented to shift the last 4 bits of the Shift register string into a DFF window (SCAN_DATA). The window is output to the tester.**
  - **A data clock (SHIFT_CLK) is also output to the tester for high speed synchronous data capture.**

Top Level DUT Architecture



Shift Register String Details

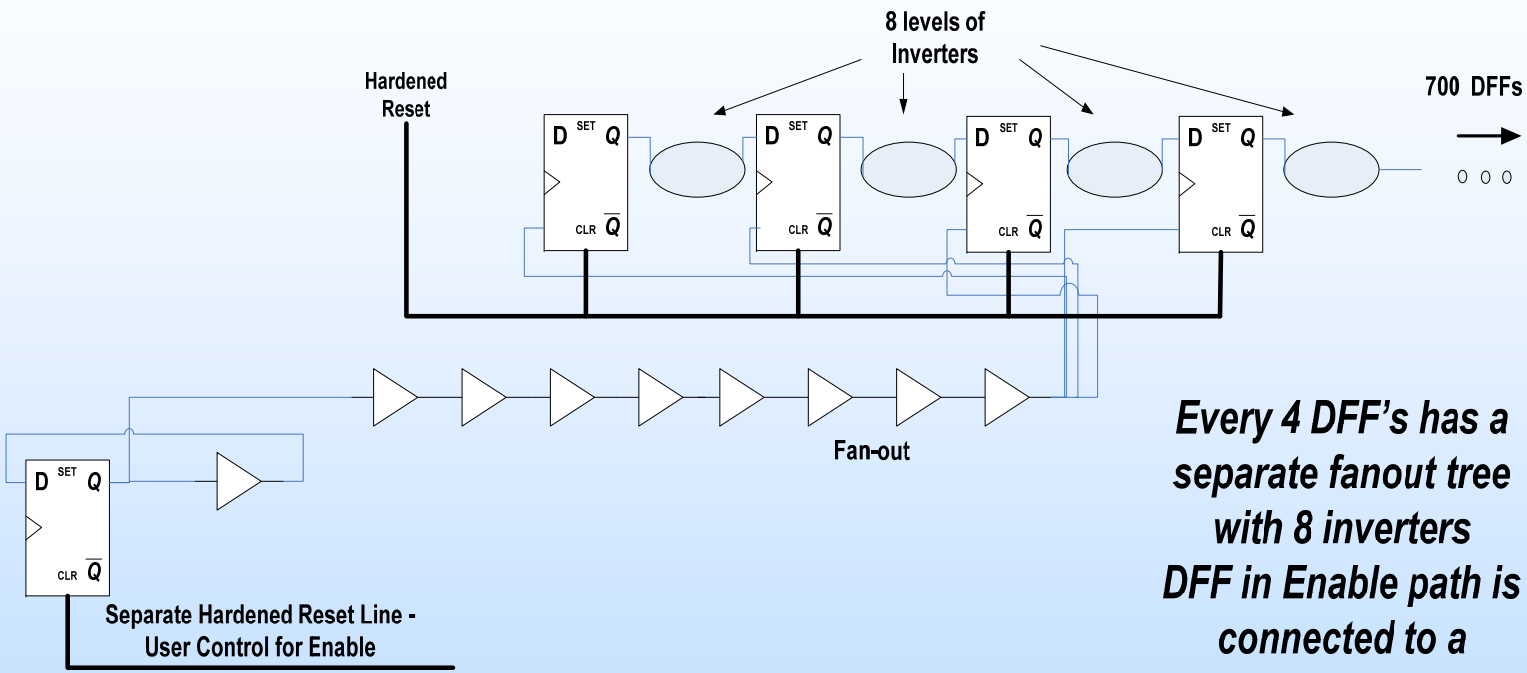
N = 0 or 8 inverters



Every 4 DFF's has a separate fanout tree with 8 inverters

- **8F8L in RTAX 1000 device: 700 DFF's N=8 with Fanout**
- **8F0L: 700 DFF's N=0 with Fanout**
- **RTAX2000 (contains two architectures): 8000 DFF's N=0 no Fanout and 800 DFF's N=0 no fanout**

Special Shift Register String

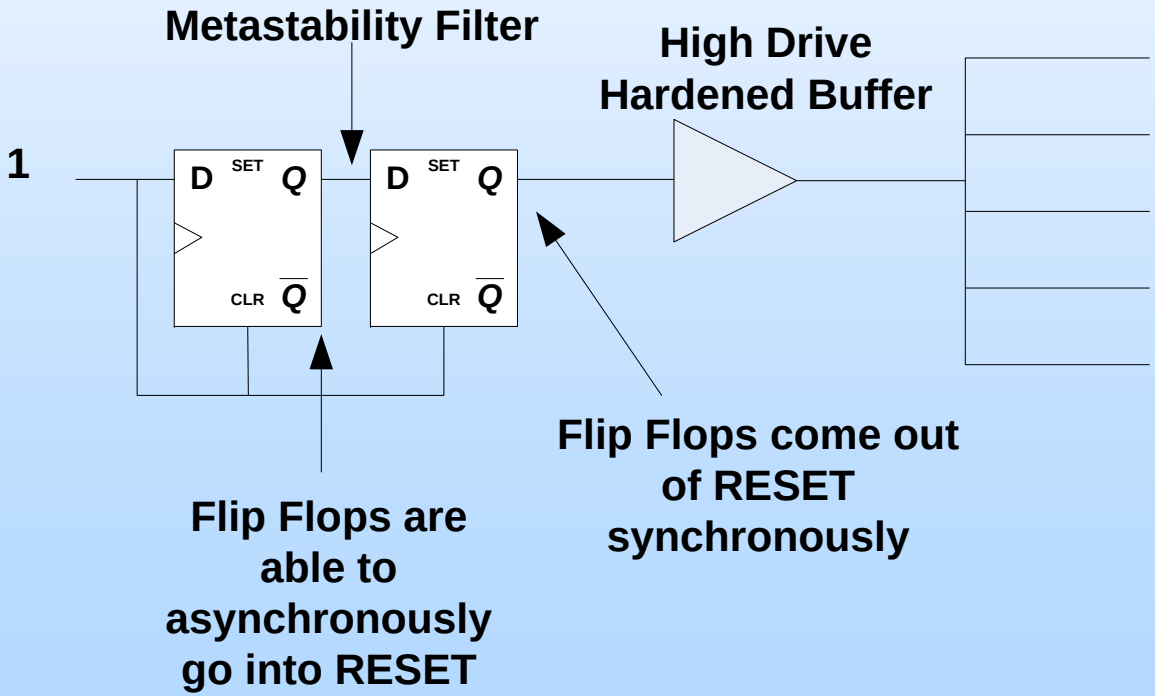


Every 4 DFF's has a separate fanout tree with 8 inverters DFF in Enable path is connected to a separate Reset line

- 8F8L Type Arcitecture
- Enable to DFF's can be disabled by placing ENABLE DFF's in Reset
- Enable to DFF's (when not in reset) is active every other cycle (inverter)
- Implemented in RTAX1000 Device type

DUT Reset Circuit

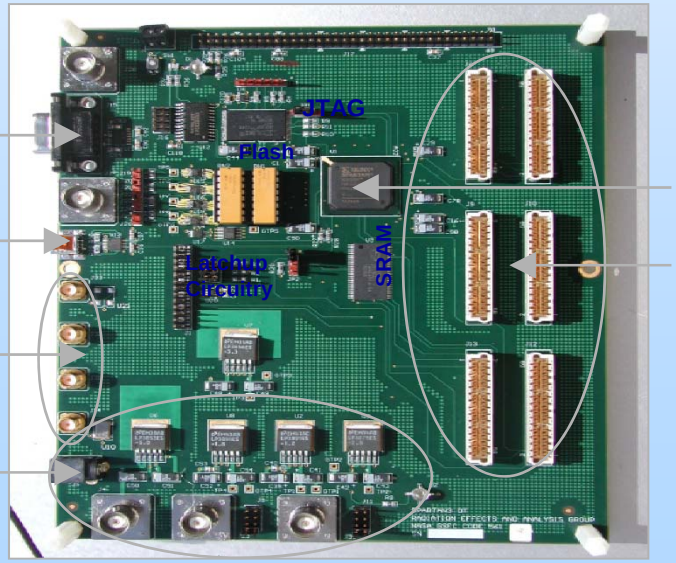
- Reset passes through an asynchronous assert – synchronous de-assert circuit and is supplied to every DFF.
- Reset is connected to Input Pad in order to be controlled by the tester
- *Note: RTAX2000S and RTAX1000S used single reset tree; 1000E used TWO reset trees*



Test System

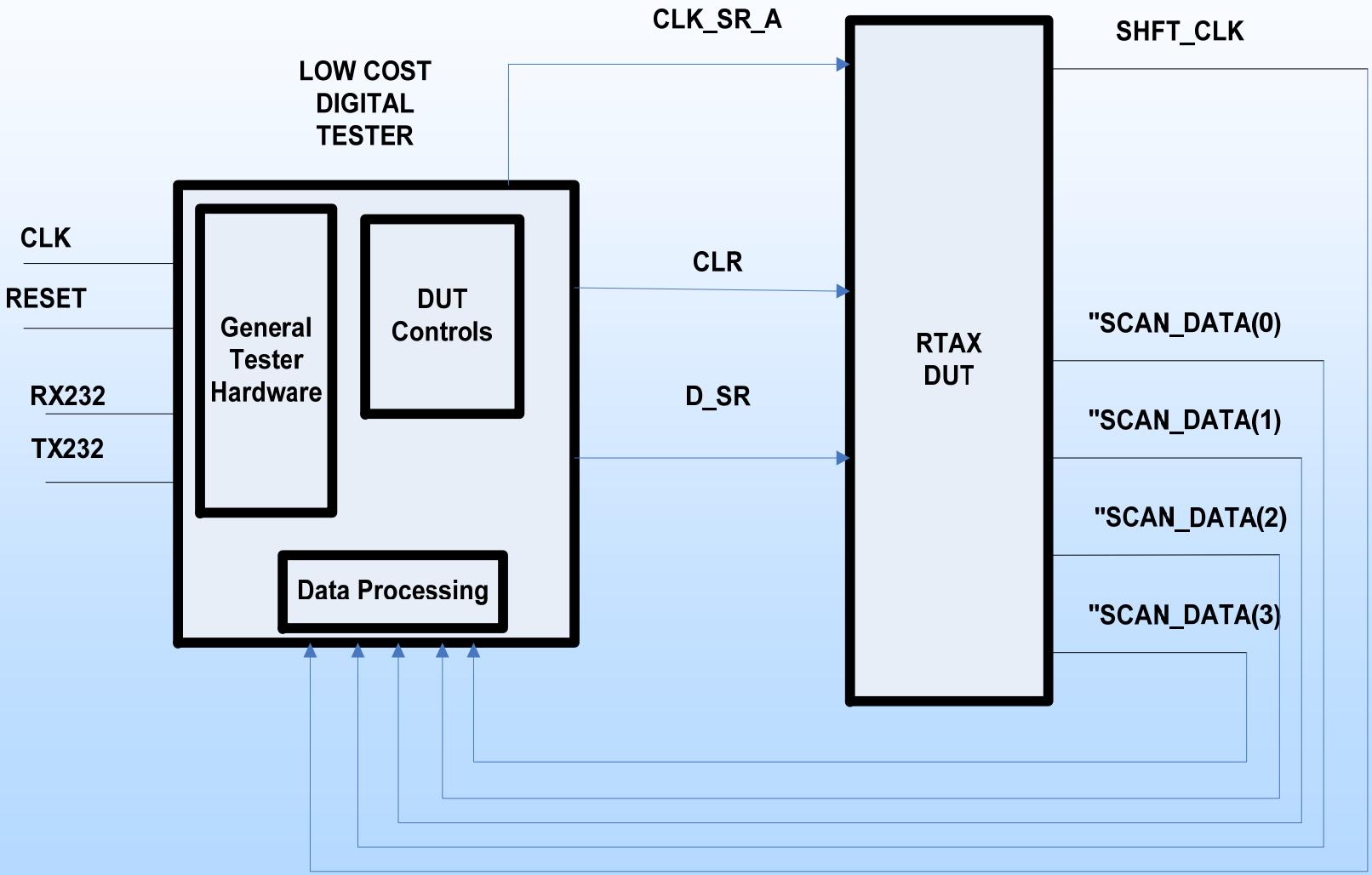
- The DUT (RTAX-S) controller/processor is instantiated as a subcomponent within the Low Cost Digital Tester (LCDT).
  - Developed by the NASA Goddard Radiation Effects and Analysis Group.
- LCDT consists of:
  - A Mother Board (FPGA Based Controller/Processor – Xilinx Spartan III) and
  - A daughter board (containing DUT and its associated necessary circuitry).
- The socket within the DUT Daughter board can accommodate the RTAX1000S and RTAX2000S devices.
- The objectives of this DUT Controller/processor are
  - To supply inputs to the RTAX-S ACTEL DUT and perform data processing on the DUT outputs, and,
  - Interface to the host PC where data is stored and preliminary analysis is performed.
- All tests were performed at
  - Test Temperature: Room Temperature
  - Operating Frequency: 15 MHZ to 150MHZ
  - Vdd: 3.3v I/O and 1.5V Core

LCDT Board



SEE Test Results of ACTEL RTAX-S presented by Ken Label, May 10th, 2006

The LCDT Connection to the RTAX DUT



Test Facility – Heavy Ion

- **Facility:**
  - **Texas A&M University (TAMU) Cyclotron Single Event Effects Test Facility, 15 MeV/amu tune).**
- **Flux:**
  - **1.0×10^4 to 2.0×10^5 particles/cm^2/s**
- **Fluence:**
  - **All tests were run to 1×10^7 p/cm^2 or until destructive or functional events occurred.**
- **Linear Energy Transfers (LET) :**
  - **8.5 to 74.5 MeV*cm^2/mg**

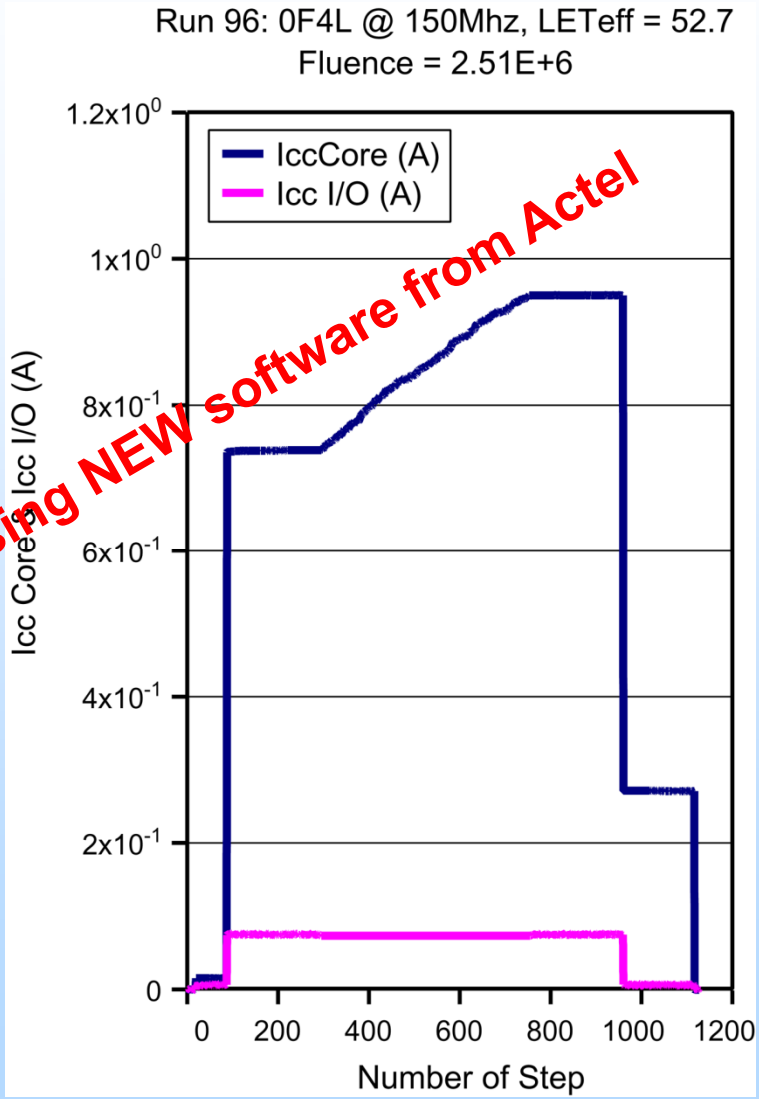
Heavy Ion Results

- Previous Results
- Frequency Response
- Date Pattern Dependence
- Architectural Effects
- Cross Section vs. LET
- BER
- Architectural and Frequency Effects
- Data Pattern Effects
- Bursts
- 1000E Architecture Analysis
- Single Event Latchup (SEL)

Previously Presented Results: Increase in Core Current

- **Non-traditional SEU effects noted**
  - **Current increases noted with number of particles used for irradiation in every test run**
    - **Soft reset and power cycle cleared**
  - **Consistent with Actel data sets**
  - **See Actel's presentation in this Briefing for detailed discussion of data, root cause (back end software), and fix.**

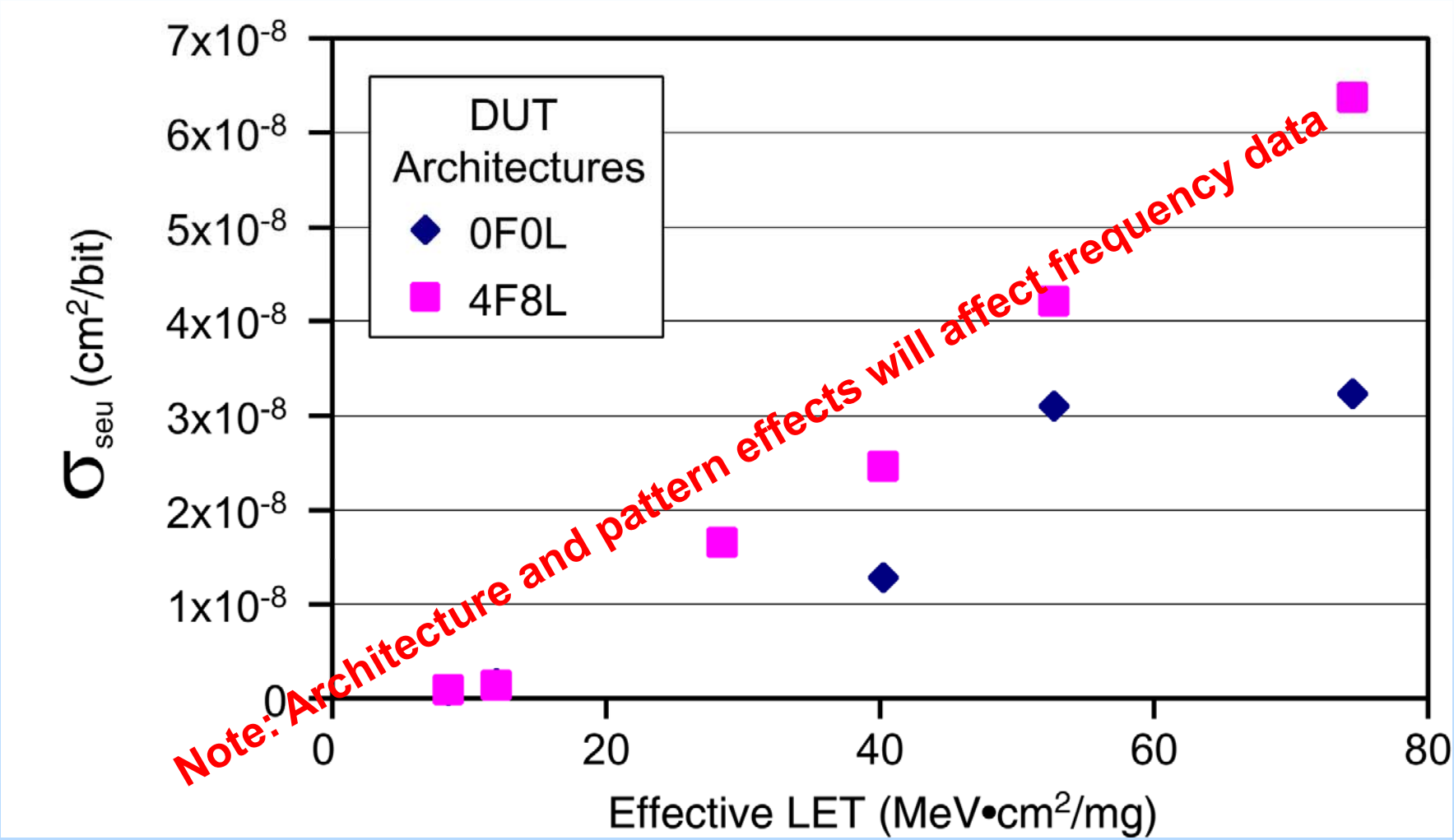
This issue has been eliminated using NEW software from Actel



Sample Current Increase During Test Run

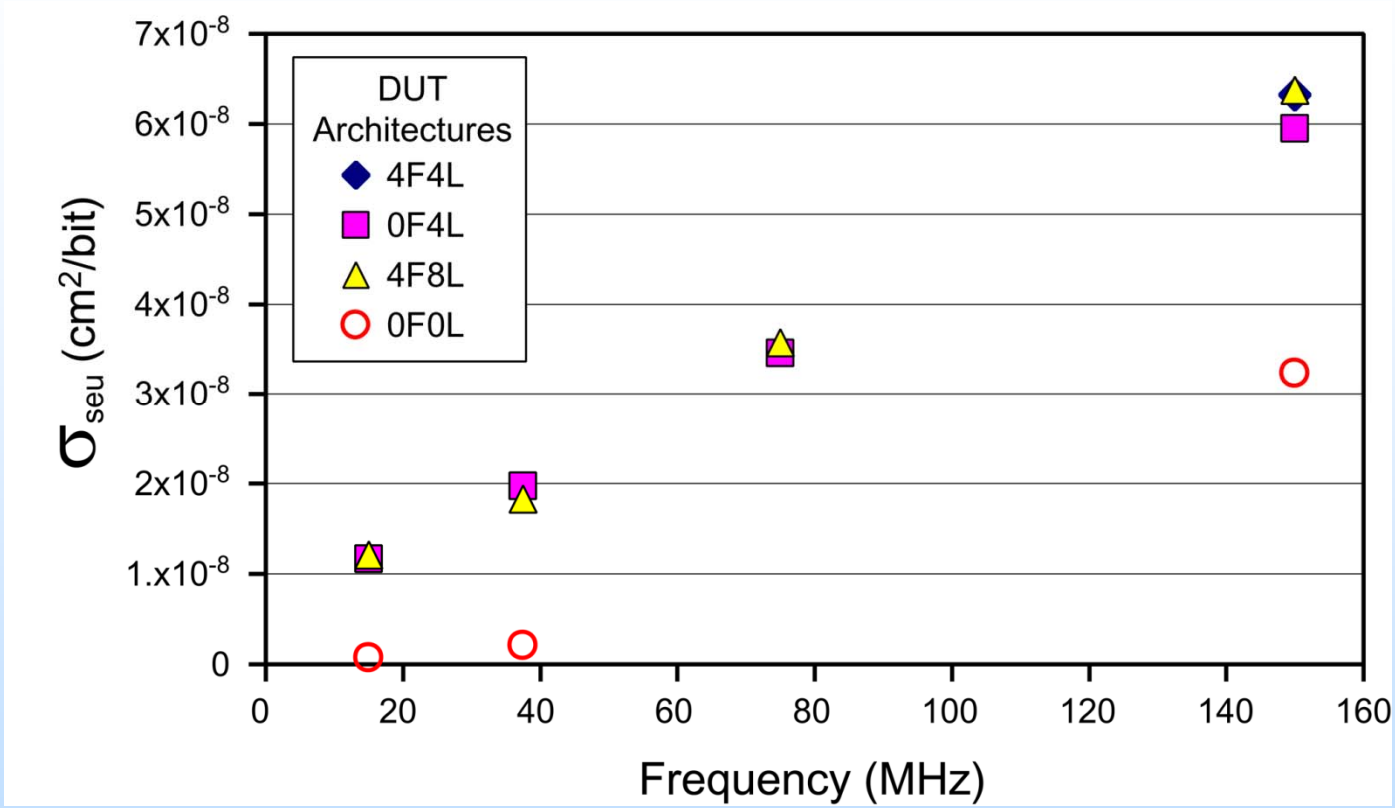
Effective LET vs Cross Section: Two Separate Architectures

freq = 150 MHz, data pattern = checkerboard



Frequency vs. Cross Section:

*LET = 74.5 MeV*cm²/mg, data pattern = checkerboard, multiple DUT architectures*



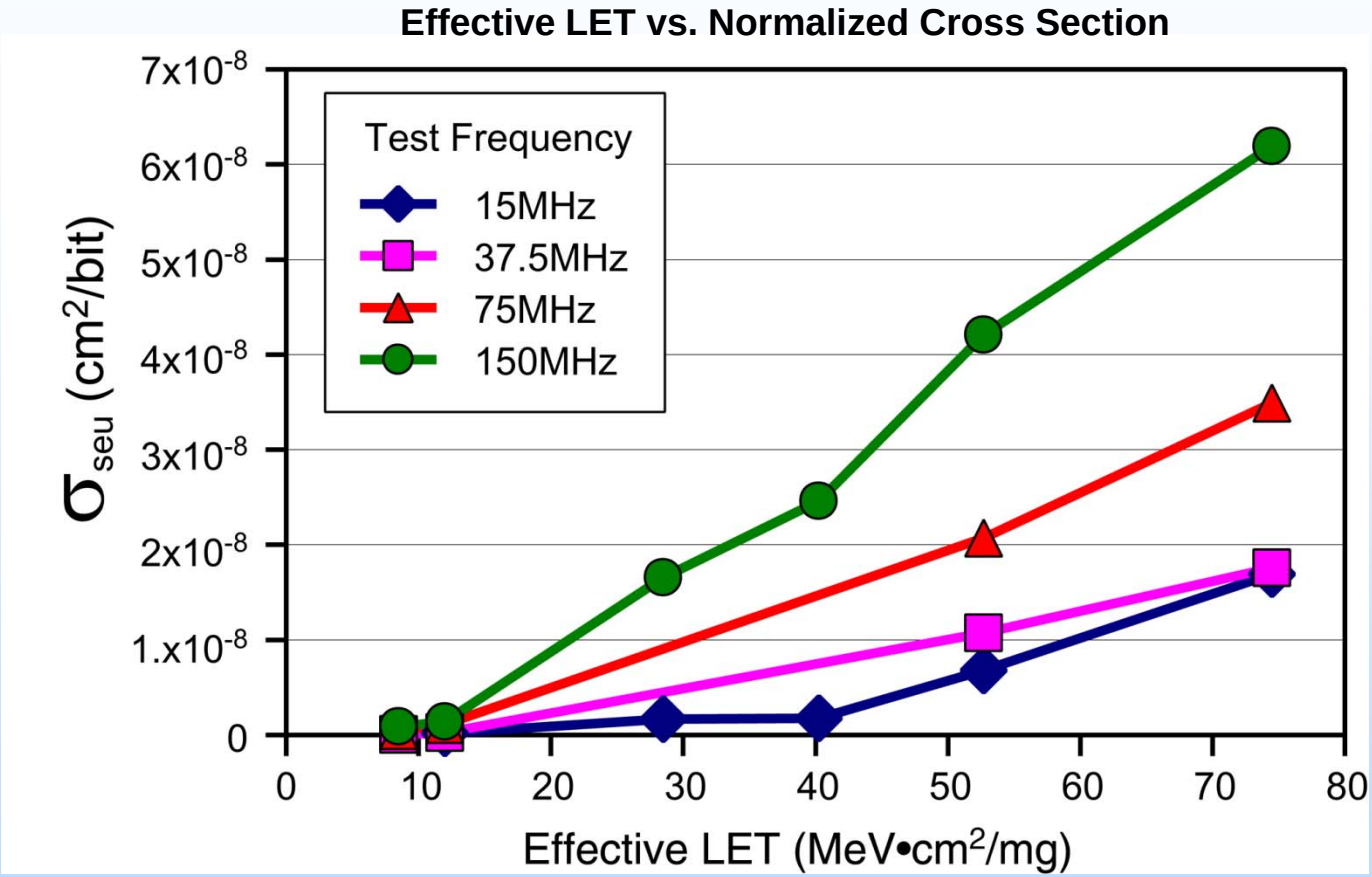
Cross-section scales with speed and combinatorial logic

Error cross section increases ~ linearly with the Frequency

- **There exists ~two orders of magnitude of difference between the 15 MHZ-0F0L point and the 150MHZ-4F4L point**
- **Note relationship with DUT architecture**

LET vs. Cross Section:

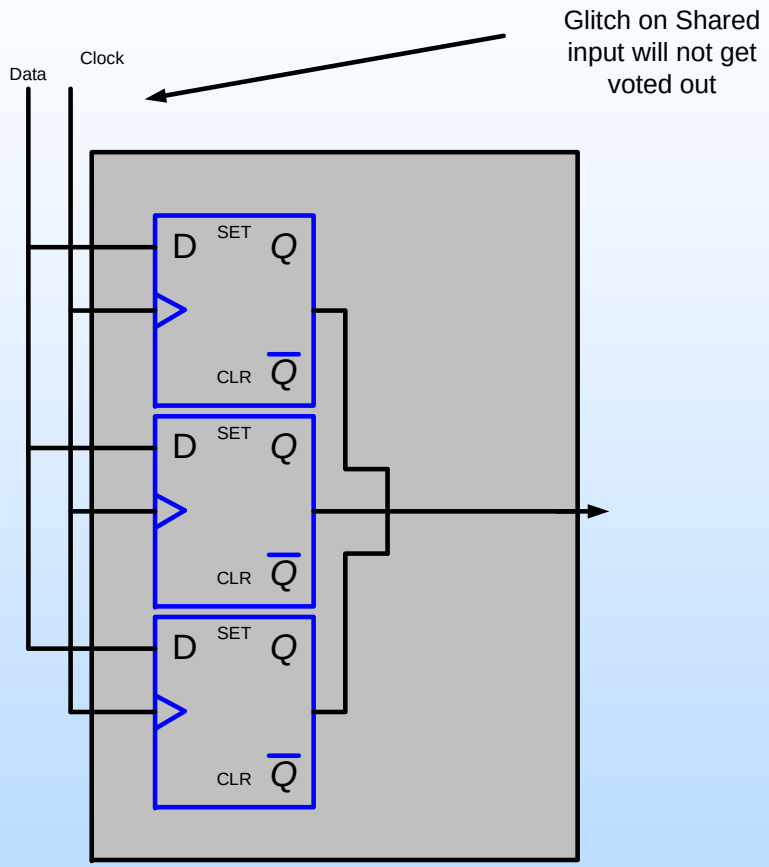
multiple frequencies, data pattern = checkerboard, 4F8L architecture



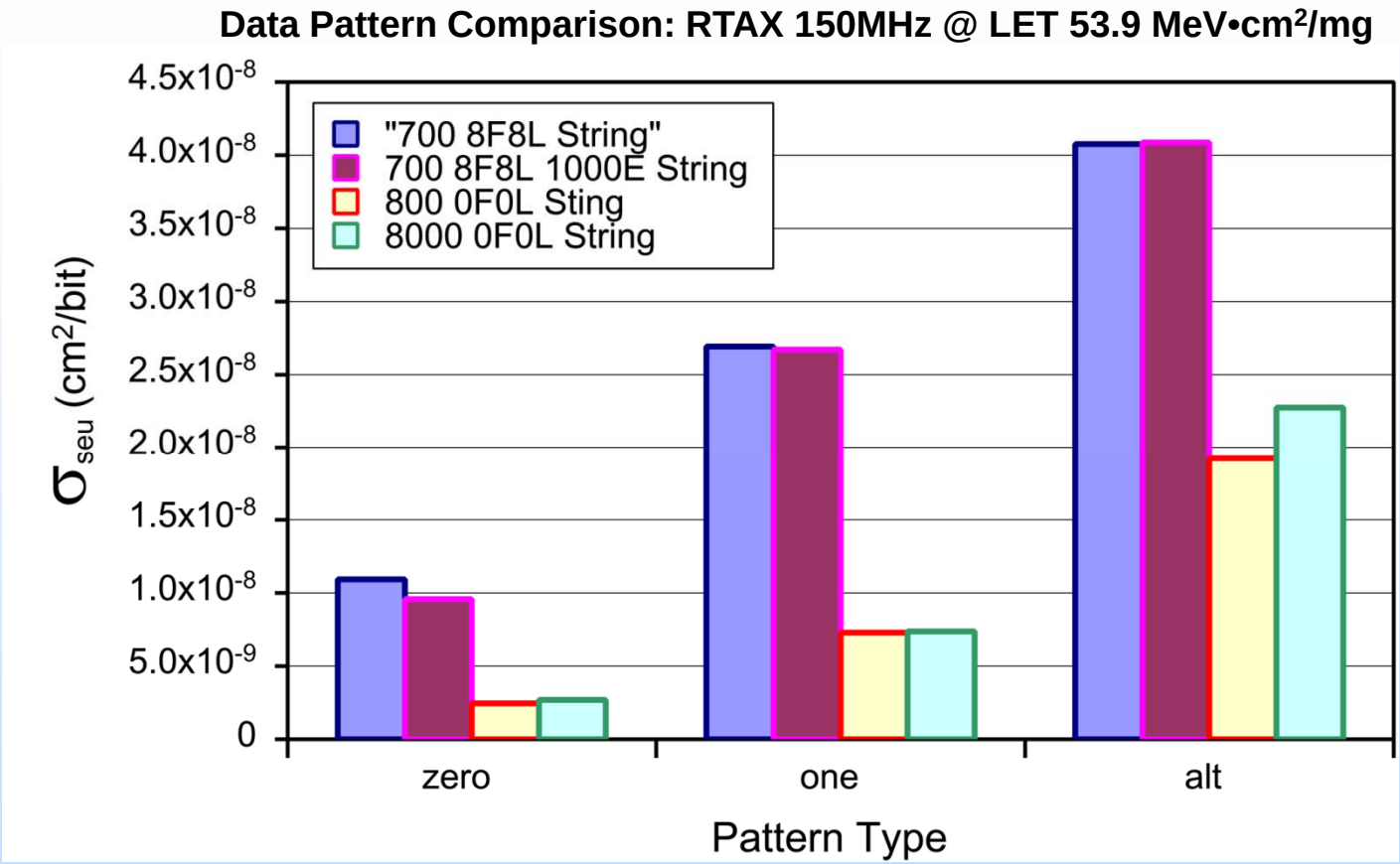
- **Frequency Differentiation after LET_{th}**
- **Extremely low cross section at 15MHZ for LET < 40Mev*cm^2/mg**

Analysis of Architectural Issue: SEU and SET Sensitivity

- **SEU sensitivity increases with increased use of combinatorial logic**
  - **Single event transients (SETs) propagate**
  - **The probability of capturing a transient within an RCELL increases with frequency**
  - **Affects cross-section and LET_{th}**

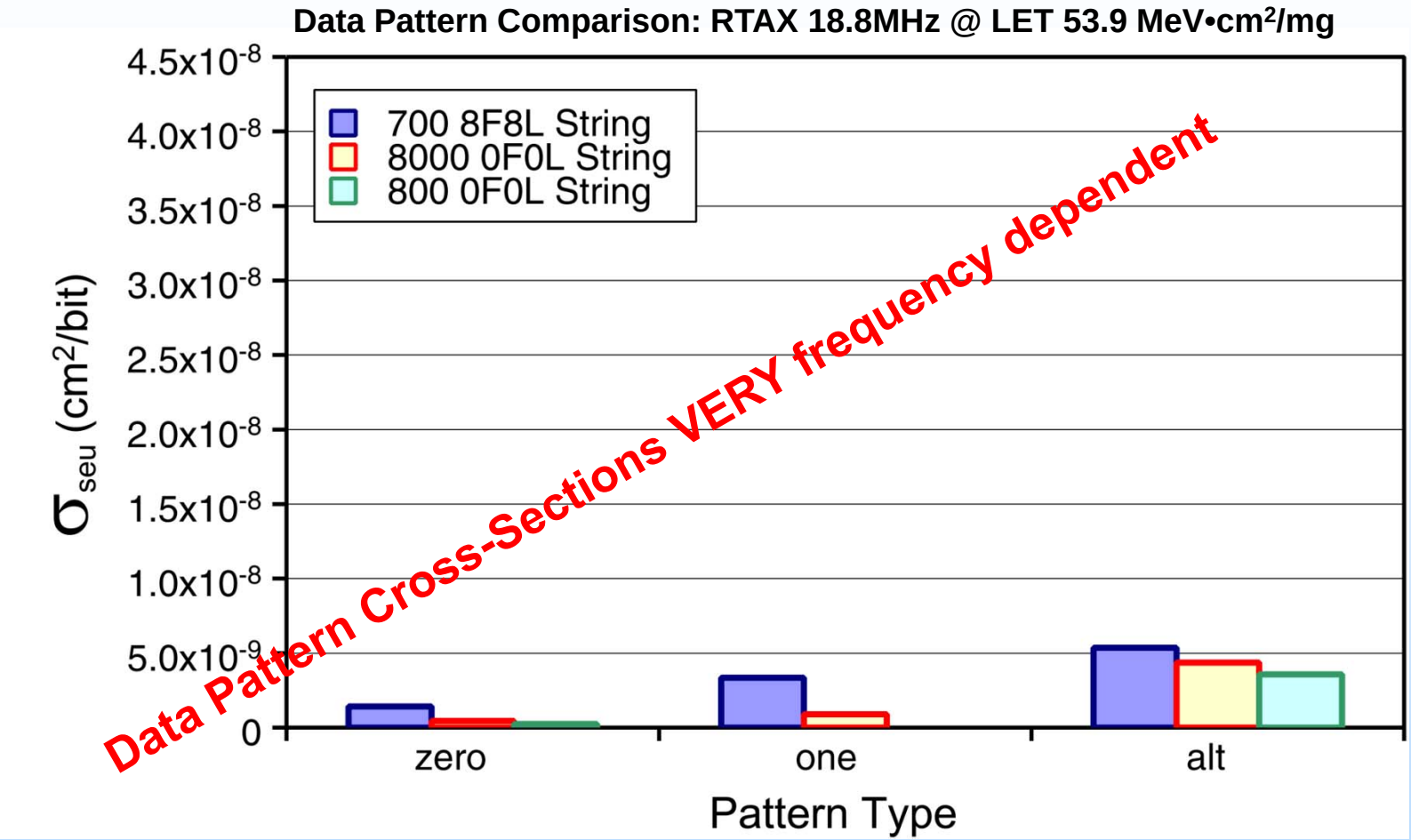


Data Pattern Effects @ 150 MHZ



- **8F8L and 0F0L strings are consistent with each other**
  - **2X sensitivity shift between these two strings**
- **Data pattern variance shows up to an order of magnitude difference in cross section from "zero" data pattern to "checkerboard" pattern**

DATA Pattern Effects @ 18.75 MHZ



- **Data pattern effects less significant at slower speed**

Heavy Ion Test Results: Burst Error

- Burst Errors appear as multiple near-continuous errors within a string
- Data Capture
  - Because of the synchronous nature of the tester in respect to the DUT, it is possible to capture, and analyze data every clock cycle (even at its highest speed – 150MHZ).
  - Every fault is time stamped and a burst counter is incremented if there is a fault in the following clock cycle
- Observed Burst Responses
  - Most Bursts appeared to be reset oriented (long strings of “0” patterns)
    - Not always the same length
    - No reset was needed – this was a self- recoverable fault
  - Loss of I/O did occur –
    - Can only be recovered upon a reset to the FPGA
    - Very rare occurrence

Burst Results - Continued

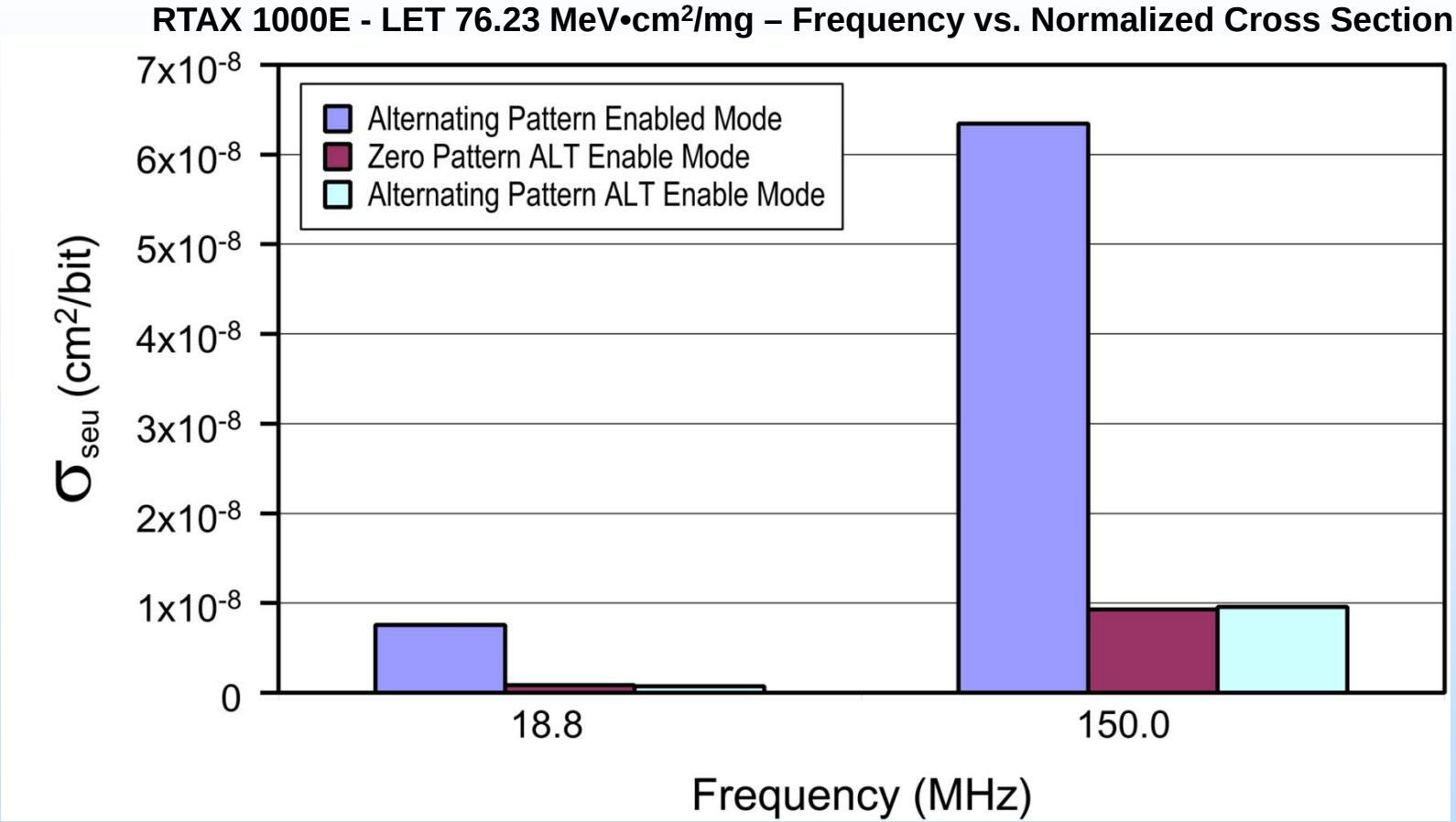
- **2000 Series**
  - **Bursts only occur at >= 75MHZ**
  - **150MHZ dramatic increase**
  - **No bursts at < 53 LET MeV*cm^2/mg**
  - **For the longer chains – Burst lengths were not the entire length of the chain**
- **1000 Series**
  - **No Bursts observed even at highest tested frequency and LET**
    - **Note: Shorter reset tree**

1000E Special String: Analysis of Alternating DFF Enable

- **Why?**
  - **Tests Enable frequency effects**
    - **Test modes: alternating enable vs. always enabled**
- **All outputs were in double bursts (2 SHFT_CLK cycles in a row) of either “1000” and “0010” or “0100” and “0001” patterns.**
- **Such patterns suggests (and is expected):**
  - **The enable line is active every other cycle – it takes the fault 8 cycles to get through the window**

1000E Analysis – Unexpected Results,

*LET = 76.23 MeV*cm²/mg, architecture = 8F8L*

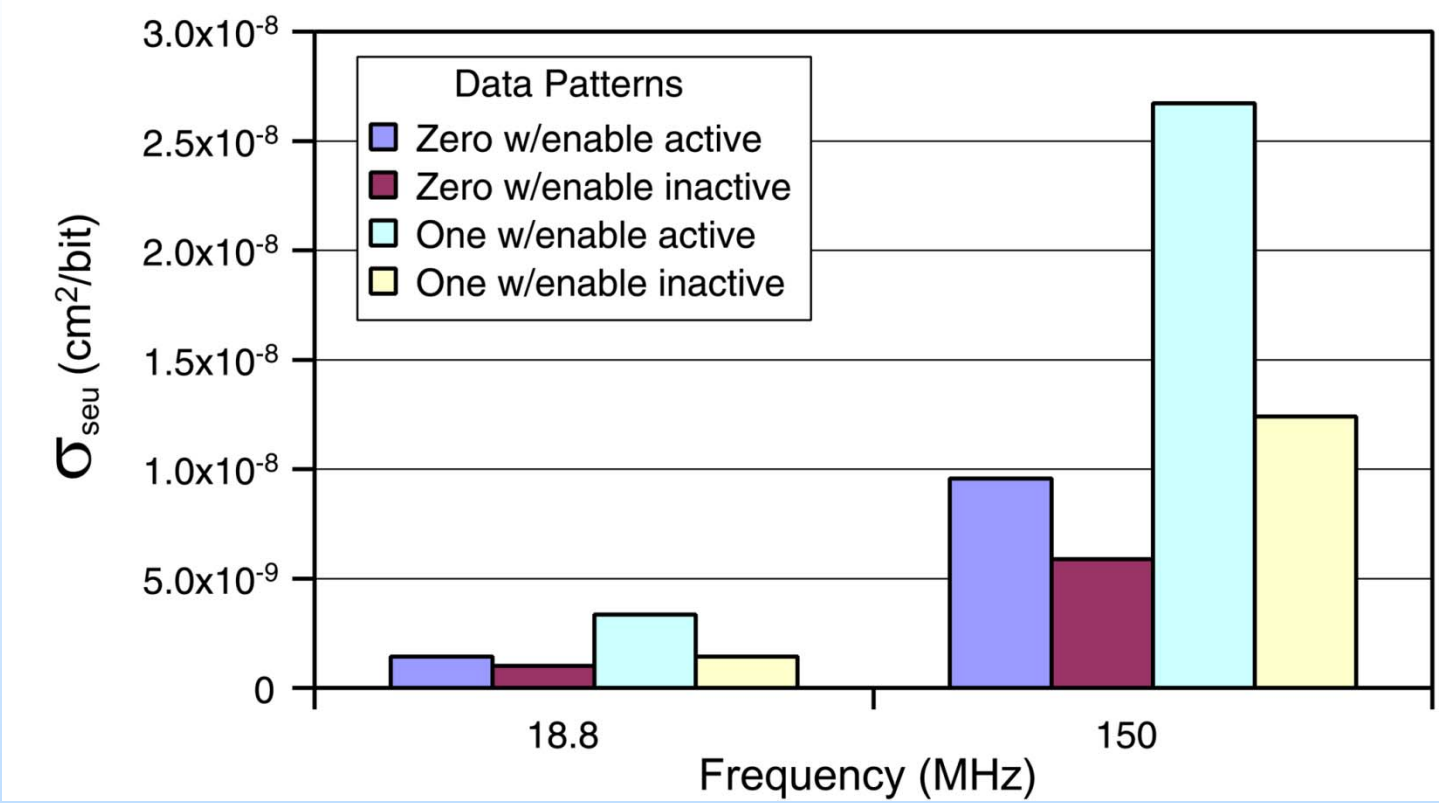


- **Data = Checkerboard Pattern**
  - **Enable always active vs. alternating enable (every other cycle): 7X difference)**
- **With alternating enable**
  - **Checkerboard Pattern and zero pattern (with checkerboard enable) are almost equal in cross section.**

1000E Analysis

*LET = 53.9Mev*cm²/mg, architecture = 8F8L*

RTAX 1000E - LET 53.9 MeV•cm²/mg – Frequency vs. Normalized Cross Section



- **Zero vs. One Data Patterns with active enables and checkerboard active enables**
  - **Both patterns show an expected 2x (approximate) difference between enable modes**

SEL Results

- No SEL was observed at room temperature and nominal power supply voltage
- Concludes that that the RTAXS series is SEL immune for LET < 75 MeV*cm^2/mg under these conditions
  - Actel data has been taken at high temp and worst-case Vdd showing no SEL

Test Facilities - Proton

- **Facility:**
  - **Crocker Nuclear Laboratory (CNL) at the University of California at Davis (UCD)**
- **Flux:**
  - **1.0E09 particles/cm^2/s**
- **Fluence:**
  - **All tests were run to 7.14E^{11} p/cm^2**
- **Energy :**
  - **63 MeV-incident**

- **Facility:**
  - **Indiana University Cyclotron Facility (IUCF)**
- **Flux:**
  - **3.0E9 particles/cm^2/s**
- **Fluence:**
  - **All tests were run to 1.0E12 p/cm^2**
- **Energy :**
  - **195 MeV - incident**

Proton Test Results

- Limited tests performed (lack of samples and time)
  - 0F0L at 15 MHz (best case)
  - 4F8L at 150 MHz (worst case)
- Proton dose levels (63 MeV protons) of 100 to 200 krads(Si) per device
  - No SEUs observed at 15 MHz for any string
  - Few SEUs observed at worst case 150 MHz
    - SEU Cross-section of 6.65E-16 cm^2 per device for 4F4L
    - SEU Cross-section of 3.5E-15 cm^2 per device for 4F8L
      - Roughly an order of magnitude confidence level on results (low statistics)
    - No SEUs observed on other DUT strings at 150 MHz
- Proton dose levels (195 MeV protons) of 300 krads(Si) per device
  - No SEUs observed at 18.75 MHz for any string
  - Few SEUs observed at worst case 150 MHz
    - SEU Cross-section of 8.5E-16 cm^2 per device for 8F0L
    - SEU Cross-section of 2.8E-16 cm^2 per device for 8F8L

Calculated SEU Rates – CREME96

SEU rates at worst-case GEO In errors/bit-day

Actel Data Sheet per R-Cell	NASA – 15 MHz, no combinatorial	NASA – 150 MHz, max combinatorial
<4E-11	<5E-9	<5E-8

RTSX-SU devices were also tested:

similar results for increase in error rates with speed

Summary

- **RTAX-S SEE Data Shows:**
  - **Frequency Variation**
  - **Data pattern Variation**
  - **Architectural Variation**
- **No SEL was observed during these tests**
- **Small sensitivity observed to protons.**
- **It is important to make sure that the observed effects above are taken into consideration when performing SEE rate predictions for a mission**

1000E Architecture Resets

- Reset is connected to the each DFF reset as in all other architectures
- Extra reset is connected to the DFF that controls enable fan out. It is also connected to an input pad for tester control
- Test sets are tested under to major conditions controlled by the tester:
  - DFF enable turned off (enable reset is active)
  - DFF enable is turned on (enable reset is inactive)