Radiation Testing on State-of-the-Art CMOS: Challenges, Plans, and Preliminary Results

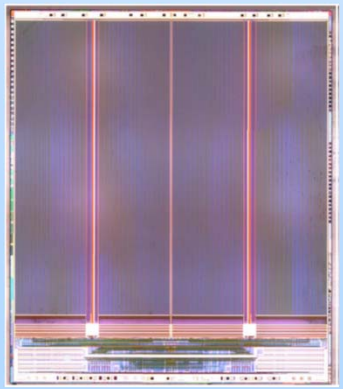
Kenneth A. LaBel
ken.label@nasa.gov

Lewis M. Cohn
lewis.cohn@nrl.navy.mil

This work was sponsored in part by the NASA Electronic Parts and Packaging (NEPP) Program and the Defense Threat Reduction Agency under IACRO #08-43-43I and 09-4587I

Abstract

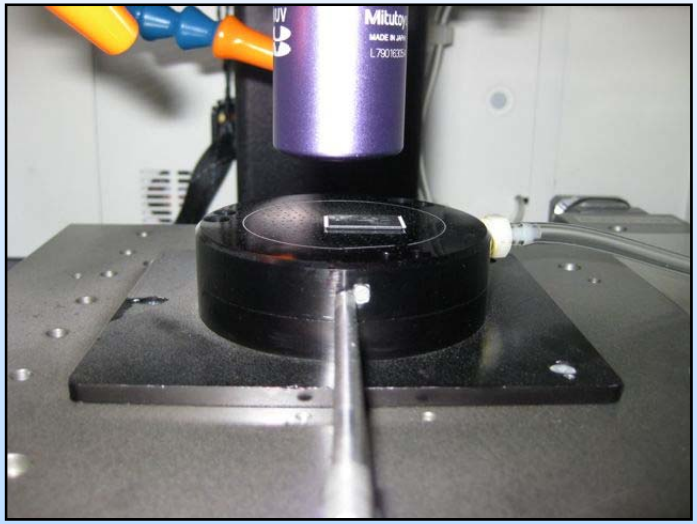
- **At GOMAC 2007 and 2008, we discussed a variety of challenges for radiation testing of modern semiconductor devices and technologies**
- **In this presentation, we provide more specific details in this on-going investigation focusing on out-of-the-box lessons observed for providing radiation effects assurances as well as preliminary test results.**



FLASH memory is often near the leading edge of CMOS

Outline

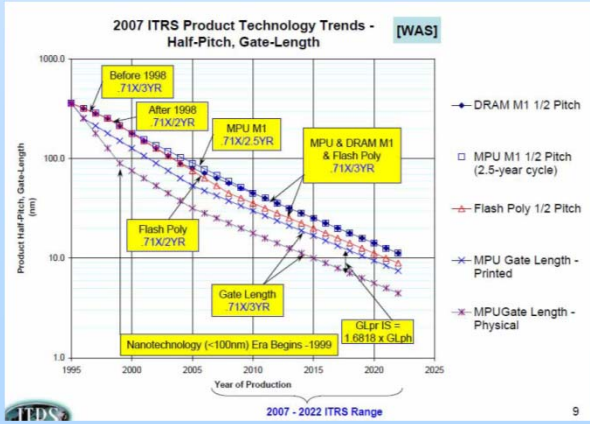
- **What issues are at stake?**
  - **What devices are we discussing?**
- **Radiation Test Plans and Results**
  - **Overall plan**
  - **Recent results**
  - **Near-term plans**
- **Radiation Test Methods**
  - **Techniques and considerations**
- **Summary**



Use of a cold LASER for device test preparation

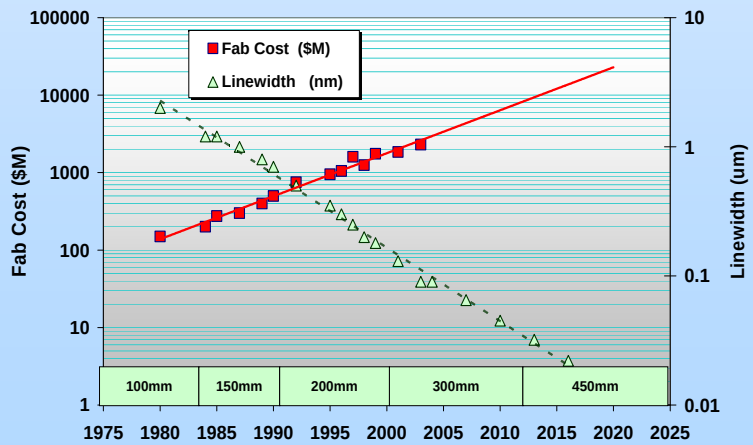
Issues

- **The radiation effects being discussed are**
  - **Total Ionizing Dose (TID) - a long-term cumulative degradation effect, and,**
  - **Single Event Effects (SEE) – impacts that occur from a single energetic particle as it deposits energy in a device**
- **For simplicity, we can characterize the challenges for <100nm CMOS in three ways:**
  - **Geometric: transistors are reduced in size and many more are available in the same form factor,**
  - **Temporal: operating speeds are getting faster and transient pulses may have increased impact, and,**
  - **Complexity: devices are now SYSTEMS in terms of functions and IP**



Geometric

- **As transistor physical volume and spacing between transistors shrinks**
  - **A single energetic ion becomes INCREASINGLY likely to affect multiple transistors**
    - ***This is the single event multiple upset (SEMU) of Multi-Cell/Bit Upset (MCU or MBU) issue***
    - **This is exceedingly important for**
      - **Design hardening options**
      - **Error detection and correction (EDAC) schemes**
      - **Space SEU rate predictions**
- **In addition, as size has scaled, power supply voltages have been reduced as well**
  - **Implies that less deposited energy may be required to cause an SEU**
    - **That is: increased SEU rates are possible**



Temporal

- **Consider a particle depositing energy in a transistor**
  - **This charge may cause a transient pulse**
  - **The energy deposition is on the picosecond timeframe, but pulse size varies with the circuit**
  - **Whether a circuit responds to the pulse is a function of circuit bandwidth**
    - **The faster the operating the speed of a device, the more sensitive it becomes to these pulses**
      - **More Single Event Transients (SETs) propagate to circuit effects in newer faster devices and may corrupt multiple clock cycles**
- **It has been demonstrated that in fast CMOS devices, SETs may be equally or more invasive than the traditional SEU.**

Complexity

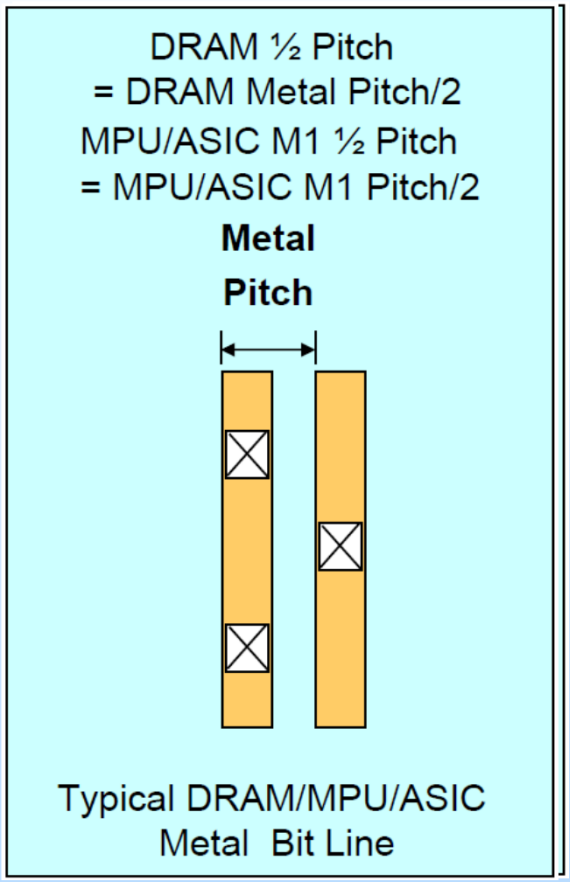
- **Scaling has allowed a myriad of functions to be embedded in a single chip**
  - **Consider a field programmable gate array (FPGA) which may have**
    - **Processors**
    - **DSPs**
    - **Gbit I/O**
    - **Programmable logic strings**
    - **Memory arrays, and so on**
- ***As we have presented in the past year's GOMAC, complete radiation testing of a device as well as a interpretation of results have become increasingly difficult!***
  - **Working with the manufacturer is often the best way to perform full parametric and functional tests**

CMOS Devices of Interest

- **There is a wide variety of device types to consider**
  - **Custom**
    - **ASICs**
    - **Partially custom like FPGAs or structured ASICs**
  - **Processors**
  - **Memories**
    - **Volatile and non-volatile**
  - **Logic**
  - **And even mixed signal**
- **We will discuss some of the work being performed on test structures as well as commercially available devices.**

Goals of This Work

- **Investigate new and emerging electronics technologies to aid**
  - **Identification of failure modes for**
    - **Hardening approaches**
    - **Test requirements**
    - **Performance predictions**
  - **Validation of RHBD designs**
  - **Suitability of electronics technologies for space utilization**
- **Support and/or validate test methods**
  - **RHA**



Radiation Test Plans/Status - Partial

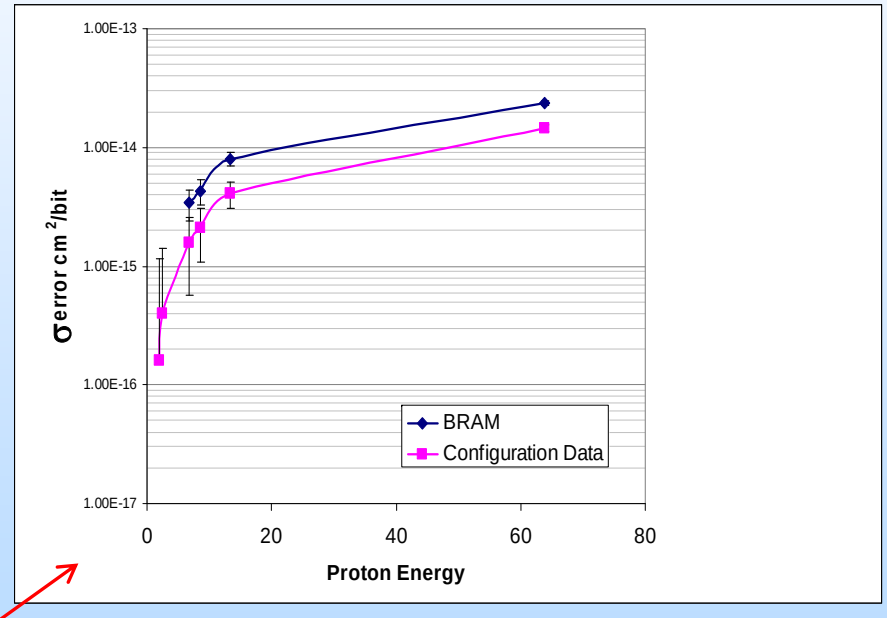
	90 nm	65 nm	45 nm	Notes
IBM		SOI and bulk SRAMs evaluated for SEE (proton and heavy ion)	SOI SRAMS received and 1st series of tests performed	Collaboration with IBM and Sandia; Seeking structures for temporal SEE testing. 32 nm samples in the offing.
Texas Instruments	TID on transistors completed (90 and 130 nm)	SEU/SEL on SRAMs completed; Preparation for TID testing of transistors underway	SRAM Test Structures delivered and test development underway; Vanderbilt designing new test structures	Collaboration with TI and Vanderbilt; Experiments also performed at temperature
SIRF Program	TID on transistors completed	TID on transistors completed		Courtesy of Xilinx and AFRL; Experiments also performed with temperature
Intel		TID and dose rate completed	1st hi-K commercial device. TID and dose rate planned. Functional TID tests completed. Parametric TID tests completed (report being drafted)	Collaboration with Intel and NSWC

Additional discussions underway with eASIC and Freescale.

Support for RHBD efforts from DTRA/DARPA and AFRL

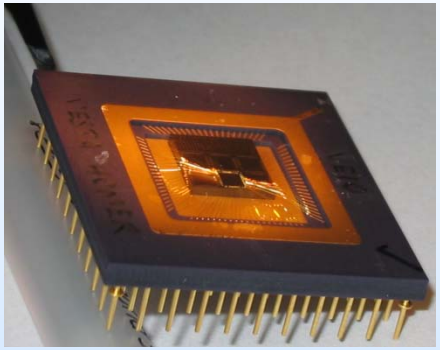
Highlights of Work So Far

- **Among the Firsts**
  - **Test of a commercial hi-K device**
  - **SEU test of 45 nm SOI**
  - **Direct SEU comparison of 65nm bulk and SOI**
    - **Observation of possible proton direct ionization**
    - **Observation of enhanced sensitivity with low energy protons**
  - **Combined radiation and reliability on sub 90 nm flash**
  - **Use of Two-Photon Absorption (TPA) Laser for comparing cell (SEU) versus logic (SEFI) in commercial SDRAMs**
  - **Test of a commercial FPGA for low proton energy sensitivity**
    - **New method development**

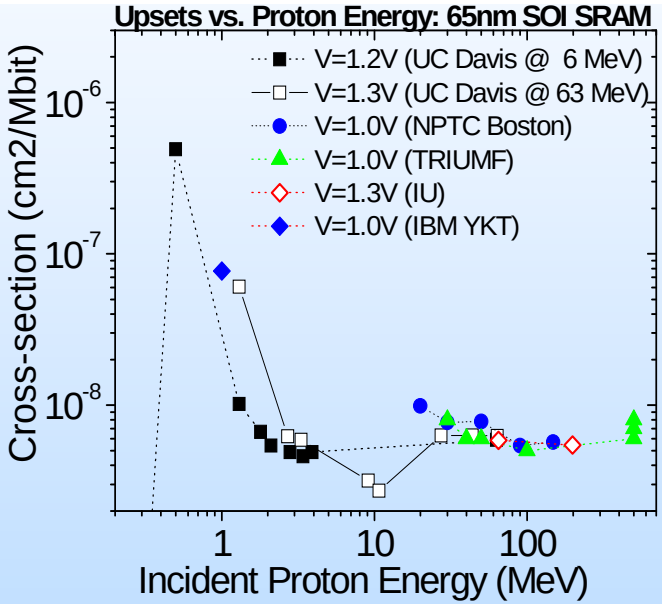


IBM 65nm SOI Results

Photo of 1Mbit 65nm SOI SRAM used for "front-side" testing



Data from 1 – 500 MeV @ normal incidence



Ratio of upsets from direct ionization vs. collision events

Shielding	SEU Ratio : Direct Ionization/Collision
50 mils	20 X
100 mils	10 X
200 mils	6 X
500 mils	3 X

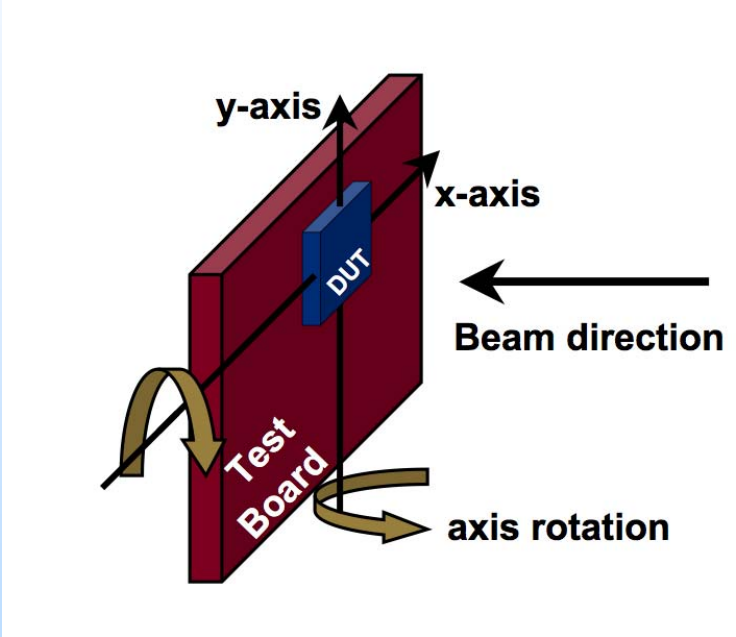
MBU and angular analyses are still being performed.

Data taken from Heidel, et al, IEEE NSREC 2008

Preliminary 45nm data will be shown at SEE Symposium and IEEE NSREC

TI CMOS Status

- **Accomplishments**
  - ***Demonstrated direct ionization upset due to protons with energy < 2 MeV***
  - ***1st test of MBU effects using goniometer set-up for solid angle coverage***
    - **Successful MBU and SEL tests for various orientations of 65 nm SRAMs**
  - **Validated pulsed I-V TID tests with comparison to DC I-V measurements for 90 nm transistors**
- **Current status**
  - **Work being extended to 45 nm CMOS SRAMs and 65 nm transistors**



Intel Processors

- **TID and dose rate on 65nm bulk CMOS processor were completed in FY08**
  - ***Data may be requested via Intel for government only***
- **45nm Wolfdale processor has been TID irradiated**
  - **Functional tests show > 1 Mrad-Si tolerance**
  - **Results can NOT be inferred as exceeding ITAR levels without parametrics.**
    - ***Testing complete and report being developed***
  - **Dose rate test planned**

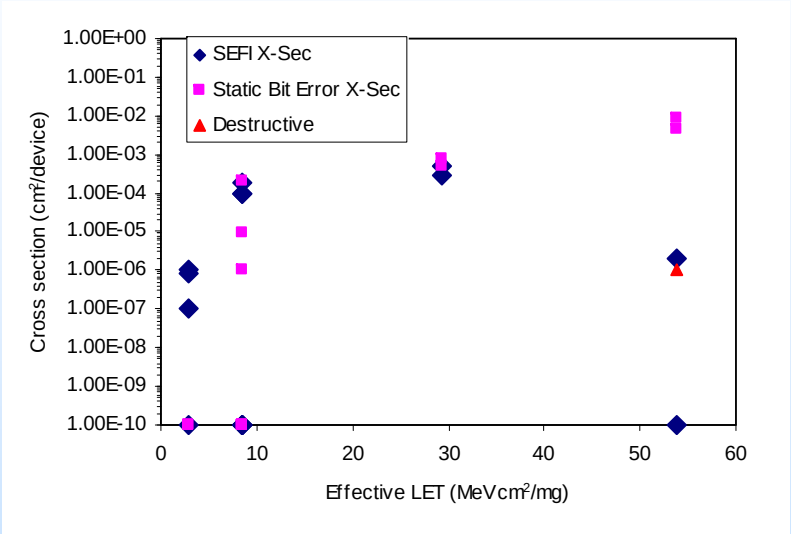
3.0 Ghz, dual-core

First commercially available hi-K device

Intel burn-in board modified for TID bias testing

Flash Memories

- **Results in FY08 show promise for both SEU and TID**
  - **SEU rates**
  - **Low dose rate exposures**
  - **Unbiased TID**
- **Radiation test results**
  - **TID test of Samsung 4G NAND flash**
    - **Passed 100 krad (Si)**
  - **Micron 4G NAND flash**
    - **Passed 100 krad (Si)**
    - **SEE testing showed SEL, high SEFI rate, and extreme angular dependence effects**
- **Preliminary reliability study indicates radiation exposure has only a small effect on flash endurance reliability**

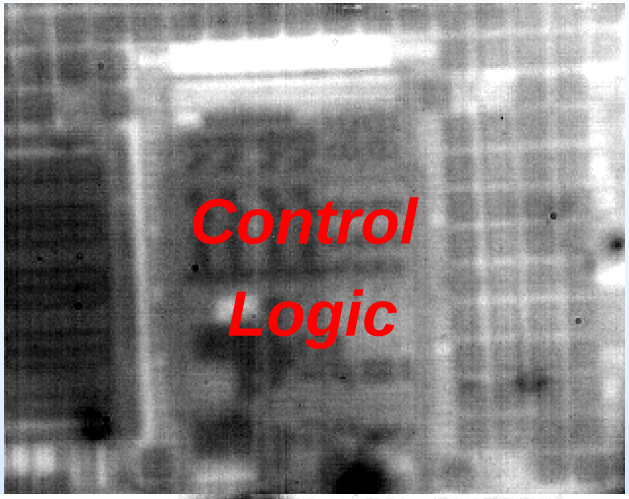


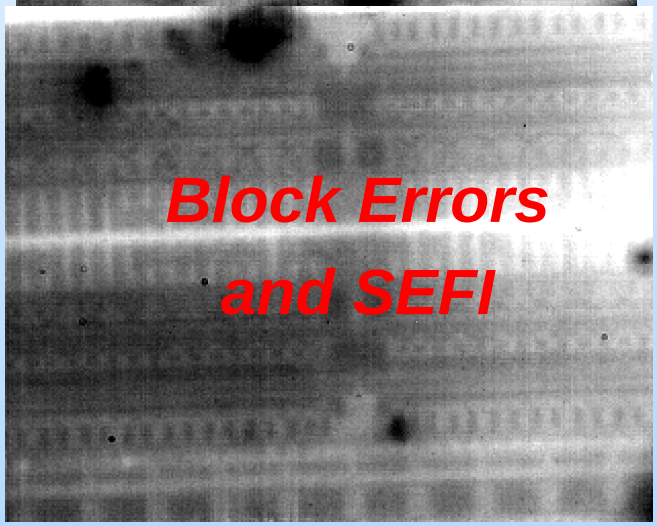
SEL observed on Micron Flash during static mode operation – Failures were destructive

These devices are having improved TID response, but SEE is still a prime concern

Highlights
SDRAMs

- **Elpida SDRAM – Use of TPA to understand failure modes**
  - **Memory cells are harder than logic cells**
    - **Block errors nearly as common as SEUs**
  - **Control logic upsets cause (mostly) correctable block errors**
  - **Some SEFI seen**
    - **Recovery requires reset or power cycle**
- **GSFC results provide context to previous results from J. Benedetto (see NSREC 2008 short course)**





TPA is a powerful technique for failure isolation

Testing with TPA

SDRAMs

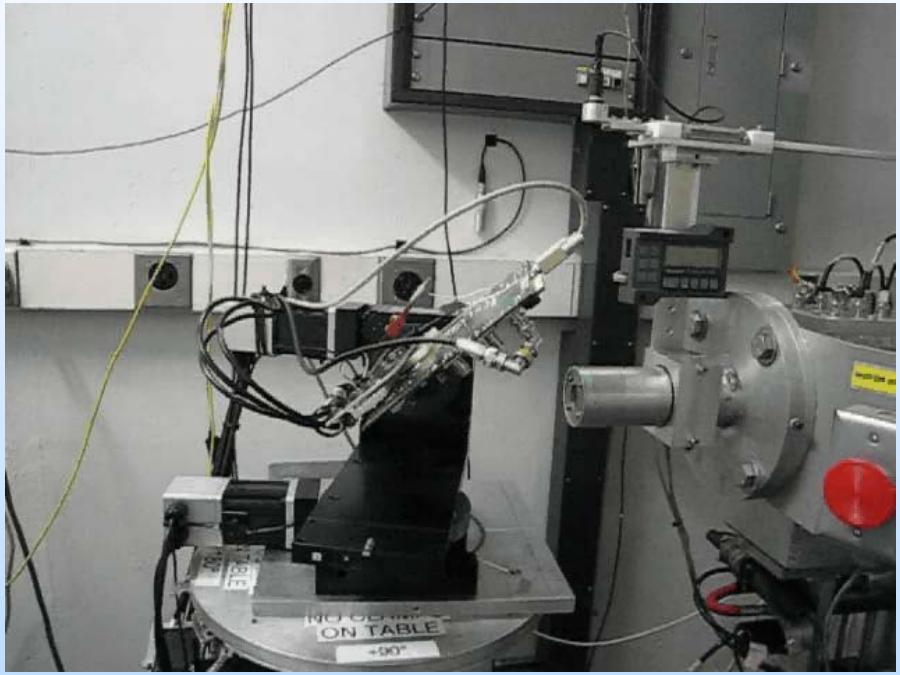
- **TPA Laser Testing**
  - **Allows probing of individual features for SEE susceptibility**
    - **Separates control logic upsets from memory upsets**
    - **Enumerates Error modes**
    - **Packaging and metallization prevent use of top-side, single-photon laser testing for SDRAMs.**
  - **Difficult to estimate charge at sensitive volumes**
    - **Heavy-ion testing needed for quantitative SEE assessment.**
  - **Tests on FPGAs and ADCs planned**

TPA places micron-sized light-pulse on targets with high accuracy.

TPA and HI testing are Complementary

New Test Methods and Validation

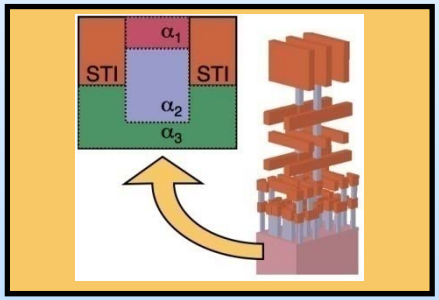
- Conical SEE irradiation
  - Goniometer test system
    - Asymmetric angle coverage
- Development of low proton energy SEU assurance
  - Test structures (SRAMs) and Xilinx FPGA
- Cold LASER Device Preparation
- Laser testing of SDRAMs (w/NRL)
  - Establishment of test procedures
- Dry ice storage (TID)
- Combined TID and SEE performance
- Use of pulsed IV for TID transistor testing
- TID performance at elevated temperature

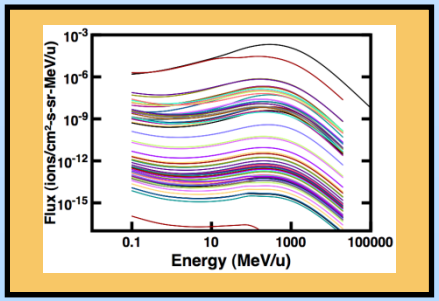


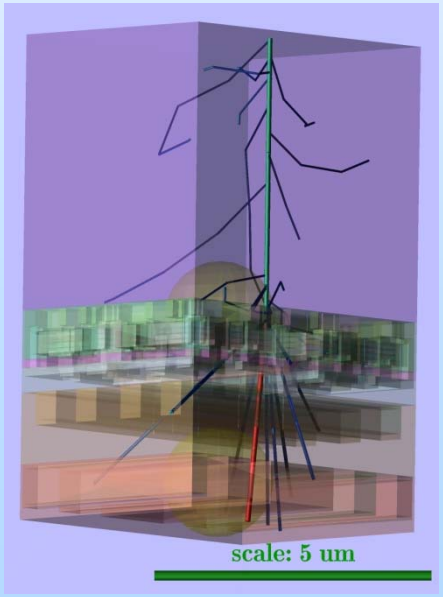
Conical Test System

Radiation Simulation – Vanderbilt and NASA

- **Development of predictive SEE models for space application**
- **Development and validation on bulk CMOS <100 nm and Power MOSFETs**
  - ***New tools for a new technology age!***







Summary

- **In the short time allotted, we have just touched the tip of the iceberg on CMOS and radiation issues**
  - **SEE and TID**
  - **Combined effects (radiation and radiation/reliability)**
  - **Test Methods**
- **The previous charts described some of the efforts supported by the NEPP Program in conjunction with DTRA**
  - ***We have not described the Vanderbilt-led efforts for development of physics-based tools for SEU rate prediction, for example, talk 11.3!***
- **If you are interested in collaboration or for more information, please feel free to contact us or visit the NEPP website at:**

http://nepp.nasa.gov