

A NASA Perspective on Validation and Testing of Design Hardening for the Natural Space Radiation Environment



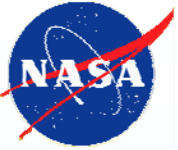
Hubble Space Telescope has utilized a robust system design to conquer radiation challenges

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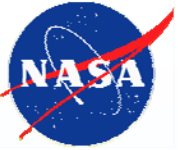
James W. Howard, Jackson and Tull Chartered Engineers,

Martin A. Carts, Raytheon, Christina Seidleck, Raytheon

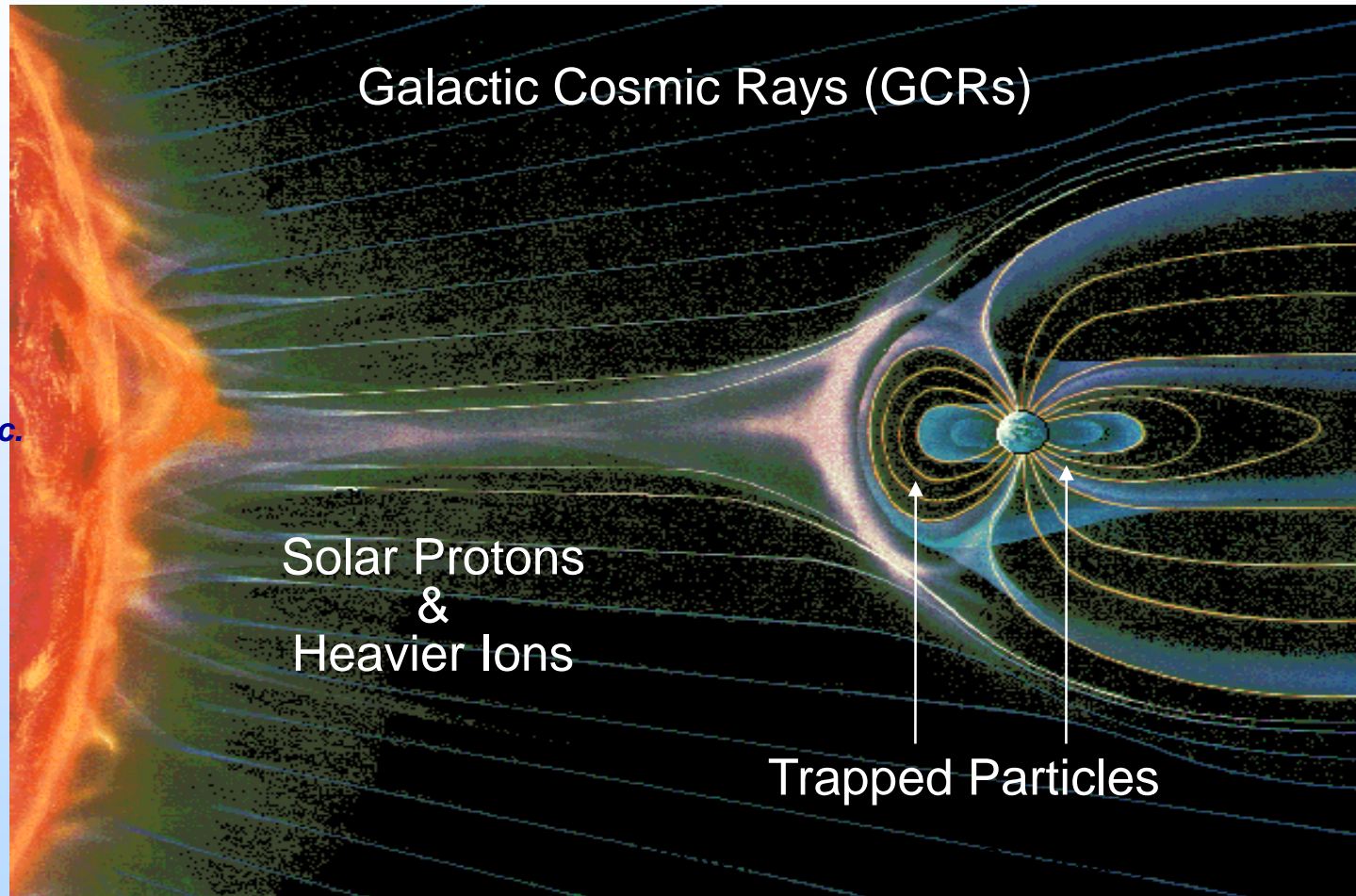


Outline

- **NASA Requirements for Radiation Hardness**
 - **What NASA needs and what environment/effects we care about**
- **Testing HBD devices: Test Considerations**
- **NASA Evaluation Task: Using a Microcontroller as a Test Vehicle**
- **Final Considerations**



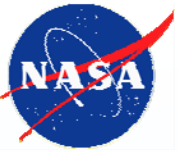
Space Radiation Environment: The Hazard for NASA



*Nikkei Science, Inc.
of Japan,
by K. Endo*

***Deep-space missions may also see: neutrons from background
or radioisotope thermal generators (RTGs);
Avionics may observe GCRs/neutrons at altitude***

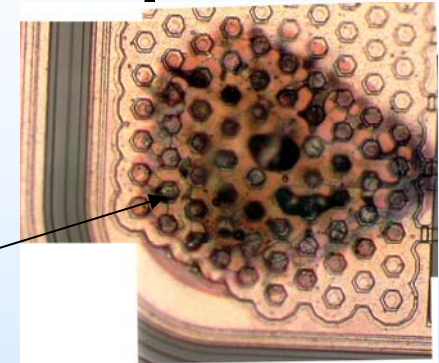
Presentation at GOMAC 2003 – Tampa, FL – Kenneth A. LaBel – Apr 2, 2003

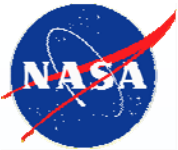


Space Radiation Effects

- **Critical areas for design in the natural space radiation environment**
 - **Long-term effects**
 - Total ionizing dose (TID)
 - Displacement damage (DD)
 - **Transient or single particle effects (Single event effects or SEE)**
 - Soft or hard errors
- **Mission requirements and philosophies vary to ensure mission performance**
 - ***What works for a shuttle mission may not apply to a deep-space mission***

*Destructive SEE
in a COTS 120V
DC-DC Converter*





Radiation Device Regimes for the Natural Space Environment

• High

- > 100 krads (Si)
- May have
 - long mission duration
 - intense single event environment
 - intense displacement damage environment

Examples:
Europa, GTO, MEO
Type of device:
Rad hard (RH)

• Moderate

- 10-100 krads (Si)
- May have
 - medium mission duration
 - intense single event environment
 - moderate displacement damage environment

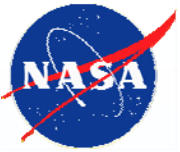
Examples:
Polar, highLEO, L1, L2, ISSA
Type of device needed:
Rad tolerant (RT)

• Low

- < 10 krads (Si)
- May have
 - short mission duration
 - moderate single event environment
 - low displacement damage environment

Examples:
Hubble Space Telescope,
Shuttle, LEO (low-inclination)
Type of device needed:
Commercial with
SEE mitigation

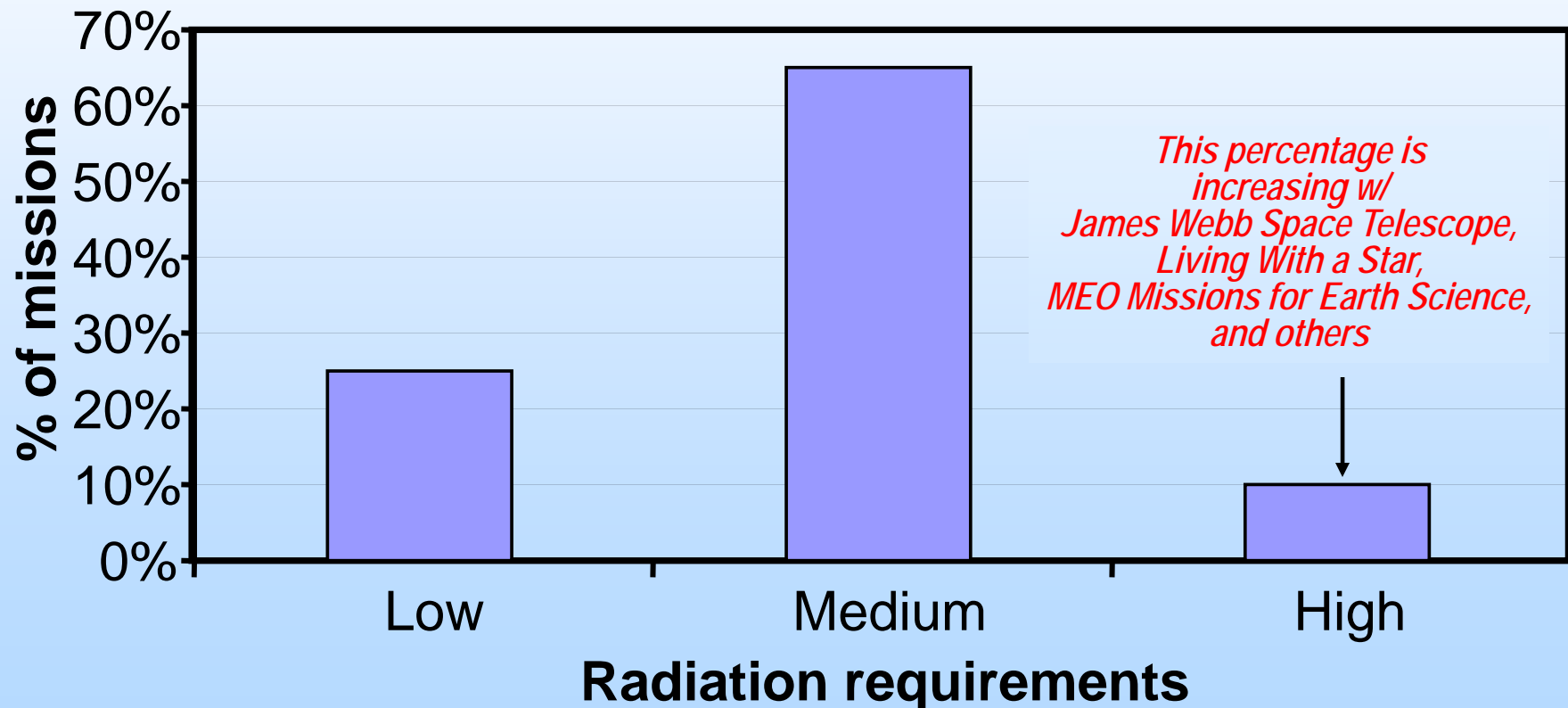
Aeronautics must deal with neutron SEE environment

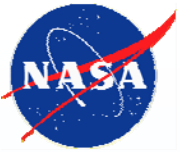


Mix of NASA Missions and Radiation Requirements

>200 missions are currently in some stage of development

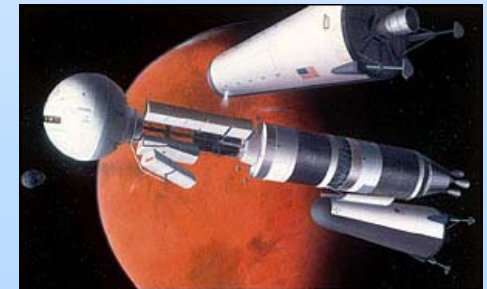
- Informal study has been performed of percent of missions in each category



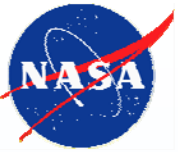


Implications of Radiation Needs for Hardening

- NASA philosophy has always been performance-driven
 - Increased capability within reduced spacecraft volume/weight/power – COTS?
 - **Radiation has usually been a secondary consideration**
- NASA Radiation Hardness Needs
 - SEE: hard to destructive issues, tolerant (or manageable) to non-destructive
 - TID/DD: 100 krad(Si) covers lots of ground for NASA
 - Few missions require above this level (even with design margin)
 - Europa being an obvious exception
 - DD becomes a larger issue for new nuclear propulsion missions
 - Added neutrons to the environment exposure



Artist's conception of a nuclear-powered MARS mission

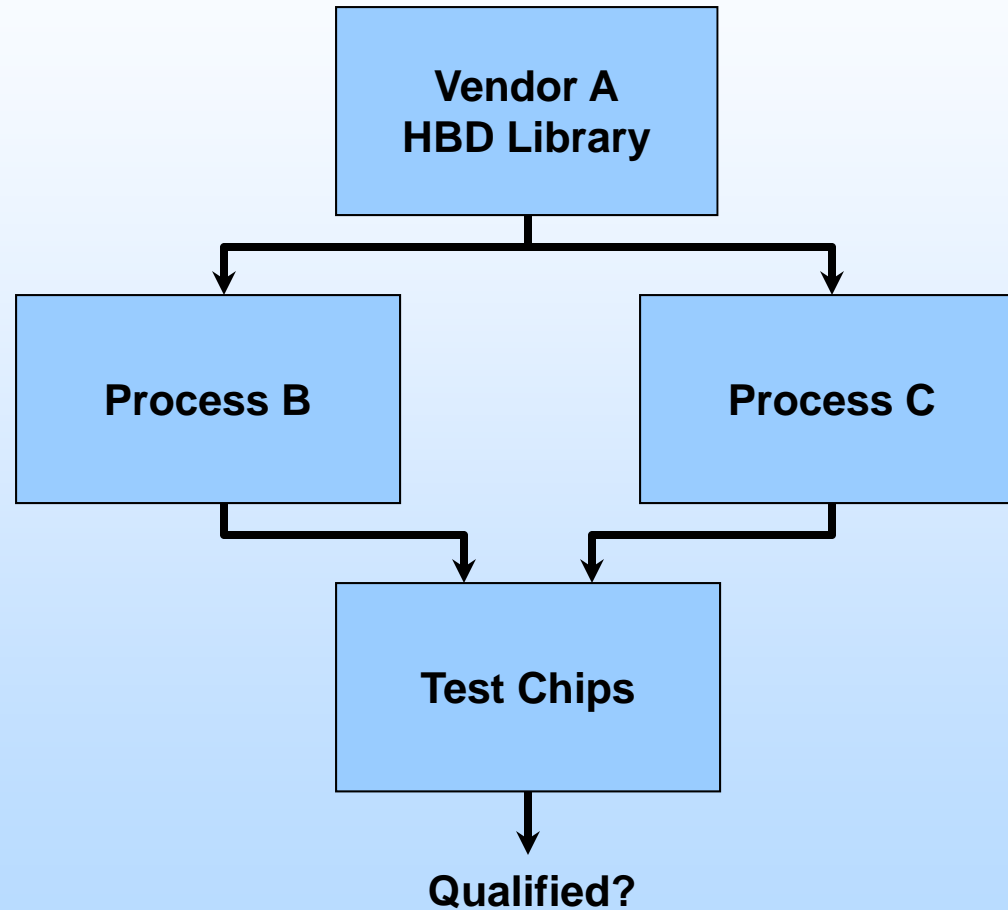


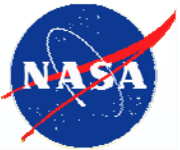
Radiation Test Considerations

- **Standard items**
 - Existing microelectronics test standards and guidelines for devices
 - ASTM, MIL-STD, JEDEC
 - Flux, fluence, rates, particle, etc...
 - Radiation test structures
 - Qualify a process
 - ASIC test methods
 - Qualifying a single design/chip
- **Unique aspects of HBD**
 - HBD can be a mix of minimally-invasive process tweaks and/or design methods (re: circuits like the Mission Research Corp.'s temporal latch)
 - **Some are “process-independent”**
 - The question becomes
 - **How do you qualify a HBD library that's portable?**



Sample HBD Test Consideration Scenario – Initial Flow





New Design: Is it already qualified?

**NASA
Project**

New chip design using HBD library; 9 months after test chip is qualified

Does HBD cover relevant effects?

**Was library designed for hardness to all relevant environments?
Nuclear dose rate hardness does not imply SEE hardness**

Any process changes?

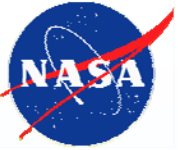
**Was any hardness characteristic a function of the process?
Might drive process selection (B versus C)**

Test chip coverage?

**Did the test chip cover all the library cells?
Statistically?
If new test, some portion may be waived based on inherent hardness**

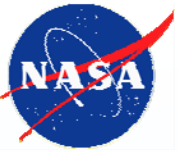
Chip operation?

**Were speed, operating voltages, etc. of the test adequate for the new chip?
Items like single event transients can be missed**



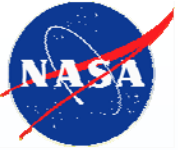
Summary of HBD-specific Test Considerations

- **These recommendations are mostly common sense**
 - Know the design library
 - Know the library coverage during “qualification”
 - Know how it was tested (versus your application)
 - Know the foundry/process
- **If all these items are known and applicable to the new chip design, then no new radiation testing may be required**



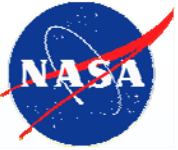
NASA Approach to HBD Evaluation

- In FY03, we have begun the process of evaluating different HBD techniques for NASA usage
 - Some have previous evaluation, while some are in development
- We have chosen the 8051 microcontroller as the test article
 - Industry standard device with COTS and HBD options available
 - Inexpensive test set development versus other complex devices
 - Mix of logic types: memory and combinatorial
 - Capable of operating at different clock speeds
 - Different power supply versions available
 - Moderately complex (realistic)
- Plan is to use the same test setup to evaluate SEE performance on both COTS and HBD devices in FY03
 - Example vendors include
 - Intel, Aeroflex-UTMC and University of Idaho's CMOS Ultra-Low Power Radiation Tolerant (CULPRiT)

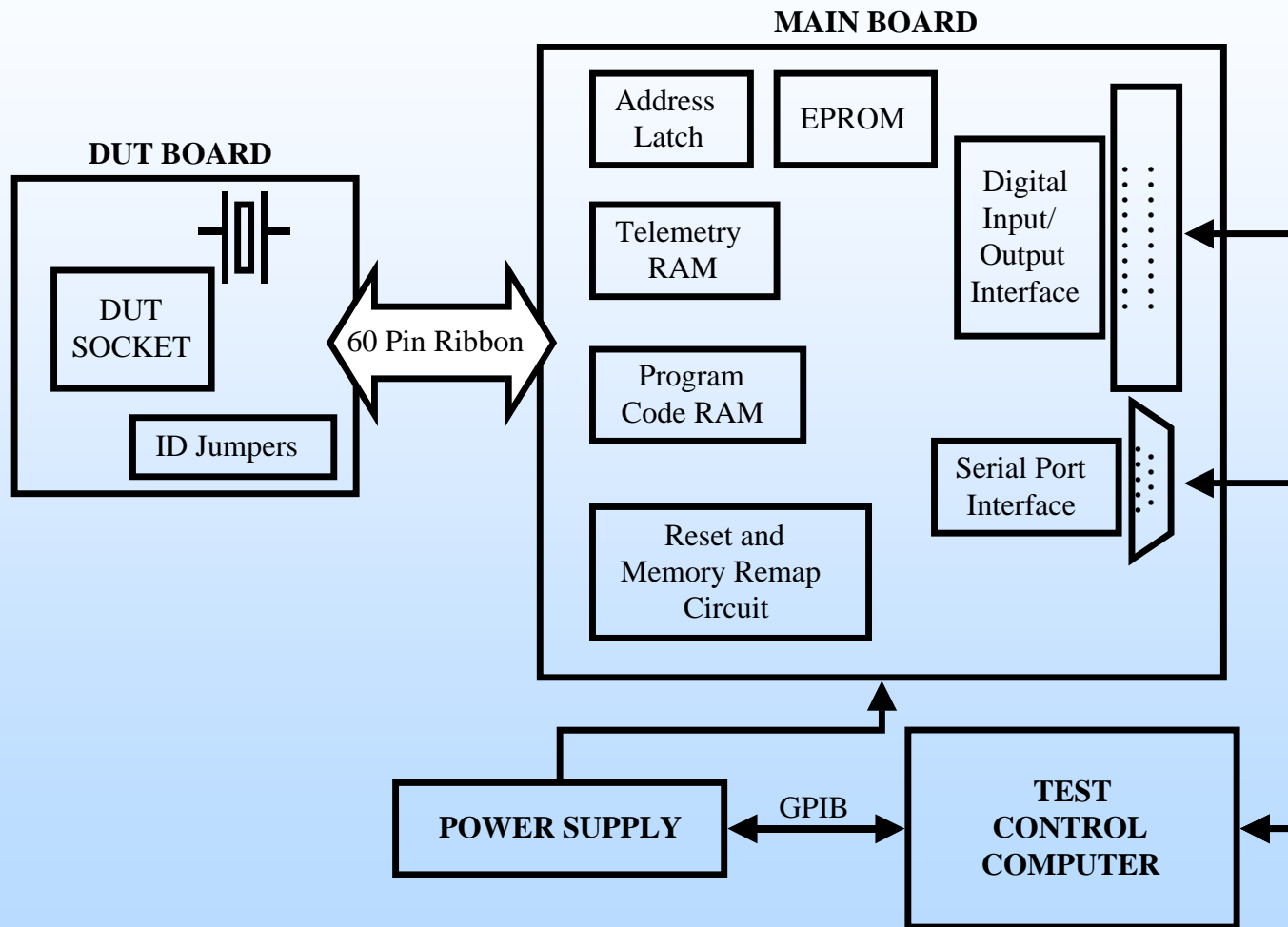


8051 Device Examples

- **CULPRIT**
 - ~0.5V V_{dd} device
 - Relies on inherent process TID hardness (AMI), but can tweak to gain additional hardness by use of backbiasing
 - SEL hardness by process
 - SEU hardness uses technique developed by Whitaker, Maki, et al for tolerant cell design
- **Mission Research Corp**
 - DoD technology development
 - Uses temporal latch designs
 - Foundry independent
- **Intel**
 - Strictly commercial
 - Used as a baseline for development and benchmarking

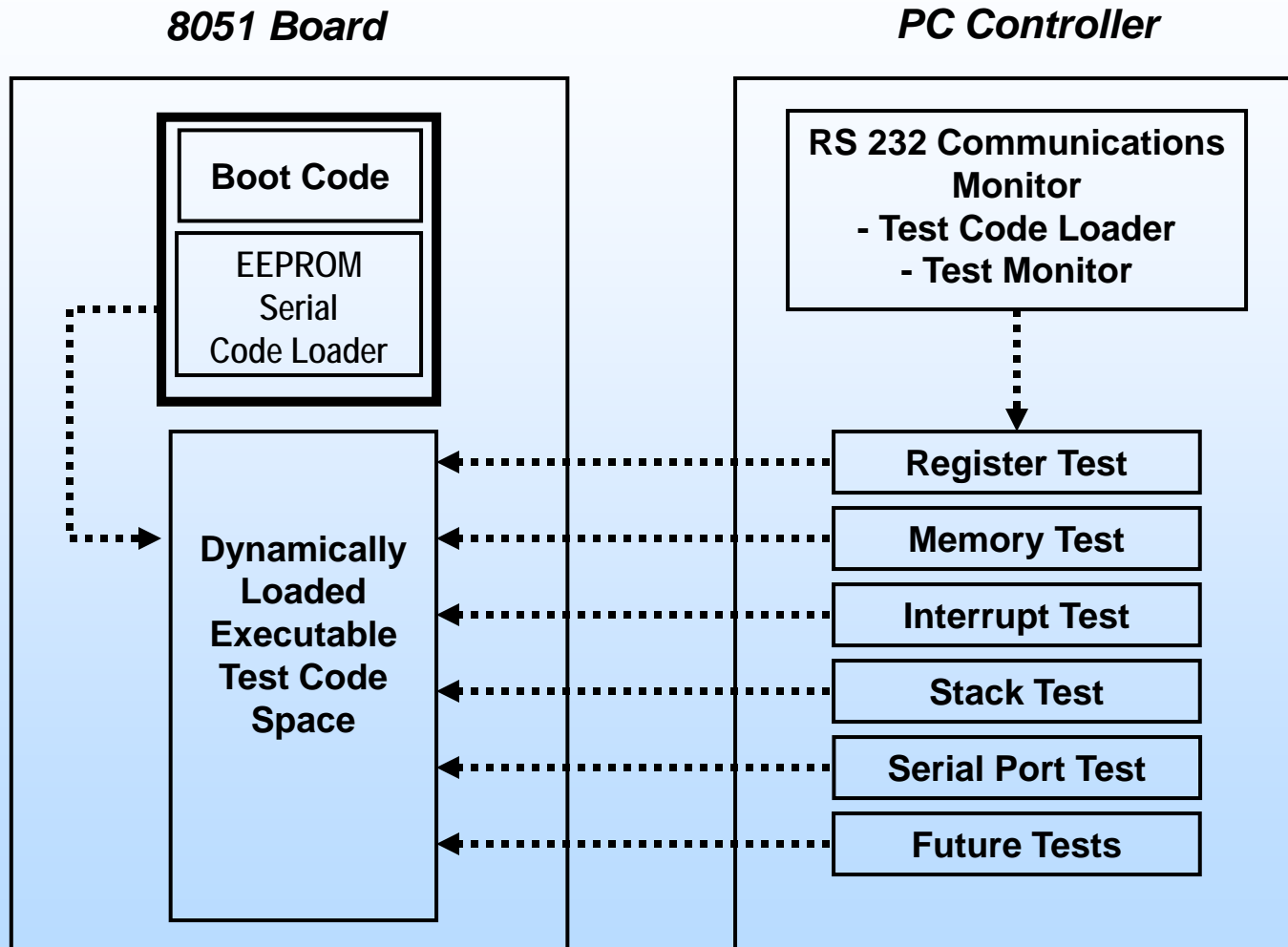


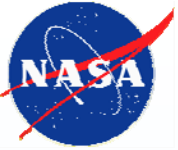
8051 Test Setup





8051 Software Testing





Summary and Comments

- **HBD is very applicable to many NASA missions**
 - Not all missions have time to develop and qualify custom designs
 - If “pre-qualified”, problem is reduced
 - Performance parameters required using COTS
 - **We did not discuss the impact of HBD on electrical (re: speed/power/size) performance**
- **Know what your testing and what has been tested and applicability**