Ken's Top Five Hidden SEE Test Challenges for 2011

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Outline

- Introductory Comments
- Single Event Transients (SETs)
  - It's just a pulse, right?
- Design Synthesis
  - Do you know what your circuit looks like?
- Co-design Issues
  - Why doesn't your circuit work like you expected?
- Angular Effects
  - Rock and roll…
- Rate Prediction
  - What next?
- Final Thoughts

Introduction

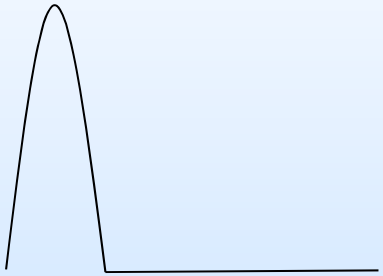
- **We've previously discussed the development of a "checklist" approach to planning single event effects (SEE) testing (HEART 2008). This talk takes that further and provides:**
  - **Updates to several of the concerns voiced previously, and,**
  - **New thoughts on data analysis and test system integrity**

SETs

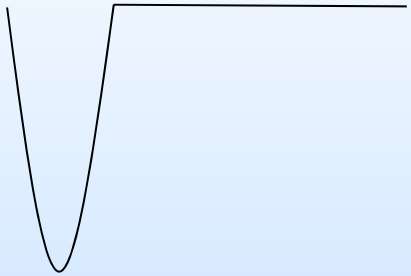
- **Wikipedia**
  - **“In digital and analog circuits, a single event may cause one or more voltages pulses (i.e. glitches) to propagate through the circuit, in which case it is referred to as a single-event transients.**
  - **Since the propagating pulse is not technically a change of "state" as in a memory SEU, one should differentiate between SET and SEU.**
  - **If a SET propagates through digital circuitry and results in an incorrect value being latched in a sequential logic unit, it is then considered an SEU.”**
- **Sounds simple, right? It’s just an output pulse that’s affected by the surrounding circuitry (basic EE101 RC theory).**

Types of SETs - ideal

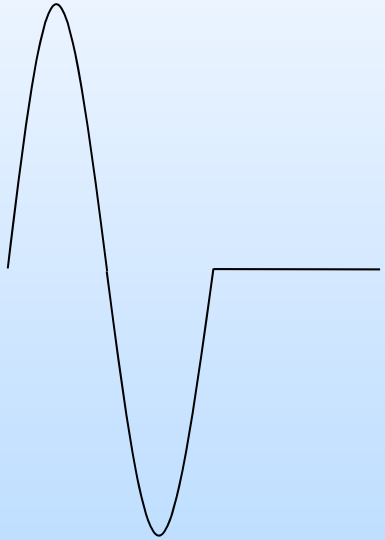
- But the world is not ideal, and pulses are rarely "clean"



Positive going SET



Negative going SET

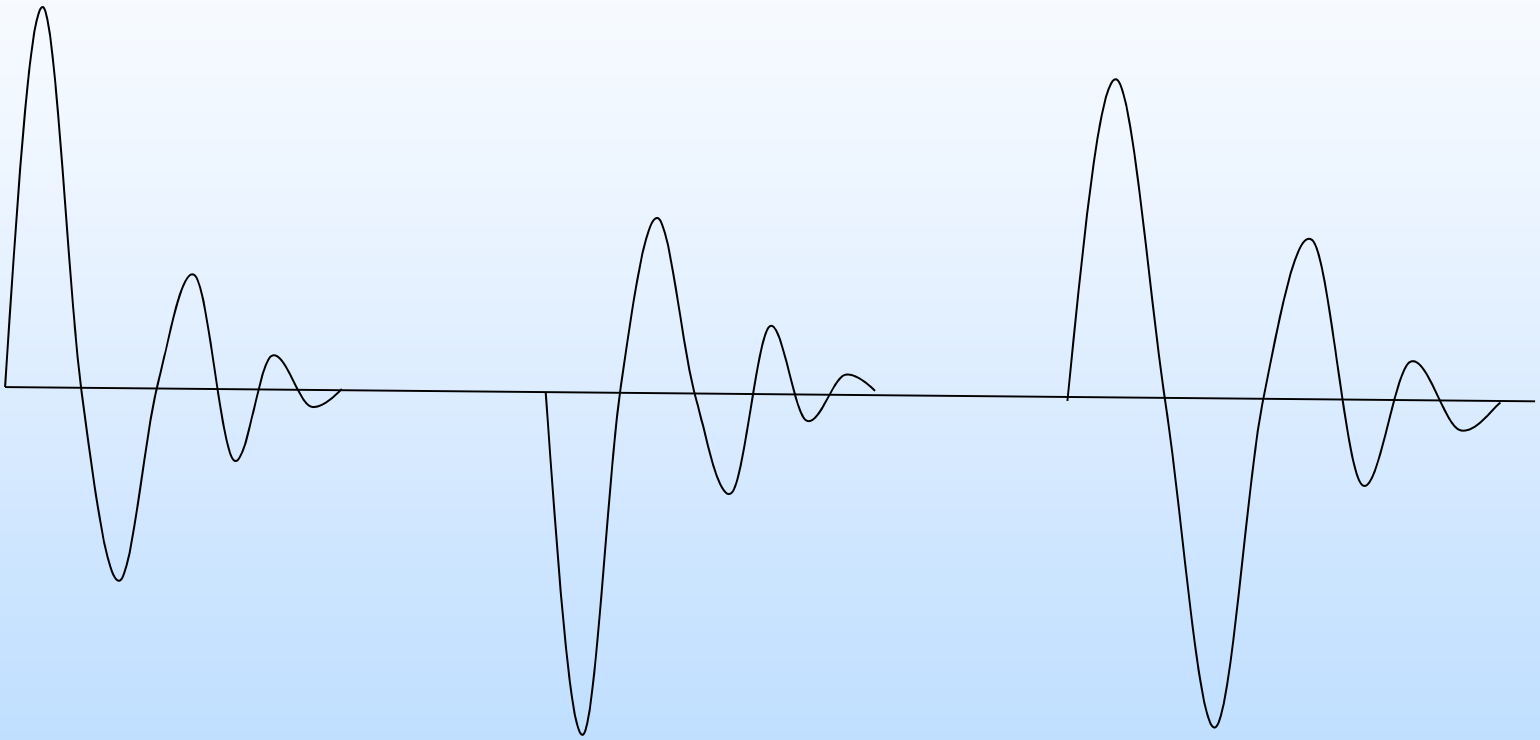


Bipolar SET

Nice and simple

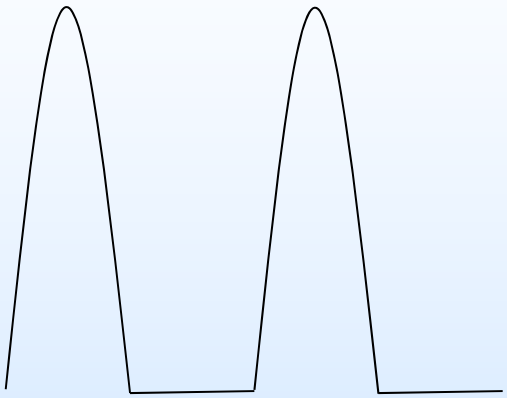
- Full-width half max, pulse height/width , etc… analysis

But often SETs are not so ideal…



SETs w/ ripple or oscillation

Or even…



Is this one event or two?

- add in some ripple and …

SET Thoughts

- Test set should emulate nearly exact conditions as application
  - Probe/cable impedance, etc… should be accounted for in test set design
- Automated analysis is tricky
  - Use spec sheet limits (i.e., ignore all ripple within 5% of expected value)?
  - Set an arbitrary exclusion zone for width and height?
  - Use statistical theory?
  - Is ripple sufficient to propagate further?
  - Hand analysis is time-consuming
- Bottom-line is be wary of “simple” test results

Design Synthesis

- Coming from the days of using a template and engineering graph paper, it's important to really know exactly what your circuit looks like.
- With modern high level design languages like VHDL and Verilog as well as graphical design tools that are even more abstract, designs are "synthesized" down to "optimized" circuits
  - Designed for function
  - Not for space reliability
  - Nor necessarily giving you what you expect!

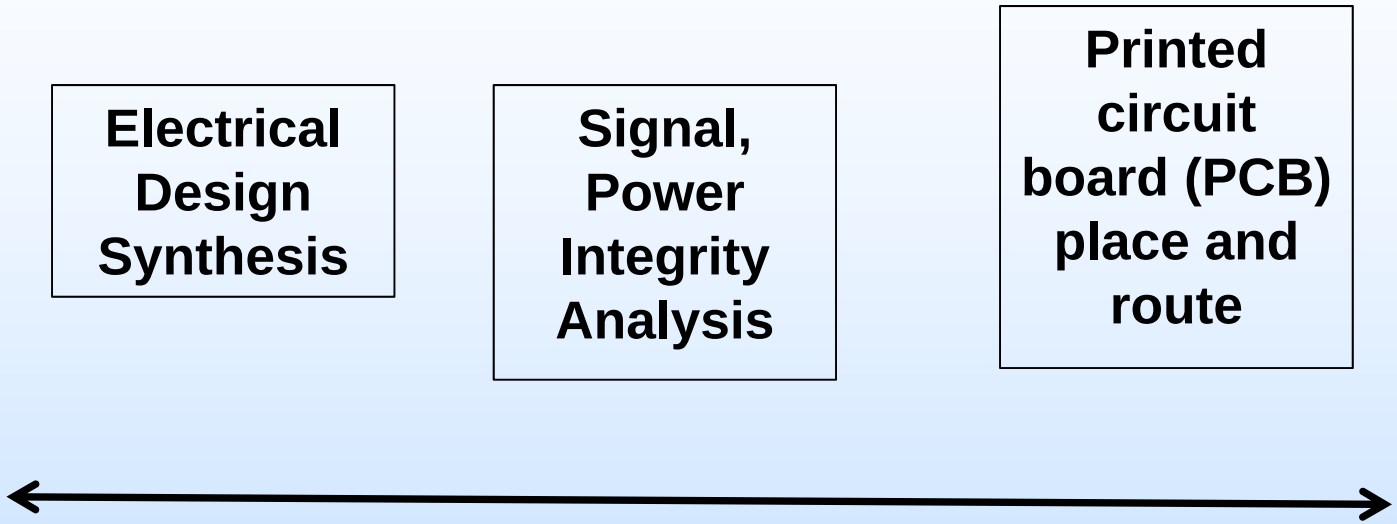
DS – what you see…

- **Example (courtesy of Melanie Berg):**
  - **I'm building a test circuit internal to an FPGA**
  - **It is a chain of inverters (speaking of propagating SETs…). Several strings of say, 0, 5, and 10 inverters**
  - **Synthesis optimization may reduce this to:**
    - **0,1, and 0 inverters**
  - **How good would these test results be for "planned test circuit"?**
- **Design tools often have options for circumventing optimization or manually inserting specific circuits**
  - **Routing (internally) needs to be looked in a similar vein**

Co-design

- **Wikipedia**
  - **"Co-design is a philosophy in the American pragmatist tradition, which argues that all people have different ideals and perspectives and that any design process needs to deal with this.**
  - **Co-design has recently become popular in mobile phone development, where the two perspectives of hardware and software design are brought into a co-design process."**
- **Many integrated design toolsets are developing co-design flow**
  - **Old way to build test boards was a serial process w/ limited feedback between tools**
    - **Could lead to missed issues in timing and application**

Co-Design: Simplified Flow



Tools interact with each other

The simple "lesson" is that design complexities have increased, IO has increased, operating frequencies have increased, and more and varied power supplies are used.

Designs are no longer "piecemeal", but need co-design considerations or suffer less reliable test systems.

It's a tilt and roll world…

- This is just a "reminder"
  - The space environment isn't just a normal incidence exposure
    - It's fairly omnidirectional
  - Ground heavy ion facilities have limited energies when compared to space exposure. This implies limited ion penetration limiting what angles can be used.
- So, two issues
  - Omnidirectional response, and,
  - Limited oblique angles (maybe 60-70 degrees max typical)

Thoughts on angle…

- **Most often, SEE data is taken in a single tilt direction**
  - **Sometimes both**
  - **Sometimes a 90 degree roll (rotate test board)**
  - **This is hardly omnidirectional, but VERY discrete**
  - **Beware:**
    - **Asymmetry of device (not just an array of memory cells anymore!)**
    - **Multi-node strikes**
    - **Secondaries from odd material interactions**
  - **We've demo'ed a goniometer approach as a means of RHA, but it's still not ideal.**
- **Oblique angle is still an issue**
  - **Same types of errors as "normal"?**
  - **Rate prediction?**

Not a hidden issue, but …

- **Rate Prediction**
  - **Ugh! Do we know what to do with low energy proton effects, angular incidence (oblique), and so forth for ultra-scaled technologies?**
  - **And what's a realistic way of predicting SEGR and SEB that's not "too" conservative?**
- **New tools**
  - **CRÈME-MC**
    - **Funding slashed, so may or may not end up as really useful tool for more than simple designs**
    - **You can get to some other tools at SPENVIS that have similarities**
  - **Alternates**
    - **Either "proprietary" and/or not validated**
- **What do we do now? Use CRÈME96 and add margin???**

Final Thoughts

- These are far from the only issues out there
  - Device prep
  - Thermal
  - Spot size
  - Noisy cyclotron facilities, …
- Test guidelines and method updates are fine, but devices are evolving faster than we can provide these.
  - Think, talk, and do the right thing!
    - Simple isn't so simple
    - And complex is complex!