Hardness Assurance for Total Dose and Dose Rate Testing of a State-Of-The-Art Off-Shore 32 nm CMOS Processor

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***Abstract*— Hardness assurance test results of an Advanced Micro Devices, Inc. (AMD) 32 nm processor for total dose and dose rate response are presented. Testing was performed using commercial motherboards and software stress applications versus more traditional automated test equipment (ATE).**

***Index Terms*— radiation, total dose, silicon on insulator (SOI), processor, test method**

I. Introduction

There has been much discussion throughout the government and industry regarding the International Traffic in Arms (ITAR) regulations as they pertain to radiation-induced device tolerance [1]. This is a dual-edged sword:

- How to protect critical U.S. technologies from unfriendly hands, while at the same time,
- Commercial semiconductor manufacturers fear inadvertently exceeding the ITAR radiation levels.

By utilizing a representative non-U.S. foundry, the authors sought to evaluate how this semiconductor process would fare against a subset of the ITAR criteria: total dose and dose rate (DR) limits for upset and latchup.

How the testing was performed is of note and appropriate for discussion within the radiation effects community: we utilized commercial processor motherboards as both testers and bias boards, forming the basis for a suite of "stress" tests. These are software tests that stress the device and measure performance.

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II. Test Techniques and Setup

A. *Device Under Test*

The device under test (DUT) we utilized is a modern state-of the-art dual-core processor from Advanced Micro Devices (AMD) [2]. The device part number is AMD A4-Series AD3300OJHXBOX (see Fig. 1). This is a 2.5 GHz dual-core processor with integrated floating point unit and both level 1 and level 2 caches packaged in a 905-pin lidded micro-Pin Grid Array (µPGA) package. The device utilizes the Llano processor core with on-chip peripherals, including a dual-channel double data rate generation-3 (DDR3) memory controller, a Peripheral Component Interconnect (PCI) Express 2.0 controller, and high-definition graphics controller all in a 228 mm^2 die. The device has an average thermal design power of 65 W. The production date code is DA 1153PGN.

AMD is a fabless semiconductor manufacturer. This specific device is built on GLOBALFOUNDRIES' 32 nm fabrication process located in Dresden, Germany. The complementary metal oxide semiconductor (CMOS) process includes hi-κ metal gates (HKMGs) on a partially-depleted silicon-on-insulator (PD-SOI) substrate.

Fig. 1. AMD A4-3300 series microprocessor.

B. Facilities Utilized

For total dose testing, a ^{60}Co gamma ray source was utilized, while a linear accelerator (LINAC) was used for dose rate testing.

C. Test Setup: Total Dose

Traditional total dose testing typically utilizes a combination of a standalone bias board used for step stress irradiations and automated test equipment (ATE) running test vectors to provide coverage of a high percentage of functional paths and parametric measurements [3]. There are two invasive challenges for modern state-of-the-art processors (and similar complexity devices):

- Cost paradigm: the cost of ownership or access to appropriate ATE to adequately test the device is high and limited; and,
- Test vector access: these are usually proprietary to the device manufacturer and the cost/schedule required to recreate them is prohibitive.

Both of these challenges can be overcome if the device manufacturer is willing to partner for the test series, but there need to be other viable options if they will not.

The solution for this test campaign was to utilize a commercial motherboard as both the tester and as the bias board. We used a Biostar A55MLV motherboard compatible with the DUT [4]. As expected, this motherboard contains a significant number of other electronics, such as peripheral devices, memory chips, video processors, *etc*. This is a concern during board-level irradiation with ^{60}Co gamma rays.

The basic concept was to perform a "semi" in-situ irradiation where the motherboard was mounted in the test chamber with cable harnesses being fed to a user area (monitor, keyboard, *etc*.) as per Fig. 2. The motherboard was booted and a series of partial stress tests were performed on a scheduled basis during irradiation. A more complete series of stress tests were performed after irradiation steps where we checked full processor performance and limited set of parametric measurements. To exercise the DUT for pre- and post-irradiation steps, two applications were utilized to support performance testing:

1. HWiNFO64 [5]. This tool collects and displays information about the hardware configuration. Part of that software function is the ability to monitor and log electrical and environmental data from the motherboard, Central Processing Unit (CPU), Graphics Processing Unit (GPU), and other on-board sensors. These data are recorded for all tests.
2. IntelBurn Test [6]. This software provides a useful stress testing tool and benchmark. The program is a graphical user interface (GUI) front-end for a compiled executable that performs mathematical functions using the Linpack programming library, which is a software library for performing numerical linear algebra on digital computers [7]. This tool burdens the CPU workload and enables the user to determine when and if there are flaws in the CPU's ability to perform operations. Inconsistencies due to radiation are recorded.

A shielding setup was developed to reduce the total dose exposure on devices surrounding the processor. Fig. 3 shows the physical configuration of the shield. Fig. 4 shows a radiographic film overlay on top of the bias board/DUT. Table I shows specific doses measurements for one of the test runs.

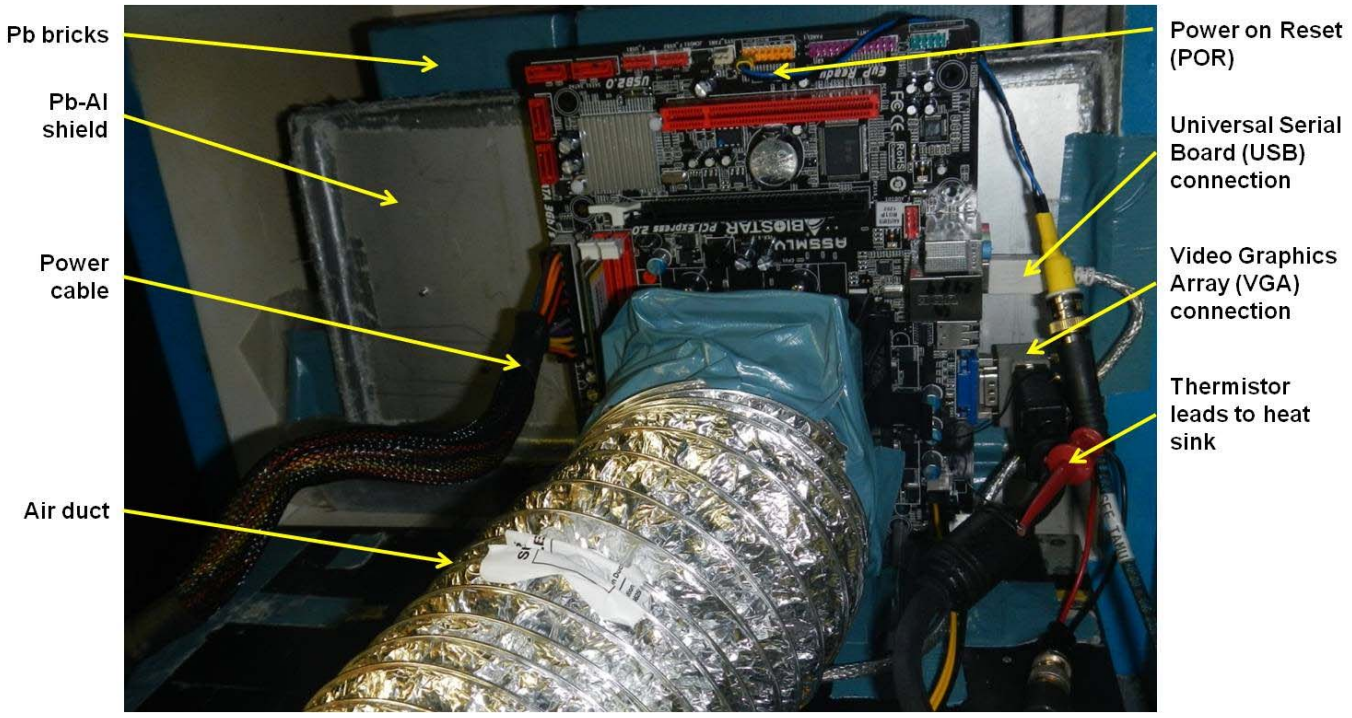


Fig. 2. DUT electrical configuration inside irradiation chamber (DUT is beneath the air duct).

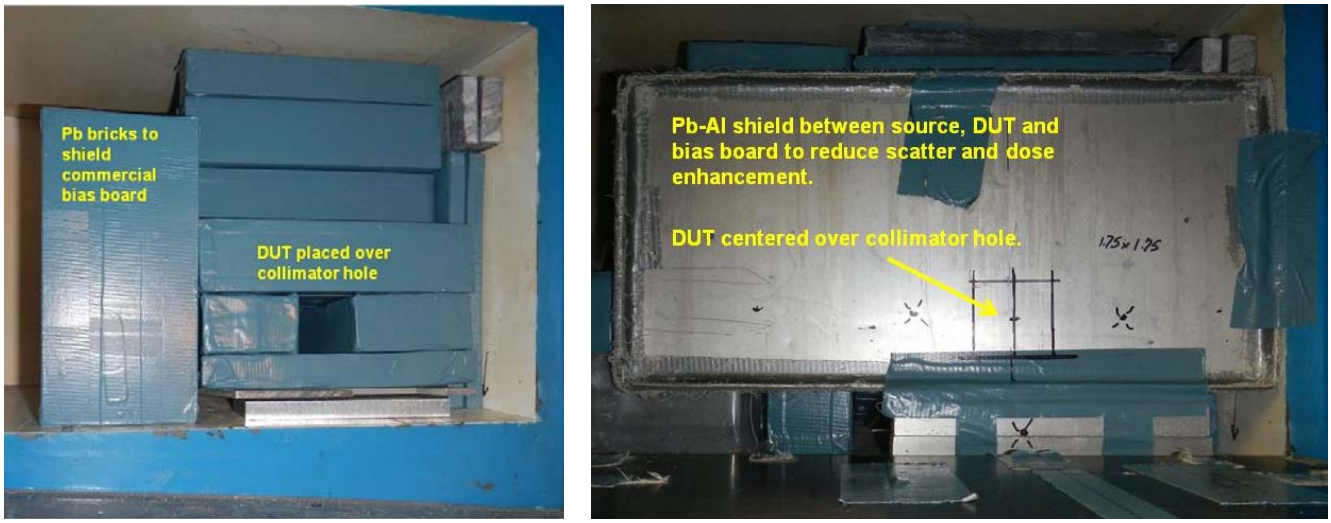


Fig. 3. Physical configuration of bias board shielding and DUT placement.

When the motherboard began having anomalies and hangups, irradiation was stopped and the processor was moved to a unirradiated motherboard for checkout (full stress tests). An unirradiated processor was also periodically used as a checkout for the irradiated motherboard failure. Irradiation would then resume as per above using the new motherboard with the irradiated processor.

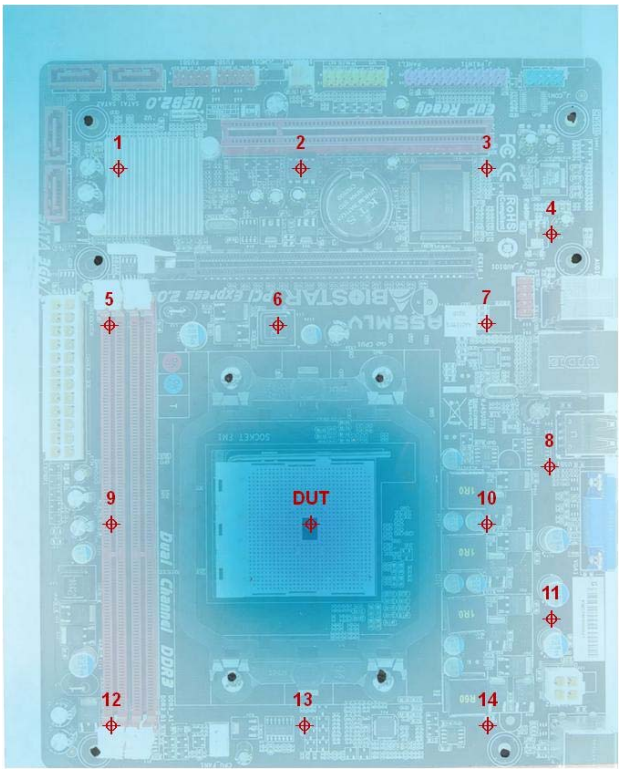


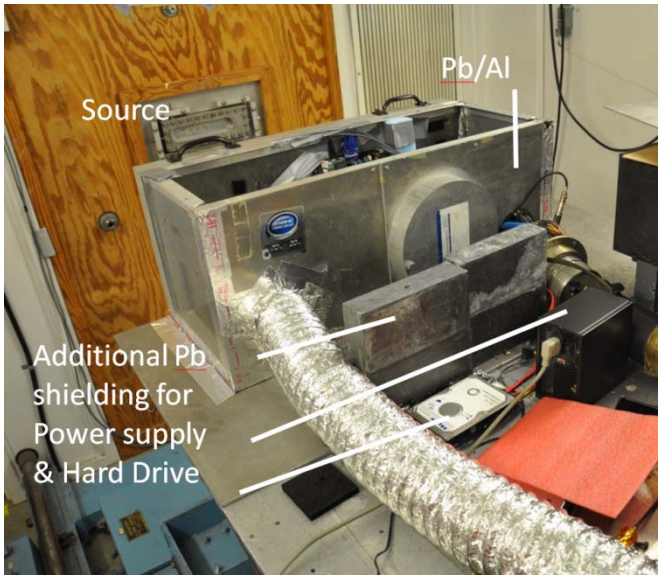
Fig. 4. Radiographic film overlay on bias board

TABLE I: MEASURED DOSE RATES FOR 4 MRAD(SI) SAMPLE.

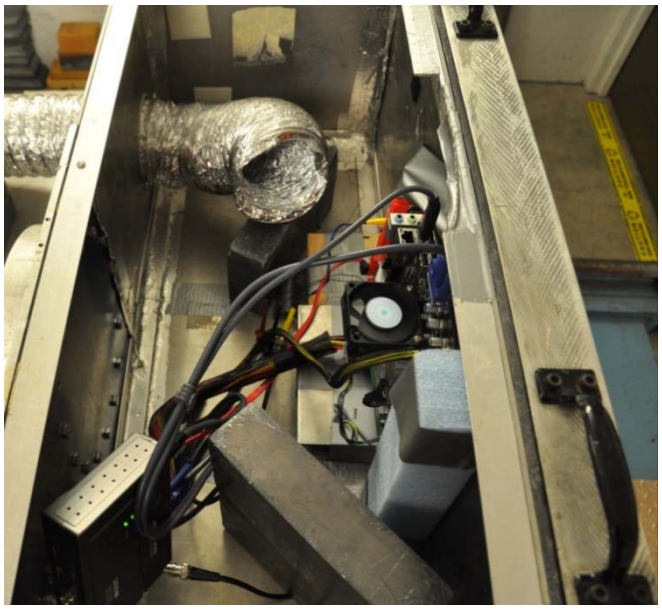
Dosimetry Location	Dose Rate (rads(Si)/sec)
1	0.11
2	0.12
3	0.12
4	0.07
5	0.07
6	0.11
7	0.08
8	0.08
9	0.09
10	0.12
11	0.08
12	0.24
13	0.47
14	0.30
9.72	0.11

D. Test Setup: Dose Rate

Dose rate tests were performed at NAVSEA Crane [8] using the linear accelerator (LINAC) in electron beam mode in accordance with ASTM F744M-10 [9], [10], [11] in a method similar to the total dose tests. ASTM was known until 2001 as the American Society for Testing and Materials. Exposures were made while executing IntelBurn Test software on the same motherboard as the total dose tests. Performance anomalies as well as board-level power consumption were recorded. A full suite of stress tests were run post-exposure. Fig. 5 illustrates this test configuration.



(a)



(b)

Fig 5. (a) and (b) Test setup at LINAC.

III. Test Results

A. Total Dose Results

Four samples have been irradiated to date using the semi in-situ test method. The total dose rate used was between 5 and 10 rad(Si)/s.

No apparent device degradation was apparent on any of the samples (*i.e.*, they passed all stress tests after exposure). Cumulative dose levels for exposures ranged from 1 to 17 Mrad(Si). For comparison, the ITAR level is 500 krad(Si).

During irradiation, the stress testing logged increasing device temperature with increasing radiation. However, through use of an infrared (IR) thermometer, it was determined that the DUT temperature had not varied significantly and it was likely a failure of the thermal diode or readout circuitry used. Fig. 6 illustrates a sample of this increase with dose.

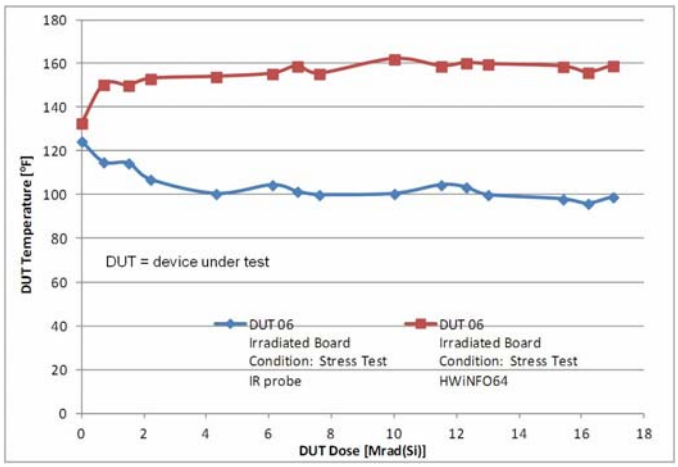


Fig. 6. CPU internal temperature sensor measurement using HWiNFO.

Failures occurred on the shielded motherboard (bias board) indicating that peripheral integrated circuits were likely sensitive to total dose levels well under 50 krad(Si) and as low as 1.1 krad(Si). These are devices of unknown manufacturers and fabrication processes. Replacement motherboards were then swapped in. The authors note that the failure on these other peripheral devices varied from board-to-board. The three main motherboard failures were:

- DDR3 memory module failure, though they passed performance testing in a TRIAD commercial memory tester [12] post-irradiation. Failure levels varied by memory module, with 1.1 krad(Si) being lowest failure level.
- Fan degradation at approximately 4 krad(Si) – this required a motherboard swap.
- One copy of the motherboard failed at 9.7 krad(Si). The failure indicator was a biased, but unknown state, which required a motherboard swap.

IV. Dose Rate Results

No dose rate latchup was observed up to $2x10^{10}$ rad(Si)/s. The processor operated through the beam shot at the same dose rate, however the video display "blinked" at every beam shot, including below $5x10^{8}$ rad(Si)/s – the ITAR level. The authors suspect this may be due to another integrated circuit on the motherboard, likely the graphics chip. Power-on-resets to the processor occurred at about $2x10^{9}$ rad(Si)/s. The individual beam shot results are show in Table 1I.

TABLE II: RESULTS OF DR TEST RUNS.

rad(Si)/sec	Response To Radiation
$5.6x10^7$	"Video Blink" - video temporarily blanked out, but independently recovered to normal in 2-3 sec. CPU and GPU stress test continued running. No visible artifacts in GPU window
$1.0x10^8$	"Video Blink"
$2.4x10^8$	"Video Blink"
$5.1x10^8$	"Video Blink"
$1.6x10^9$	"Video Blink"
$1.8x10^9$	"Video Blink"
$2.3 x10^9$	CPU turned off; power-on-reset (POR) to recover
$4.4x10^9$	CPU reset; auto recover
$8.2x10^9$	CPU turned off; POR to recover
$2.6x10^{10}$	CPU turned off; POR to recover

V. DISCUSSION

The methodology used for testing essentially was a "best effort" method to replace traditional custom bias boards and expensive ATE. The device manufacturers are able to afford both the ATE and the manpower to develop the test vectors due to profit motives from commercial sales volumes. Radiation test groups, unfortunately, are not able to afford these expenses and this is a novel compromise scheme to accommodate the evaluation of advanced microelectronics.

As noted, total dose and DR device tolerances exceed the ITAR limits for this off-shore fabricated design. To the best of the authors' knowledge, AMD has not intentionally radiation hardened the device for these environments, but the technology itself supports these characteristics.

Historically, the tolerance of commercial digital processors has shown increasing total dose tolerance as the feature size has shrunk. Table III illustrates this trend prior to this series of tests.

TABLE III: HISTORICAL HARDNESS OF PROCESSOR TECHNOLOGIES.

Device	Technology	Test Date	Results	Ref.
Intel 80386-20	1 µm CHMOS IV	1993	Failure between 5-7.5 krad(Si)	[13]
Intel 80486DX2-66	0.8 µm CHMOS V	1995	Failure between 20-25 krad(Si)	[14]
Intel Pentium III	0.25 µm	2000	Failure ~ 500 krad(Si)	[15]
AMD K7	0.18 µm	2002	Failure > 100 krad(Si)	[15]

It is also important to note the failures that did occur happened on the other integrated circuits on the motherboard. In particular, both the potential for variability of commercial electronics and low tolerance to total dose were observed.

VI. SUMMARY

We have performed a series of total dose and dose rate irradiations on a 32 nm off-shore product using commercial motherboards. Several takeaway points should be considered:

- Digital CMOS devices can definitely exceed the portions of the ITAR criteria that were tested here without any intentional radiation hardening.
- Multiple commercial support/peripheral integrated circuits (*i.e.*, surrounding the processor) failed at levels well below ITAR criteria. These are likely bipolar or analog (video) functions.
- No single conclusion can be made as to whether commercial technology is pushing the ITAR envelope inadvertently. Based on the results provided here, this will depend on the technology and device. However, the potential for some devices to push these levels is there.
- The hardness assurance method used here, while clearly not as thorough as traditional ATE, provides a reasonable approach that is cost-effective.

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