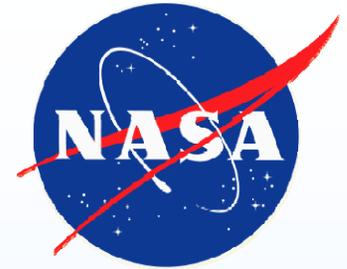


National Aeronautics and
Space Administration



Radiation Testing Considerations for Advanced CMOS Electronics

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Thank You to Sponsors and Collaborators



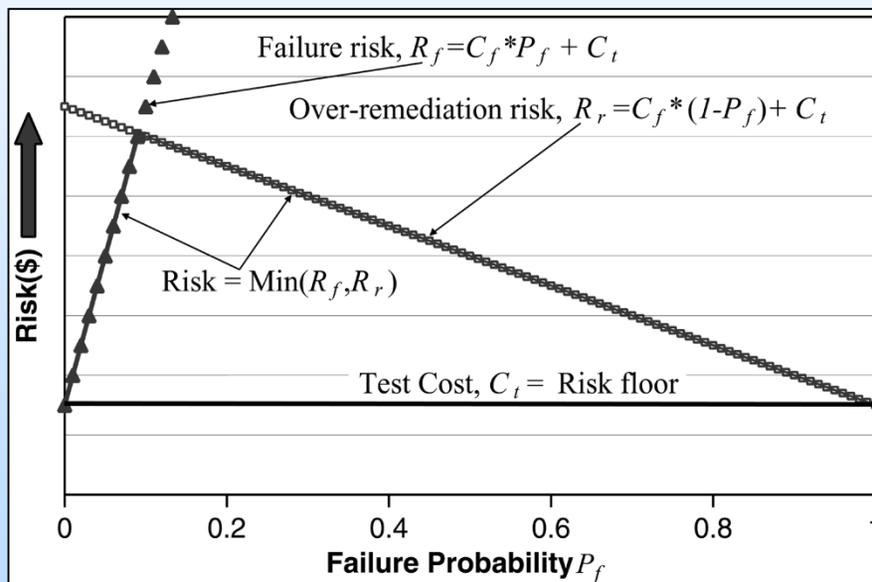
- **Sponsors**
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Goal Statement

For advanced CMOS electronics:

Gather necessary data to ensure that you can accurately bound the risk for a given mission application



- **Two risks**

- **Decide to fly the part “as is” when the risk of failure is unacceptably high**
- **Decide part requires remediation (*i.e.*, testing) when its failure probability was sufficiently small “as is”**

R. Ladbury *et al.*, *RADECS*, Cap d'Agde, France, 2005, pp. PB1-1-PB1-8.

CMOS = complimentary metal oxide semiconductor

Outline



- **Describe two flavors of advanced CMOS**
 - Commercial-off-the-shelf (COTS)
 - Radiation-tolerant standard products and application specific integrated circuits (ASICs)
- **Define “necessary data”**
 - Total ionizing dose
 - Single-event effects ← *key driver*
- **Question how we “accurately bound the risk” for a given mission**
 - Phenomenological,
 - Analytical, and
 - Statistical techniques
- **Conclusions**

Advanced CMOS Flavors



- **COTS**

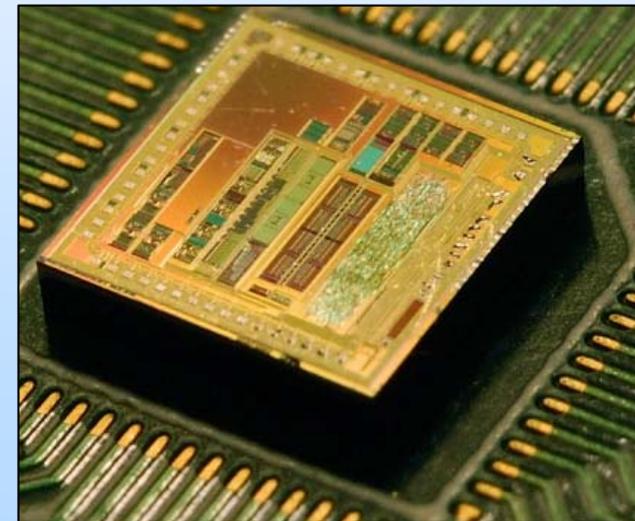
- Designed with no attempt to mitigate radiation effects. COTS can refer to commodity devices or to ASICs designed using a commercially available design system.

- **Radiation-tolerant**

- Designed explicitly to account for and mitigate radiation effects.
 - By process and/or design



<http://www.samsung.com/us/computer/memory-storage/MV-3T4G3/US>



<http://www.embedded-systems-portal.com/CTB/ASIC,1005.html>

K. Kohnen and K. Chestnut, *IEEE NSREC Short Course*, 2009.

Examples of Advanced CMOS

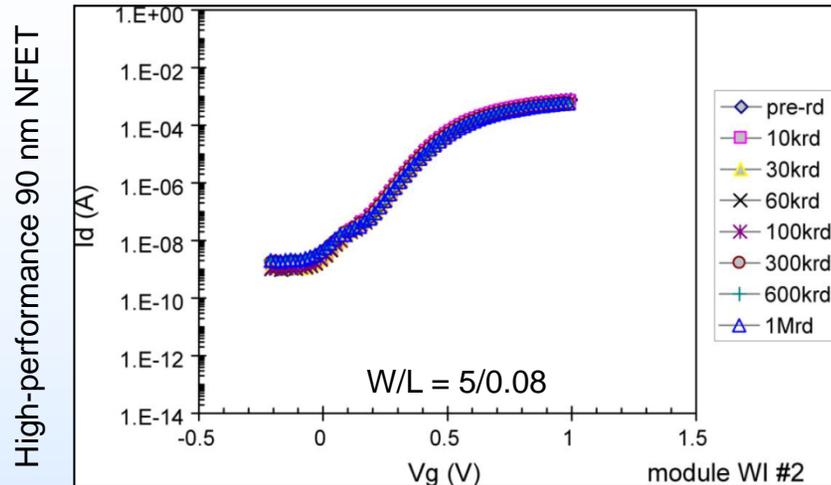


- **COTS**
 - Synchronous dynamic random-access memory (SDRAM)
 - Flash memory and other non-volatile solutions
 - Data converters
 - High-speed amplifiers
 - Digital signal and multi-core processors
 - Field programmable gate arrays (FPGAs)
- **Radiation-Tolerant**
 - RHBD + RHBP in boutique foundries
 - RHBD applied to AMS, IBM, Jazz, ONSem, or TSMC \leq 90 nm bulk/SOI CMOS
 - Use of pre-processed (*i.e.*, hardened) silicon substrates in commercial process flows
 - FPGAs

AMS = AustriaMicroSystems

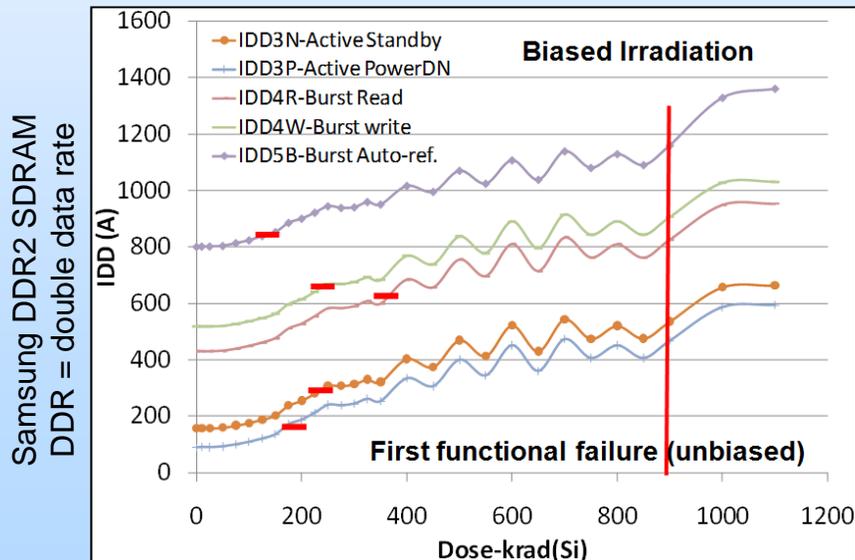
TSMC = Taiwan Semiconductor Manufacturing Co.; SOI = silicon-on-insulator
RHBD = radiation-hardened by design; RHBP = radiation-hardened by process

Total Ionizing Dose (TID) Data



N. F. Haddad et al., *IEEE TNS*, 2009.

- One bright spot for most missions that use highly-scaled technologies
- Thinner oxides have led to increased TID tolerance
 - For NASA, meets most mission requirements
- One exception might be floating gate (FG) non-volatile memories
 - FG cells and charge pump are susceptible to TID



R. L. Ladbury et al., *NEPP Electronics Technology Workshop*, 2011.

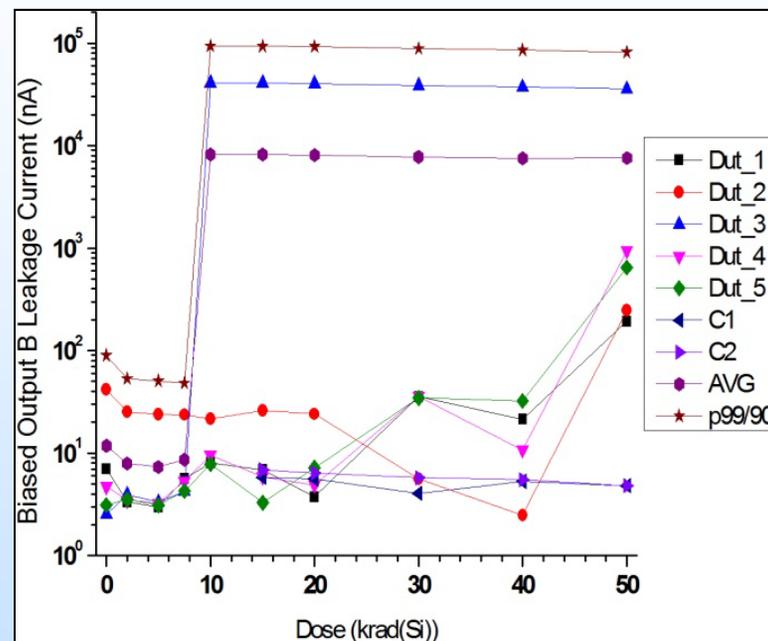
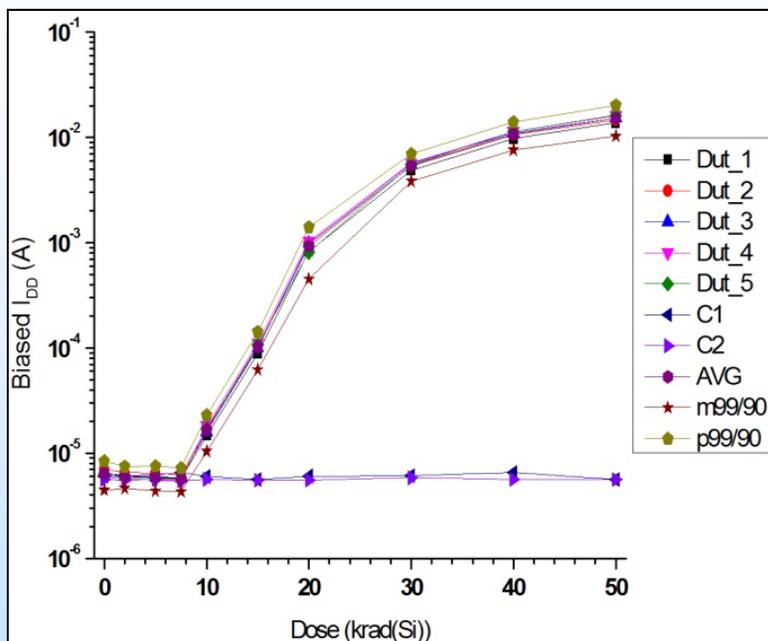
T. R. Oldham et al., *IEEE TNS*, 2006.

M. Bagatin et al., *IEEE TNS*, 2011.



Total Ionizing Dose (TID) Data

Analog Devices AD5544 CMOS 16-bit Digital-to-Analog Converter
(0.5 μm CMOS used to demonstrate a point)



Thank you to the NASA Magnetospheric MultiScale (MMS) Mission for testing support

- **Part-to-part and lot-to-lot variability**
 - Affects number of components that must be tested to bound risk
 - Limits usefulness of *heritage* data
 - Tied to bias conditions and temperature – combined effects

Bounding TID Risk

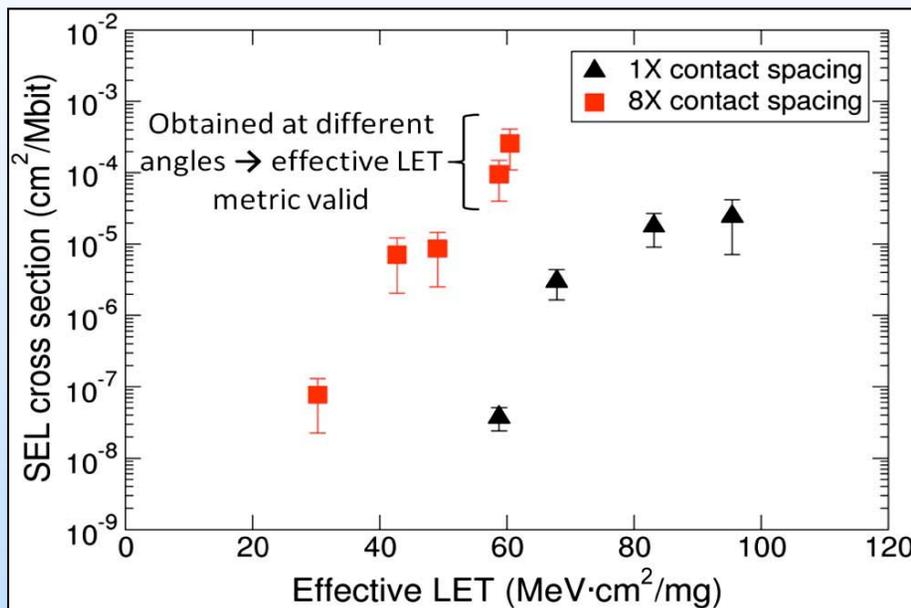


- **Test more hardware – easiest answer**
 - Example: 22 trials (*i.e.*, parts) with 0 failures establishes $p_s > 90\%$ with 90% confidence (binomial distribution)
 - Not always possible due to schedule, budget, hardware availability
- **Define part-to-part and lot-to-lot variability – dictates how many components should be tested**
 - Consideration for development phase with a process
 - Use kerf structures to gather test data on multiple wafer lots
 - Perhaps easier with qualified processes
- **Utilize heritage (suspension) and similarity data, if available, to augment analysis**
 - See R. L. Ladbury *et al.*, *IEEE TNS*, 2011.

Single-Event Effect (SEE) Data



45 nm bulk CMOS SRAM



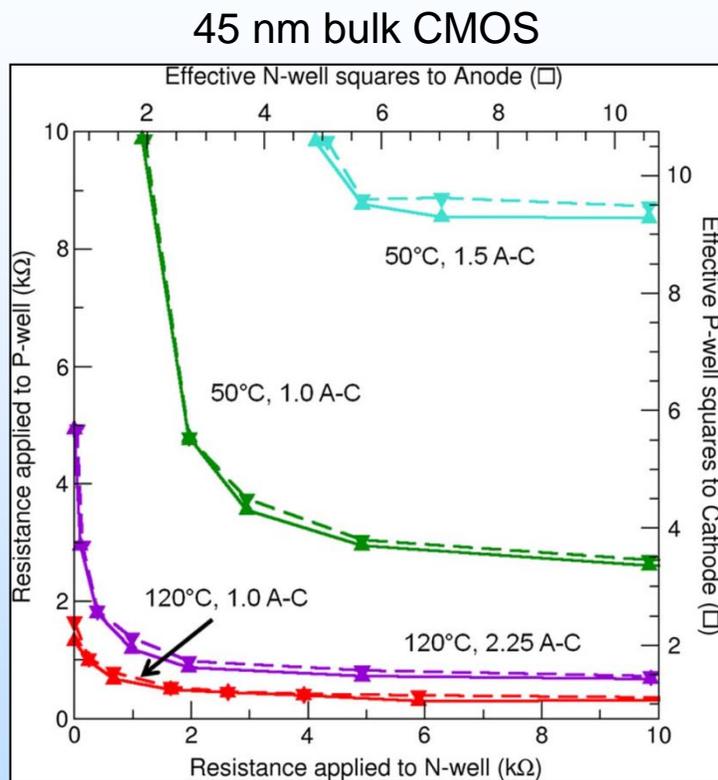
N. A. Dodds *et al.*, *IEEE TNS*, 2010.

Develop deterministic rules for layout that will avoid single-event latchup

SRAM = static random access memory

- **Destructive SEE can still be an issue with advanced bulk CMOS**
 - **Dependent on**
 - Rail voltage
 - Layout constraints
 - Temperature (cryogenic latchup)
 - C. J. Marshall *et al.*, *IEEE TNS*, 2010.
- **Solutions include**
 - **Efficient well contacting**
 - **Hardened silicon wafers or SOI process**

Single-Event Effect (SEE) Data



N. A. Dodds *et al.*, *IEEE TNS*, 2010.

- Contours are boundary where $V_{\text{hold}} = V_{\text{dd}}$
- Below = vulnerable; above = immune
- A-C = anode-cathode spacing

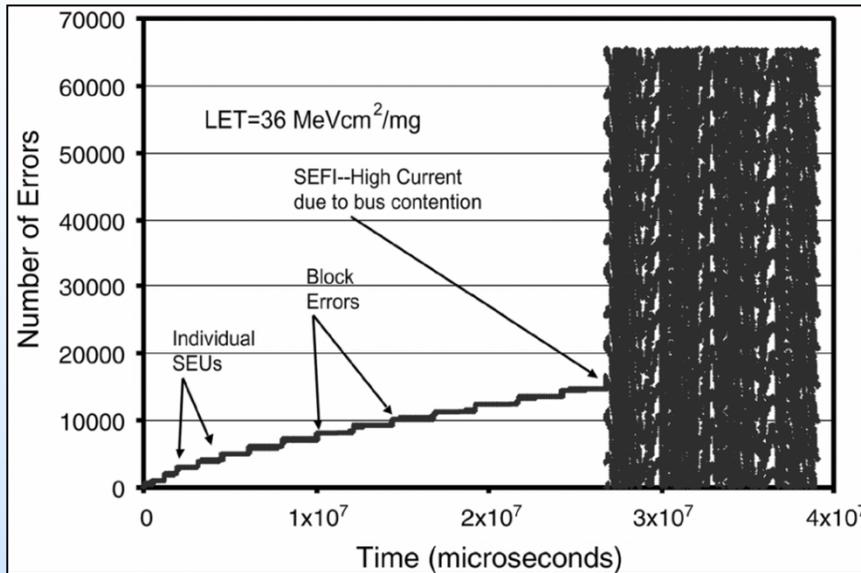
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Single-Event Effect (SEE) Data

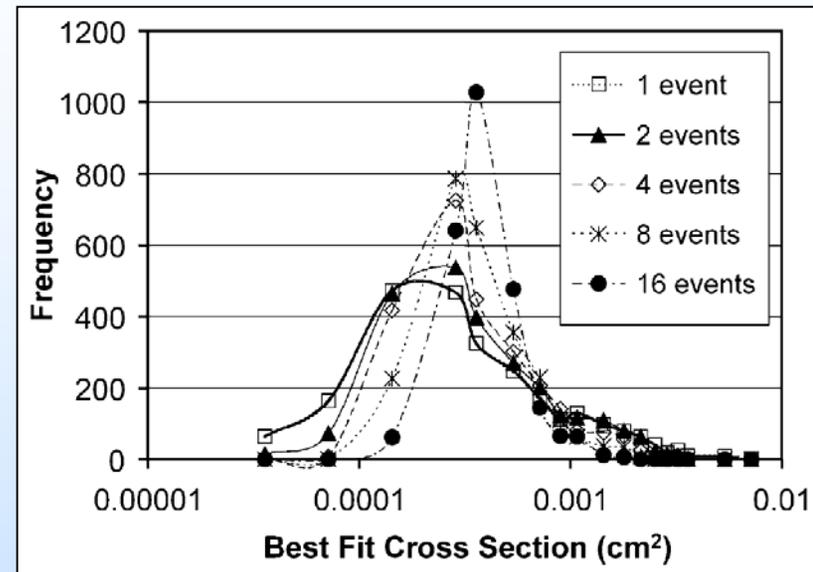


Sample SDRAM SEE Test Data



K. A. LaBel et al., *IEEE TNS*, 2008.

Convergence can be slow!



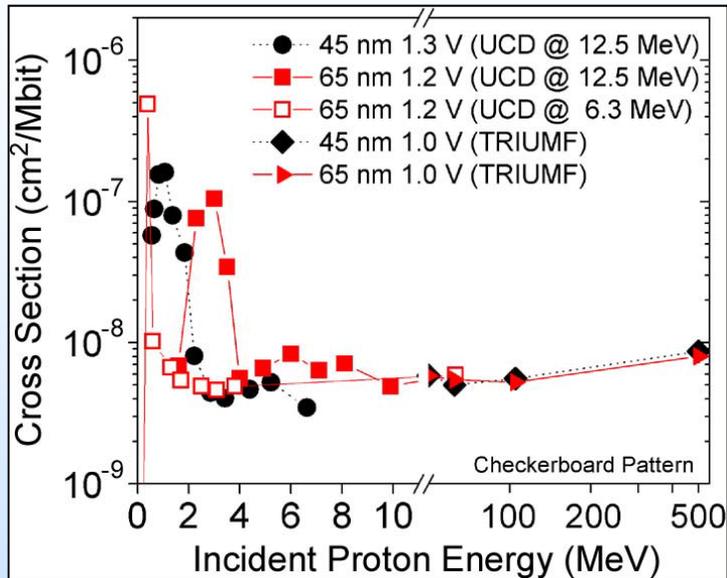
R. L. Ladbury et al., *IEEE TNS*, 2007.

- **Non-destructive SEE continue to be the most difficult aspect of advanced CMOS radiation effects**
 - Small event counts for effects like functional interrupts – often depend on state, location, *etc.*

Single-Event Effect (SEE) Data

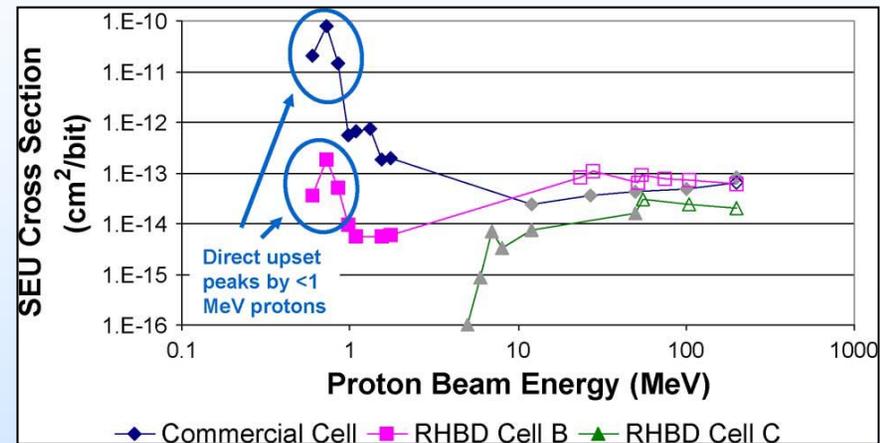


45 nm SOI CMOS SRAM



D. F. Heidel *et al.*, *IEEE TNS*, 2009.

90 nm bulk CMOS SRAM cell varieties



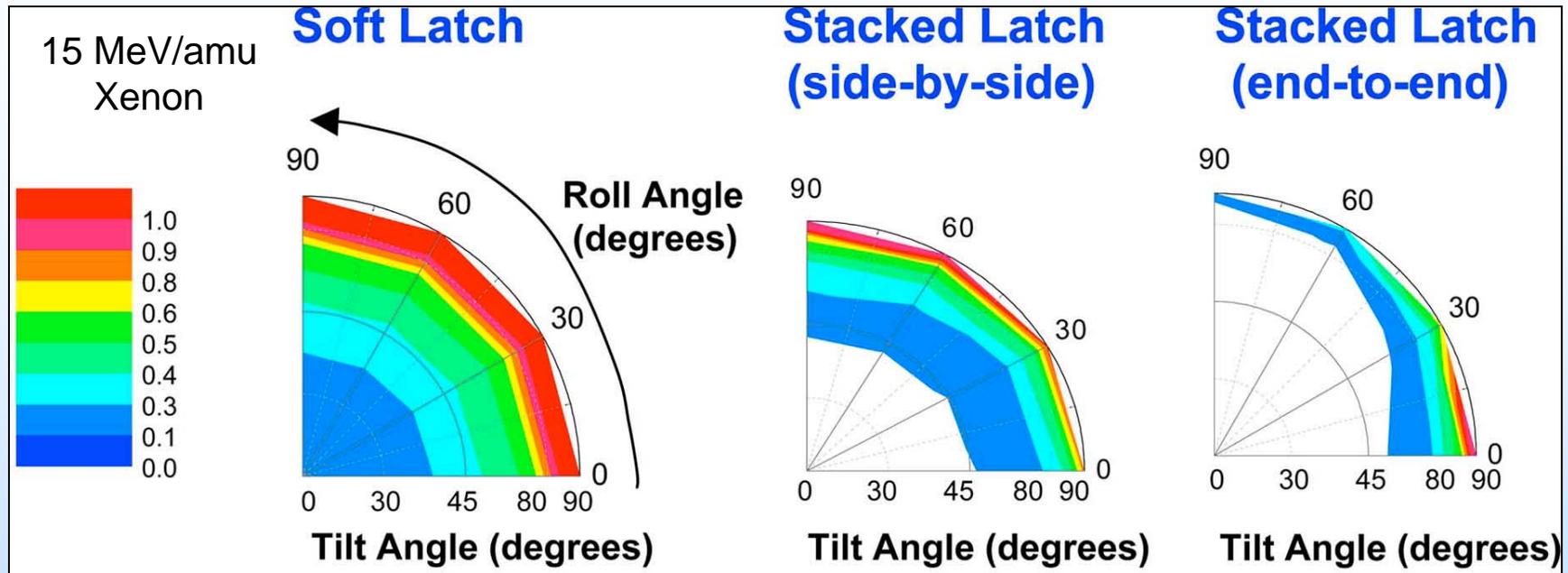
E. H. Cannon *et al.*, *IEEE TNS*, 2010.

- **Non-destructive SEE continue to be the most difficult aspect of advanced CMOS radiation effects**
 - **Potential threats from low-energy protons**

Single-Event Effect (SEE) Data



32 nm SOI CMOS latch cross sections – contours are based on data & simulation



K. P. Rodbell et al., *IEEE TNS*, 2011.

- **Non-destructive SEE continue to be the most difficult aspect of advanced CMOS radiation effects**
 - **Varied angular sensitivity (test considerations)**

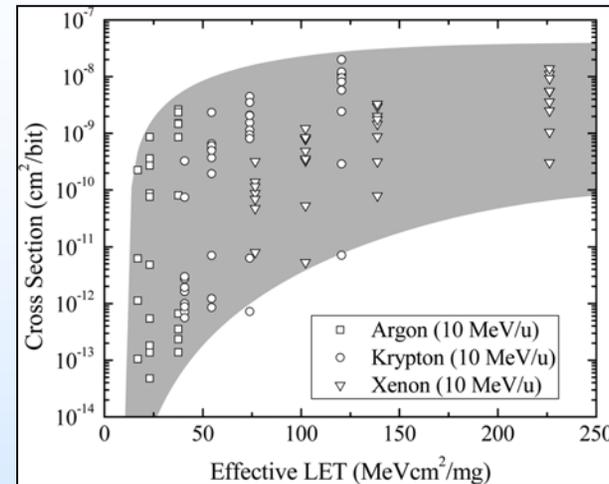


Bounding SEE Risk

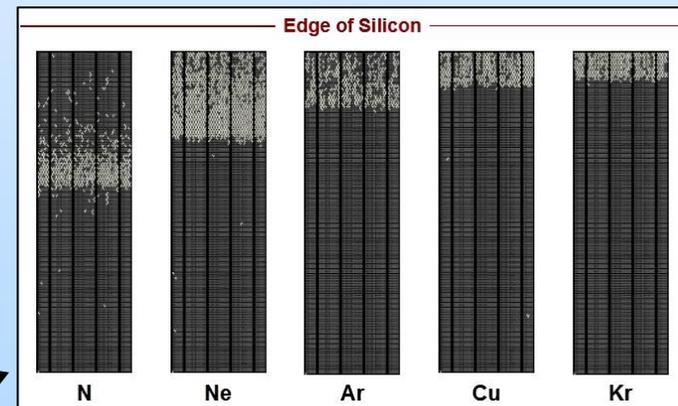
- Investigate risk of destructive events like latchup in bulk CMOS
- Recognize importance of roll and tilt angle sensitivities
 - Large-angle irradiations are critical
 - Test setup and packaging considerations
 - Observed in both SRAM and latches
- Choose the right tool to interpret the data and get an on-orbit event rate
 - From Figure of Merit to full, multi-dimensional Monte Carlo

True, end-on (90° tilt) irradiation of 90 nm bulk CMOS SRAM

90 nm CMOS, RHBD Latch



K. M. Warren et al., *IEEE TNS*, 2007.



D. G. Mavis et al., 2009 *SEE Symposium*; and 2009 *IEEE Int. Conf. IC Design and Tech.*



Summary

- **Size, weight, and power benefits of advanced CMOS dictate its use in certain applications**
- **TID performance is acceptable as-is in many cases**
- **SEEs are real radiation driver concerning advanced CMOS**
 - Risk of destructive effects still exists in bulk CMOS,
 - Rare non-destructive effects like functional interrupts,
 - Low-energy proton sensitivity, and
 - Angular effects that place requirements on test setup, packaging, and ion beam characteristics
- **Real need for simulation tools capable of both informing data collection and extrapolating data sets to yield on-orbit rates**
 - See, for example, R. A. Weller *et al.*, *IEEE TNS*, 2010.