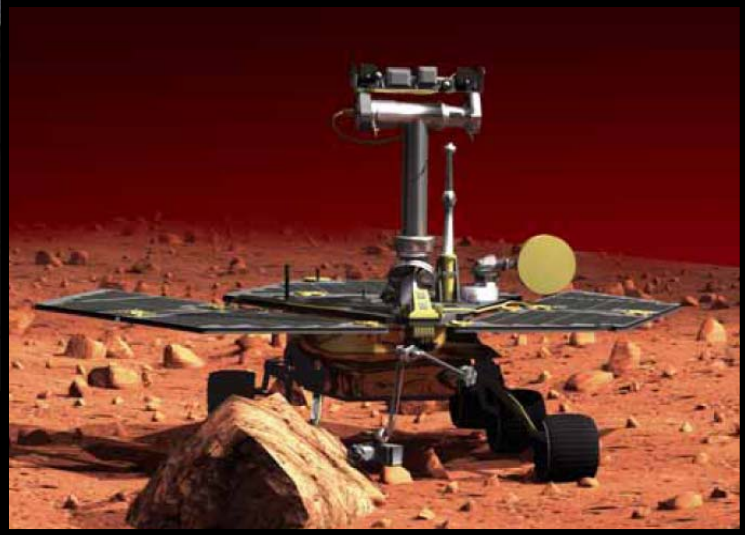
Characterizing Data Path Single Event Upsets in a Synchronous Design



Melanie Berg, MEI Technologies in support of NASA/GSFC

Presented by Melanie Berg at Radiation and its Effects on Components and Systems (RADECS), Biarritz, France, September 24-28, 2012 and published on radhome.gsfc.nasa.gov and nepp.nasa.gov.

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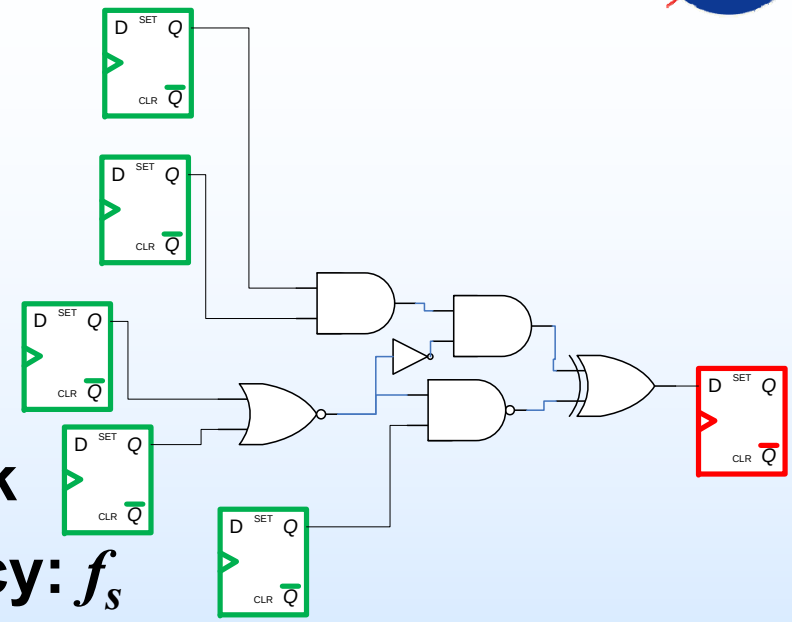
Contact Information:

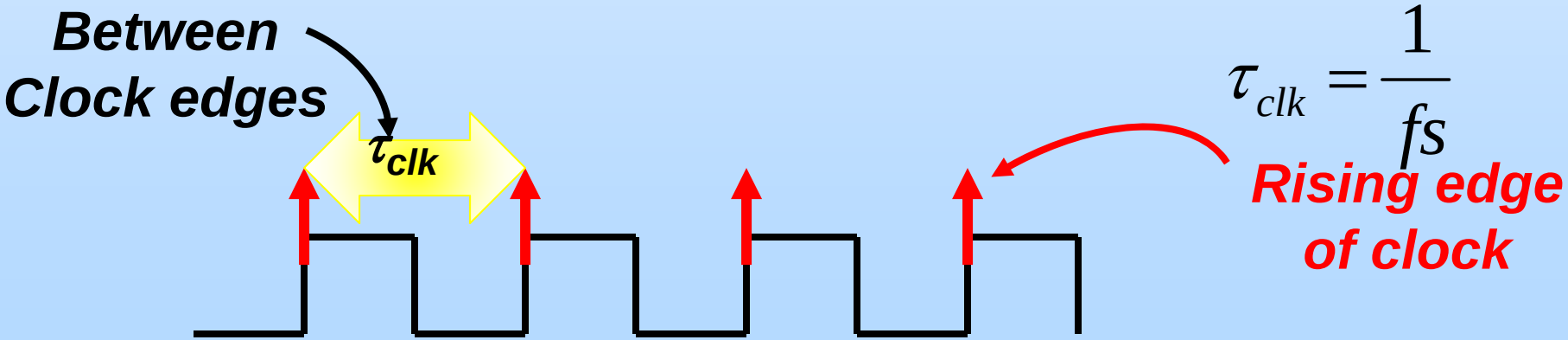
Melanie Berg: NASA Goddard REAG FPGA Principal Investigator:

Melanie.D.Berg@NASA.GOV

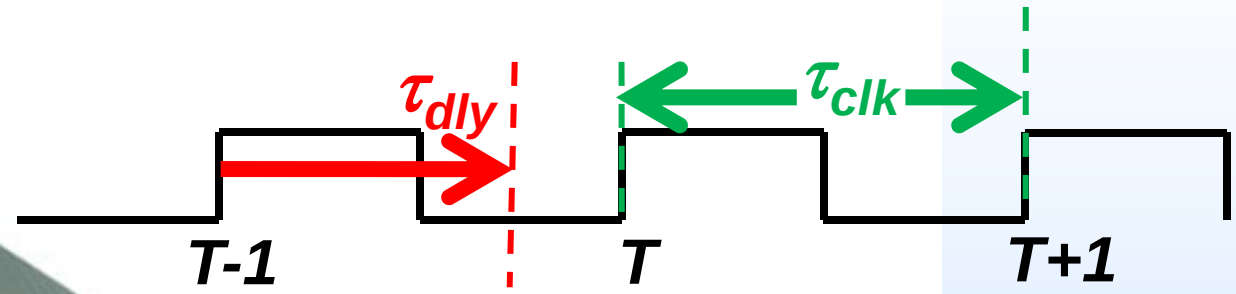
Background: Synchronous Design Data Path



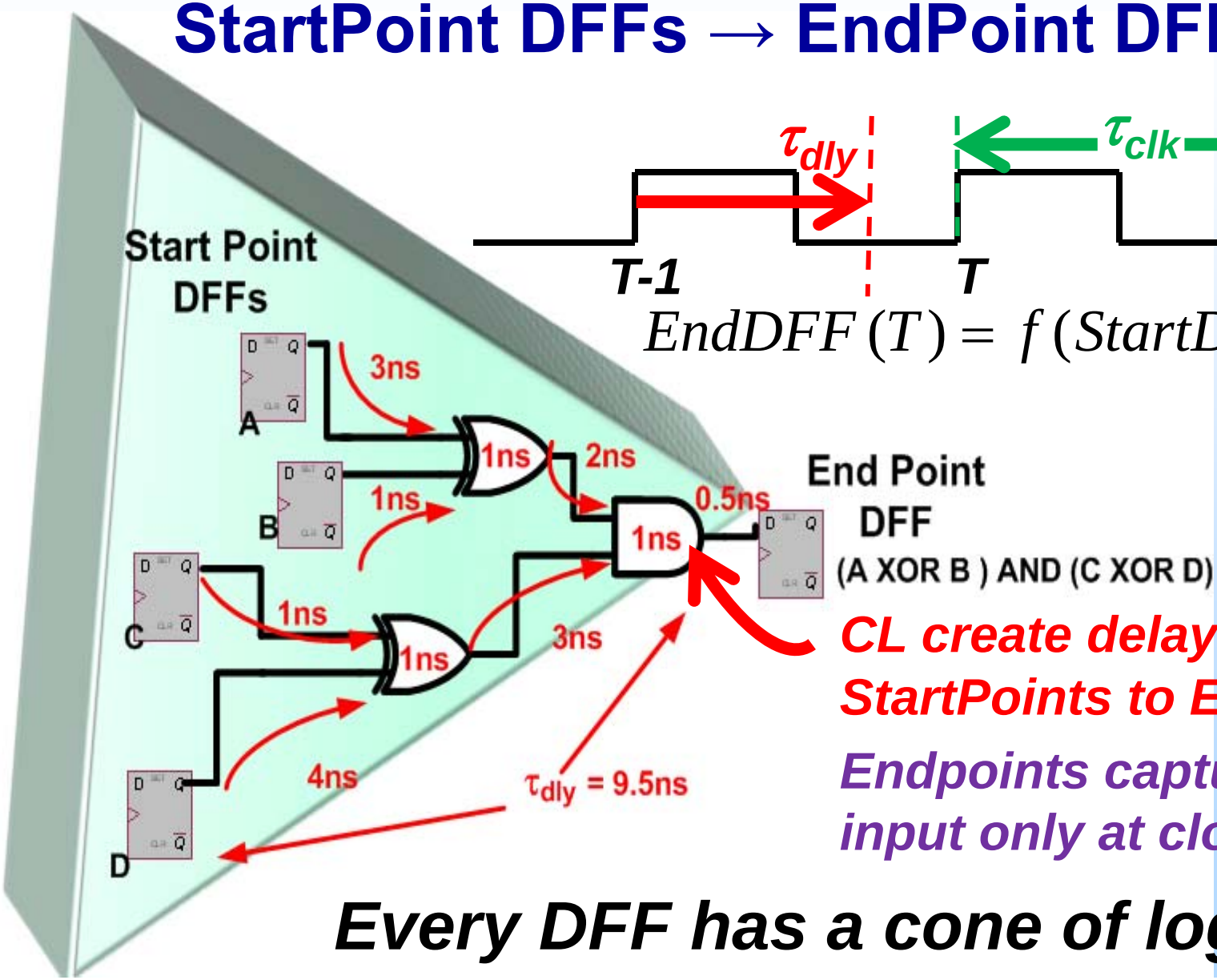
- **Designs are comprised of:**
  - **Combinatorial Logic (CL)**
  - **Edge Triggered Flip-Flops (DFFs)**
  - **Clocks and resets**
- **All DFFs are connected to a clock**
- **Clock period: τ_{clk}; Clock frequency: f_s**
- ***Combinatorial Logic: Compute between clock edges***
- ***DFFs: Hold (or sample) at the rising edge of a clock***



Background: Synchronous System Data Paths:
StartPoint DFFs → EndPoint DFFs



$$EndDFF(T) = f(StartDFFs(T-1))$$



CL create delay (τ_{dly}) from StartPoints to EndPoints

Endpoints capture data input only at clock edge

Every DFF has a cone of logic

Background: NASA REAG's Approach to Error Rate Prediction in a Synchronous Data Path

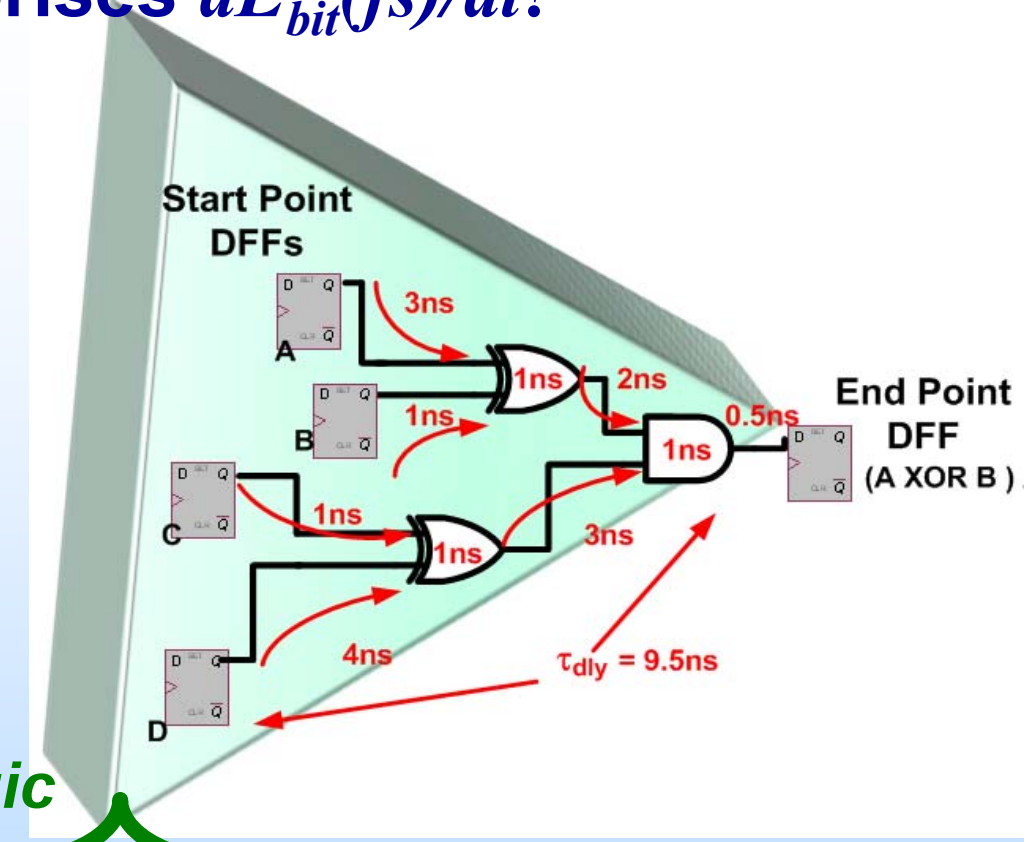
- **A goal of FPGA Single Event Upset (SEU) testing is to provide error rate (*dE(fs)/dt*) predictions to critical missions**
- **Depending on the FPGA type, calculations are performed with respect DFFs or configuration memory bits**
- ***dE(fs)/dt* for FPGA devices are calculated using :**

System upset rate ***SEU bit upset rate*** ***Number of used Bits in the design***

$$\frac{dE(fs)}{dt} < \frac{dE_{bit}(fs)}{dt} * (\#UsedBits)$$

This presentation focuses on data path $dE_{bit}(fs)/dt$ (for DFFs)

How can a DFF Contain an Incorrect State?
…or What Comprises $dE_{bit}(fs)/dt$?



Evaluate Each DFF as an EndPoint

DFF_k Cone of Logic

$\exists_{DFF}$ ***EndPoint DFF SEUs*** + ***StartPoint DFF SEUs*** + ***CL SETs (Single Event Transients)***

$\alpha P(fs)_{DFFSEU}$

DFF upsets that occur at the clock edge

$\beta P(fs)_{DFFSEU}$

DFF upsets that occur between clock edges

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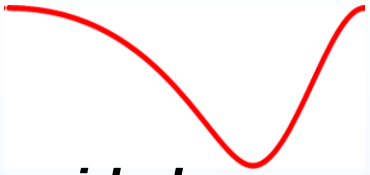
Overview

SET: 

Double sided current spike

EndPoint

StartPoints

Combinatorial Logic

$$\sum_{k=1}^{\#EndPoint\ DFFs} P_{logic(k)} * \left(\alpha P(fs)_{DFFSEU(k)} + \sum_{j=1}^{\#StartPoint\ DFFs} \left(\beta P_{DFFSEU(J)} (1 - \tau_{dly(j)} fs)) * P_{logic(j)} \right) + \sum_{i=1}^{\#CL} (P_{gen_{(i)}} * P_{prop_{(i)}} * P_{logic_{(i)}} * \tau_{width_{(i)}} fs) \right)$$

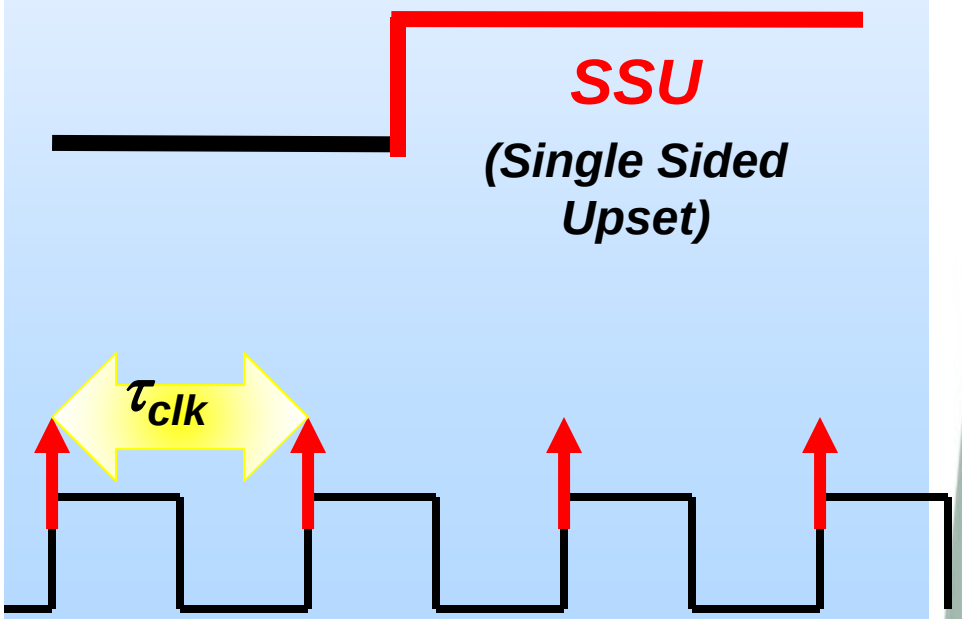
Probabilities:

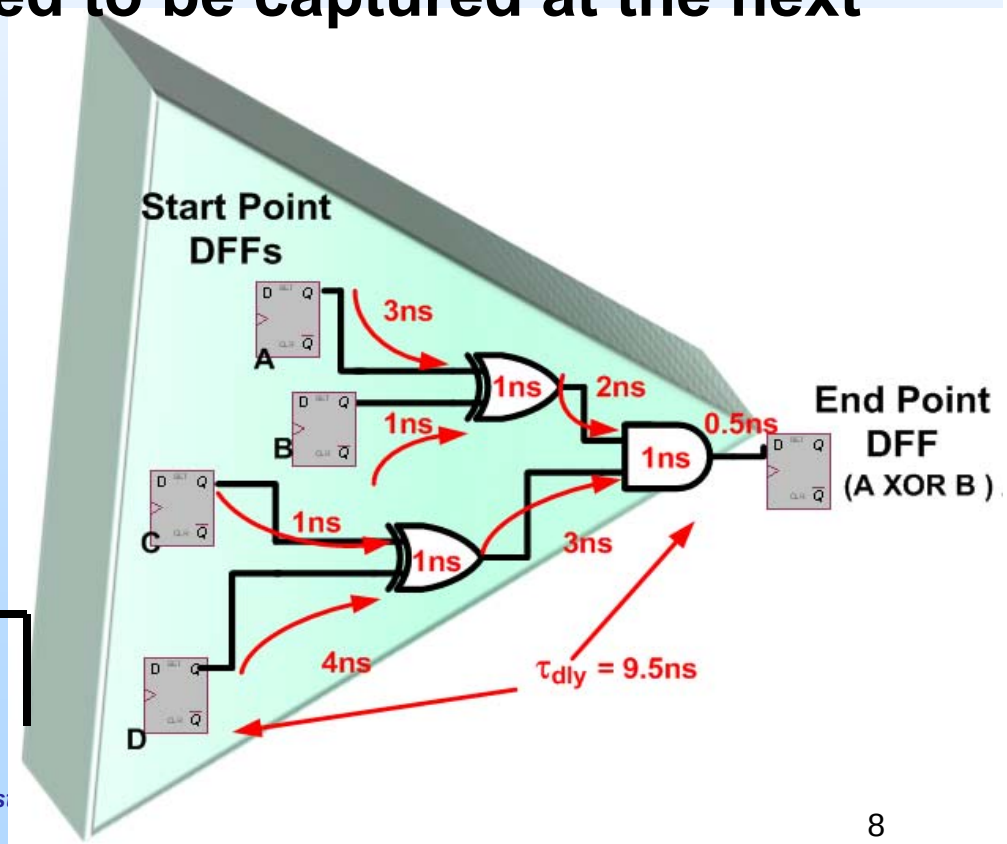
- $P_{logic(k)}$ ➔ ***EndPoint Logic Masking***
- $P_{logic(j)}$ ➔ ***StartPoint Logic Masking***
- $P_{logic(i)}$ ➔ ***Combinatorial Logic Masking***
- P_{DFFSEU} ➔ ***DFF Upset***
- $P_{prop(i)}$ ➔ ***Electrical Masking***
- $P_{gen(i)}$ ➔ ***SET generation***

τ_{width} ***= average width of SET***

SEUs Generated Internally to DFFs ($P(fs)_{DFFSEU}$)

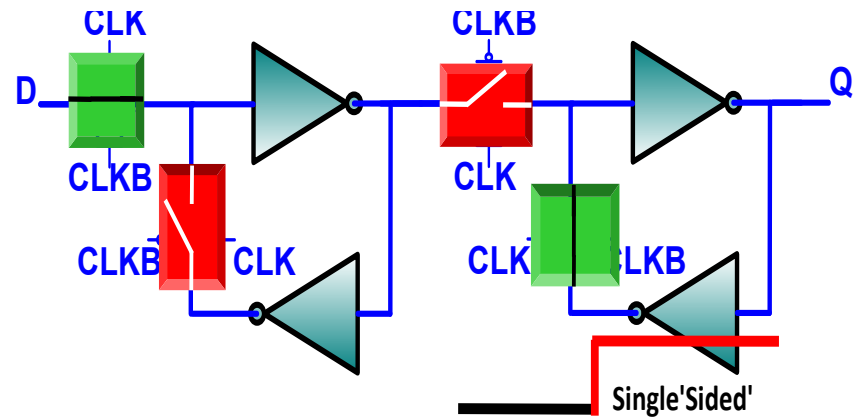
- We categorize upsets generated internal to DFFs
  - Upsets occur at the clock edge – analyzed as EndPoint upsets (already captured into system state)
  - Upsets generated between rising clock edges-analyzed as StartPoint upsets (need to be captured at the next clock edge)



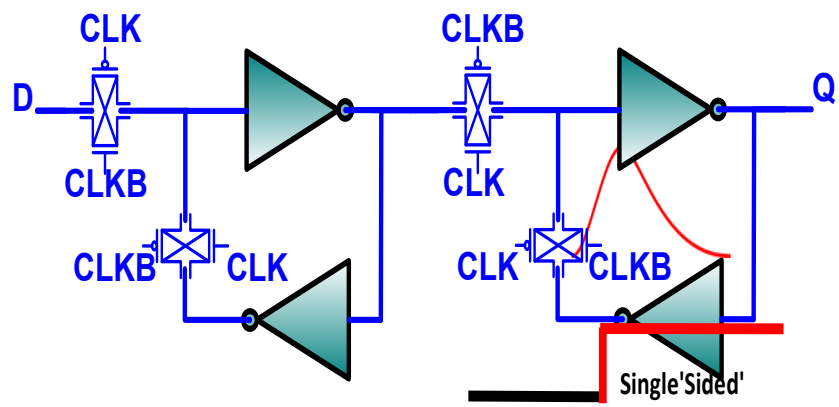


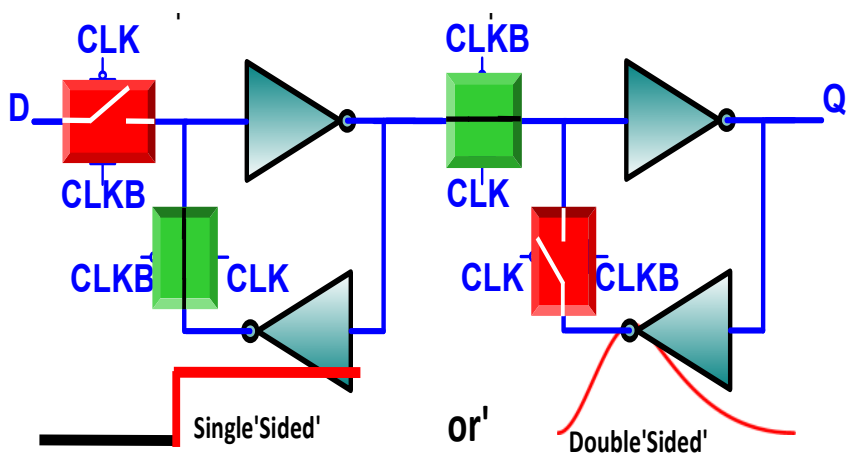
DFF SEUs: Can Occur at a Clock Edge or Between Rising Clock Edges

Low: SSU generated in Slave

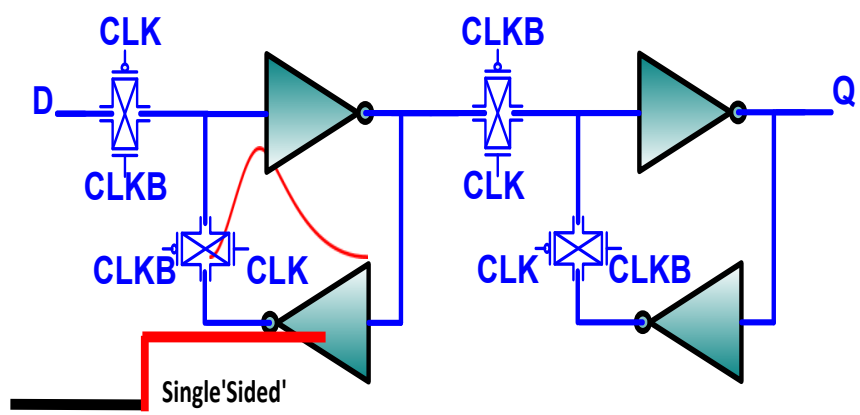


High→Low: Slave Captures its SET





High: SSU generated in Master; or SET in Slave



Low→High: Master Captures its SET

Summary of Internal DFF SEUs

$$P(fs)_{DFFSEU} = \alpha P(fs)_{DFFSEU} + \beta P_{DFFSEU} + P(fs)_{DFFSET}$$

Percentage of single sided upsets that occur at clock edge (low to high)

- **Frequency dependent: Master SET gets trapped during transition from transparent to hold state (rising edge of clock)**
- **This is considered a state change**

Percentage of single sided upsets that occur between clock edges

- ***Not Frequency dependent: Master or slave is in hold state***
- ***This is not considered a definitive state change***

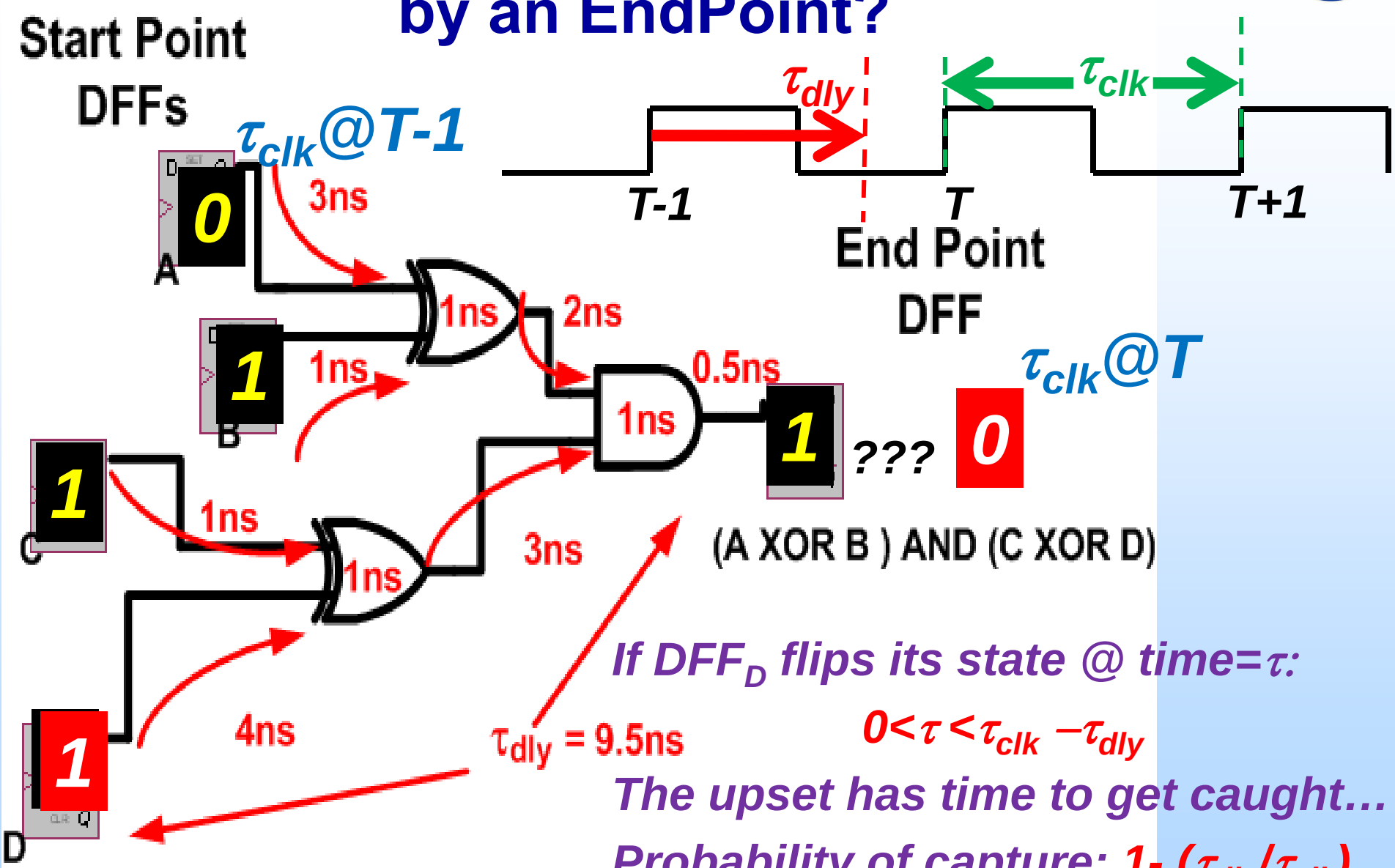
SETs generated in slave when clock is high

- ***Frequency dependent***

EndPoint SEU

StartPoint SEU

How Does a StartPoint SEU get Captured by an EndPoint?



If DFF_D flips its state @ time=τ:

$0<\tau<\tau_{clk}-\tau_{dly}$

The upset has time to get caught…

Probability of capture: 1- (τ_{dly}/τ_{clk})

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Details of Capturing StartPoint DFFs

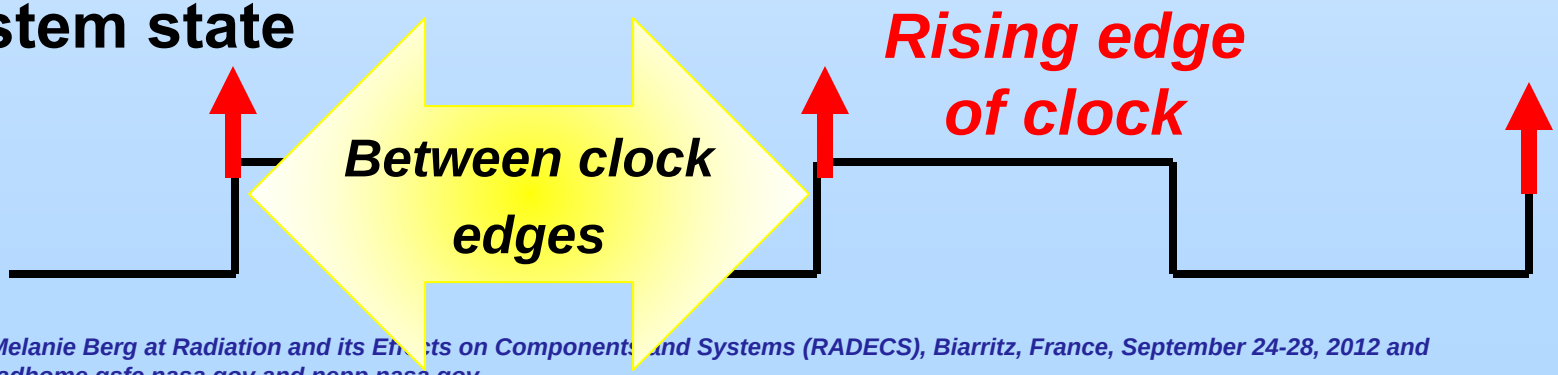
$$\exists_{DFF}\left(\left(\sum_{j=1}^{\#StartPoint\,DFFs} \beta P_{DFFSEU(j)}(1-\tau_{dly(j)}fs)P_{logic(j)}\right)\right)$$

Upset generated internally to DFF between clock edges

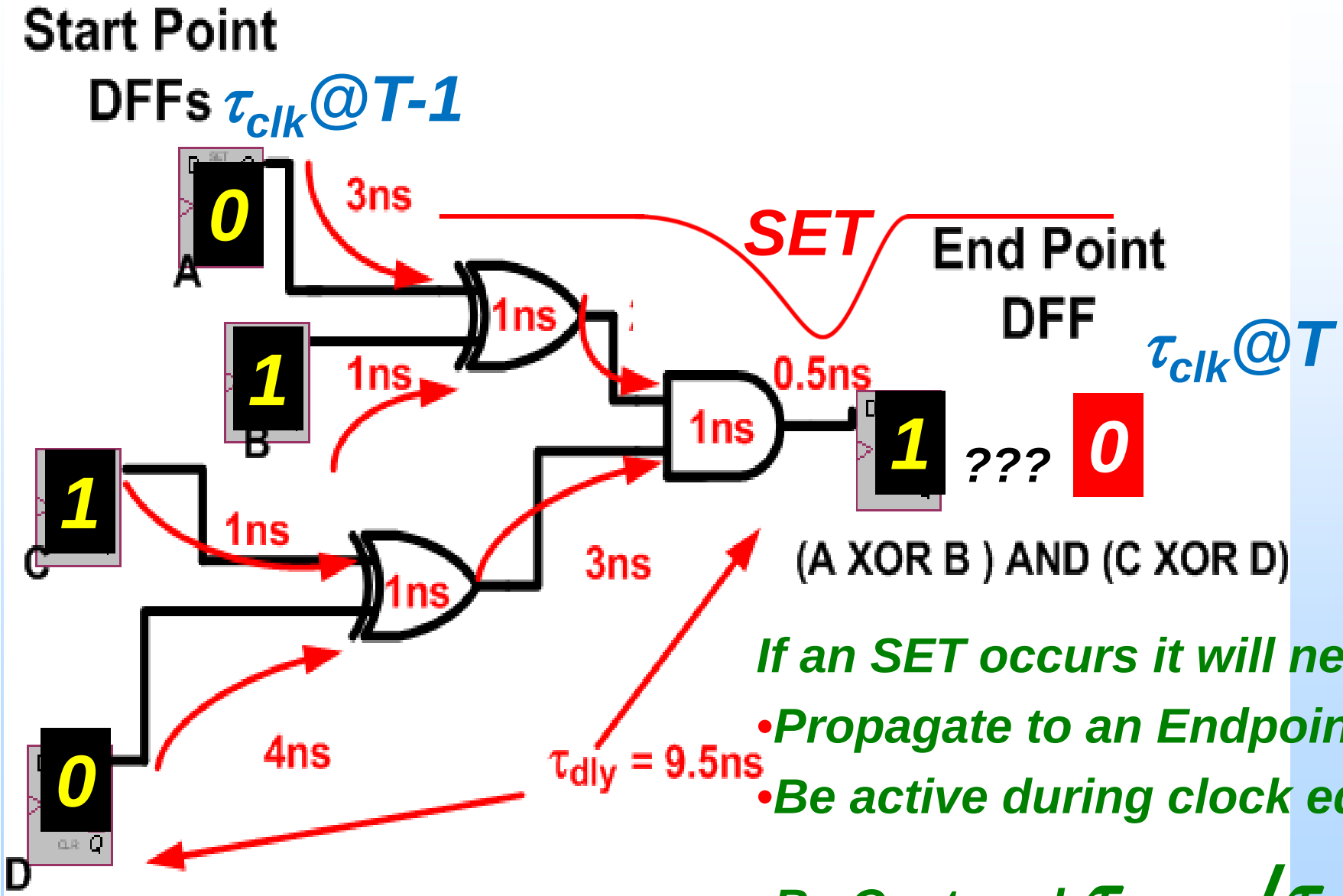
Capture

Logic Masking

- **SEU generation occurs in a StartPoint between rising clock edges (βP_{DFFSEU})**
- **Will need to be captured by an EndPoint to affect the system state**



Synchronous System: CL SET Capture

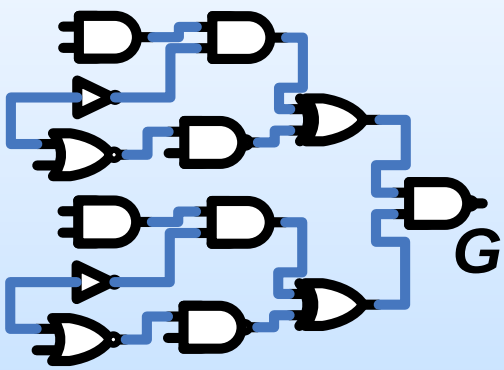


If an SET occurs it will need to

- *Propagate to an Endpoint*
- *Be active during clock edge*
- *Be Captured τ_{width}/τ_{clk}*

Details of Combinatorial Logic SET Capture

$$\exists_{DFF}\left(\sum_{i=1}^{\#Combinatorialcells}(P_{gen(i)}P_{prop(i)}P_{logic}\tau_{width(i)}fs)\right)$$



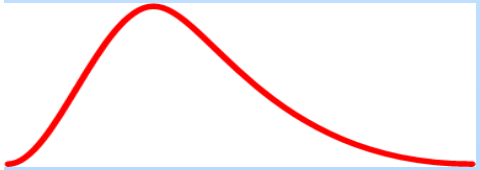
CL

Generation

Propagation

Logic Masking

Capture



Double Sided

- SET Generation (P_{gen}) occurs between clock edges
- SET Capture occurs at a clock edge

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Putting it All Together: What Do We Expect from Our Data?

$$\sum_{k=1}^{\#EndPoint\ DFFs} P_{logic(k)} * \left(\alpha P(fs)_{DFFSEU(k)} + \sum_{j=1}^{\#StartPoint\ DFFs} \left(\beta P_{DFFSEU(J)} (1 - \tau_{dly(j)} fs)) * P_{logic(j)} \right) + \sum_{i=1}^{\#CL} (P_{gen_{(i)}} * P_{prop_{(i)}} * P_{logic_{(i)}} * \tau_{width_{(i)}} fs) \right)$$

EndPoint

EndPoint Logic Masking

StartPoints

Combinatorial Logic

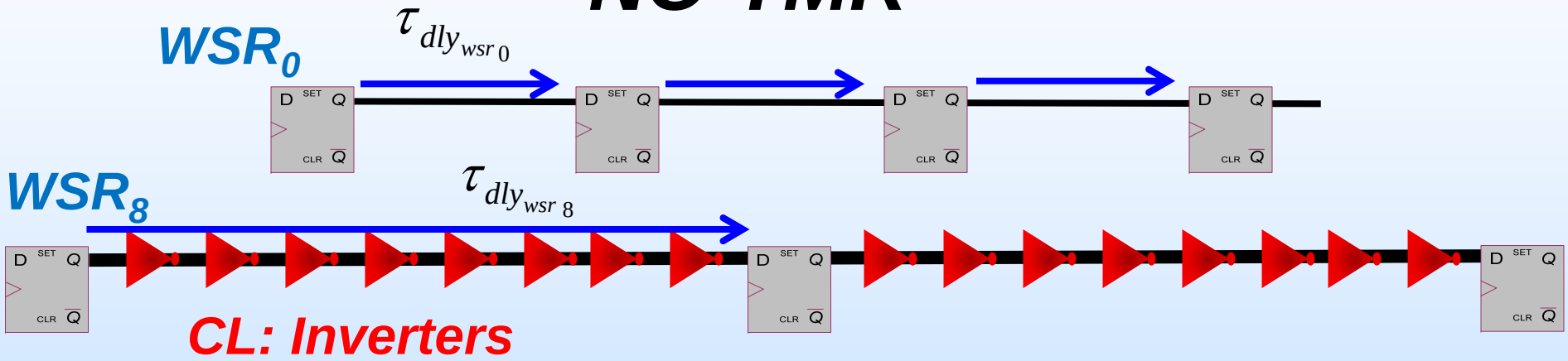
- **EndPoint DFFs: Directly proportional to frequency**
- **StartPoint DFFs: Inversely proportional to frequency**
- **Combinatorial Logic: Directly proportional to frequency**

Helps us study trends. Used to better extrapolate radiation data for characterizing real designs

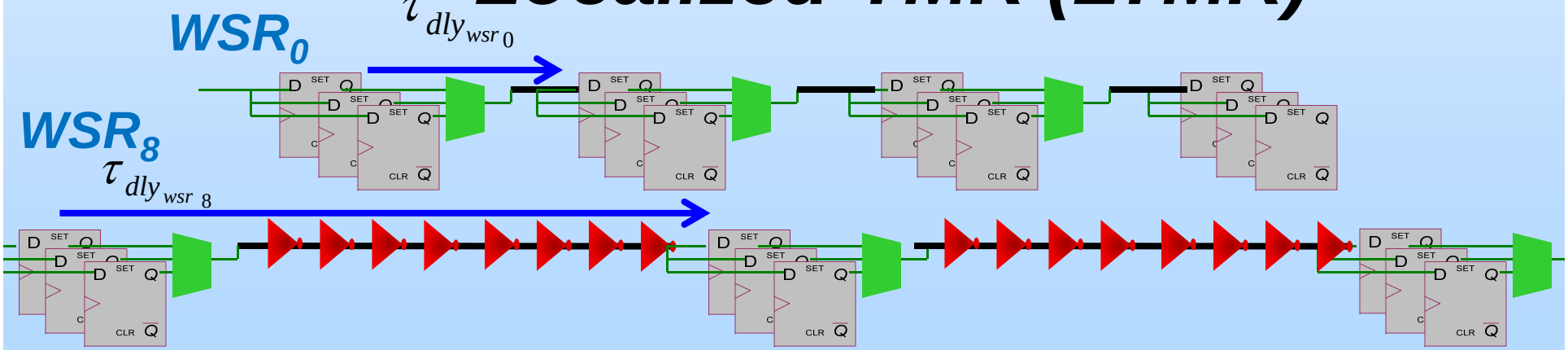
Radiation Test Structures: Windowed Shift Registers (WSR) and Triple Modular Redundancy (TMR)

$$\tau_{dly_{wsr\ 8}} > \tau_{dly_{wsr\ 0}}$$

NO-TMR



Localized-TMR (LTMR)



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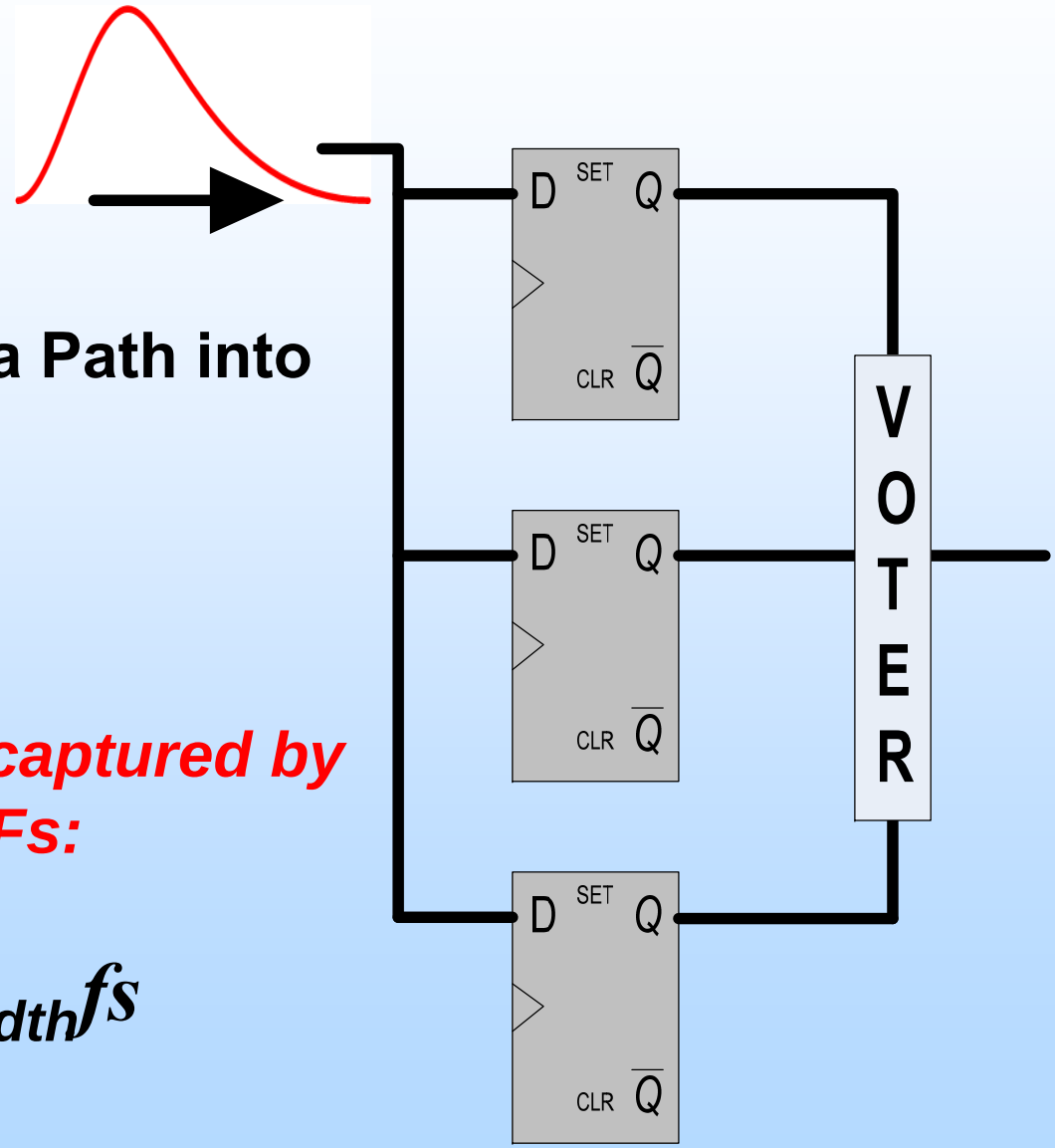
LTMR Failure



- **SETs from Shared Data Path into DFFS**
- **Voters can upset**

Data path SETs can be captured by the LTMR'd DFFs:

$$P_{gen} P_{prop} P_{logic} \tau_{width} fs$$

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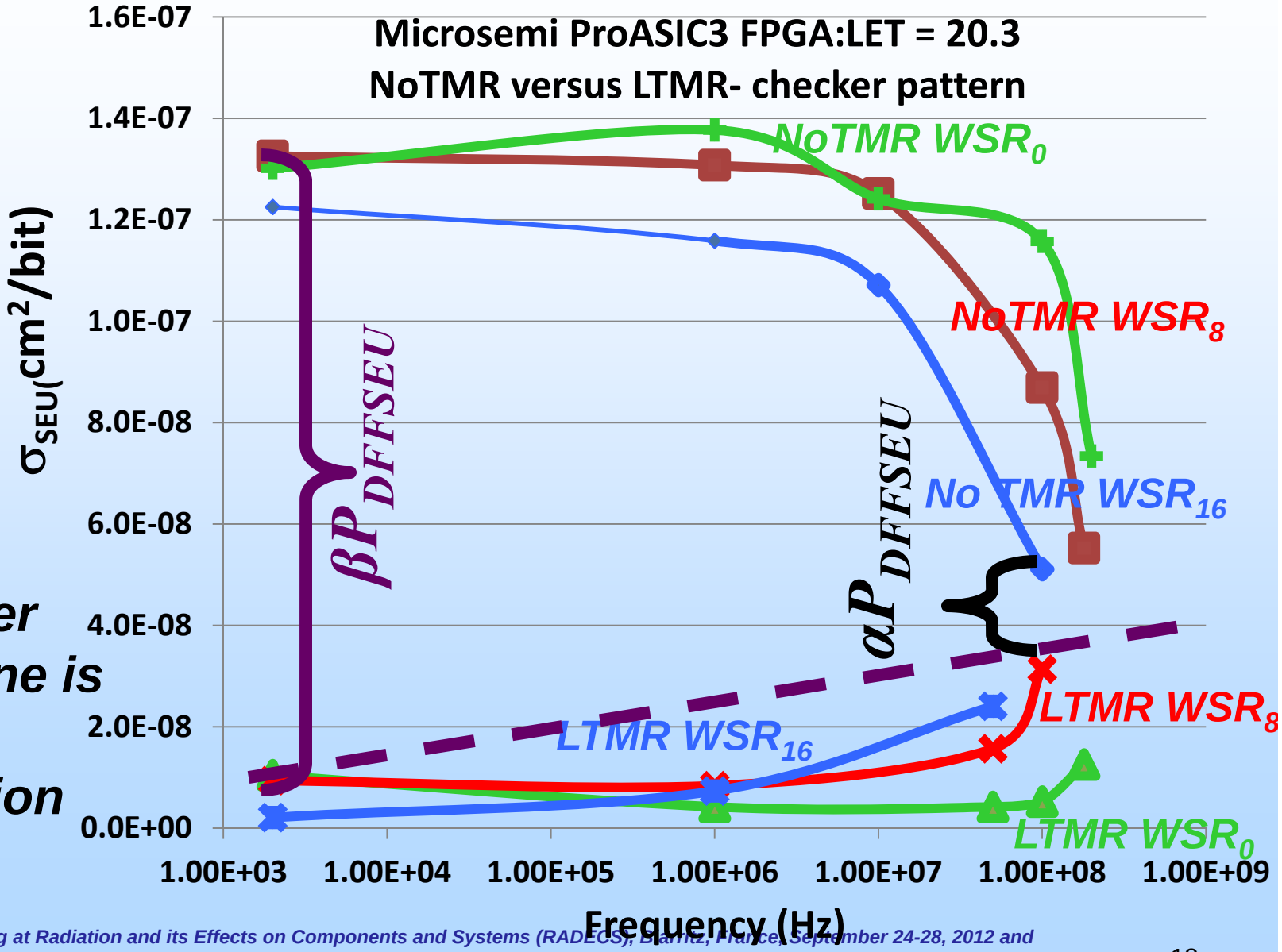
Using the Model+Data to Analyze StartPoint and EndPoint SEUs



Area under dashed line is SET contribution

Conclusions

- **NASA Goddard REAG has developed a model to characterize upsets in synchronous designs.**
- **The characterization for the functional data path has been presented**
- **Contrary to conventional theory, frequency effects are shown for DFFs (EndPoints). However the model was used to empirically determine, for this technology, that EndPoint frequency effects are insignificant**

$$\sum_{k=1}^{\#EndPoint\ DFFs} P_{logic(k)} * \left(\alpha P(fs)_{DFFSEU(k)} + \sum_{j=1}^{\#StartPoint\ DFFs} \left(\beta P(fs)_{DFFSEU(J)} (1 - \tau_{dly(j)} fs) \right) * P_{logic(j)} \right) + \sum_{i=1}^{\#CL} \left(P_{gen_{(i)}} * P_{prop_{(i)}} * P_{logic_{(i)}} * \tau_{width_{(i)}} fs \right) \Bigg)$$