Single-Event and Total Dose Testing for Advanced Electronics

Jonathan A. Pellish

NASA Goddard Space Flight Center
Greenbelt, MD USA

16 July 2012

This work was sponsored in part by the NASA Electronic Parts and Packaging program and the Defense Threat Reduction Agency.

www.nasa.gov

Presented by J. A. Pellish at the 2012 Institute of Electrical and Electronics Engineers (IEEE) Nuclear and Space Radiation Effects Conference (NSREC), July 16-20, 2012, in Miami, FL USA and published on http://nepp.nasa.gov/.
AR 1520’s X1.4 Flare and CME

2012 NSREC Gets a $K_p = 6$ Geomagnetic Storm

Left image captured with the NASA Solar Dynamics Observatory’s Atmospheric Imaging Assembly
http://aia.lmsal.com/

SINGLE-EVENT AND TOTAL DOSE TESTING FOR
ADVANCED ELECTRONICS
CME’s Projected Impact to Earth

Simulations from NASA/GSFC Integrated Space Weather Analysis System
http://iswa.ccmc.gsfc.nasa.gov/iswa/iSWA.html
Introduction

• Describe what we mean by advanced electronics and how they relate to flight projects
• Review the natural space radiation environment
• Cover the impacts of the space radiation environment on advanced electronics
• Discuss evaluation methods for total ionizing dose (TID) degradation in advanced electronics – not going to focus on displacement damage dose (DDD)
• Discuss evaluation methods for single-event effects (SEE) in advanced electronics
The Landscape Is Always Changing…

The missing memristor found


IEF2011: HP to replace flash and SSD in 2013

David Manners
Thursday 06 October 2011 12:17


HP intends to have an alternative technology to flash on the market in eighteen months, an alternative to DRAM in three to four years and, following DRAM, a replacement for SRAM. Stan Williams, Senior Fellow at HP, told the IEF2011 meeting in Seville this morning.

"We're planning to put a replacement chip on the market to go up against flash within a year and a half," said Williams, "and we also intend to have an SSD replacement available in a year and a half."

"In 2014 possibly, or certainly by 2015, we will have a competitor for DRAM and then we'll replace SRAM."

http://www.japantimes.co.jp/text/nb20120228n1.html

DDR4 makes its debut at ISSCC 2012

Servers in 2013, desktops the coming year

23 Feb 2012 18:47 | by Paul Taylor in Lisbon | Filed in Chips, Samsung, DDR3

http://news.techeye.net/chips/ddr4-makes-its-debut-at-isscc-2012

http://www.japantimes.co.jp/text/nb20120228n1.html

Where We’re Going…

<table>
<thead>
<tr>
<th>THEN</th>
<th>NOW</th>
</tr>
</thead>
<tbody>
<tr>
<td>Magnetic core memory</td>
<td>NAND flash, resistive random access memory (RAM), magnetic RAM,</td>
</tr>
<tr>
<td></td>
<td>phase-change RAM, phase-change RAM, programmable metallization cell</td>
</tr>
<tr>
<td></td>
<td>RAM, and double-data rate (DDR) synchronous dynamic RAM (SDRAM)</td>
</tr>
<tr>
<td>Single-bit upset (SBU) and single-event</td>
<td>Multiple-bit upset (MBU), block errors, single-event functional</td>
</tr>
<tr>
<td>events (SETs)</td>
<td>interrupts (SEFIs), frequency-dependence, etc.</td>
</tr>
<tr>
<td>Heavy ions and high-energy protons</td>
<td>Heavy ions, high- and low-energy protons, delta rays, muons, ???</td>
</tr>
<tr>
<td>Radiation hardness assurance (RHA)</td>
<td>RHA what?</td>
</tr>
</tbody>
</table>
Where We’re Going…

Increases in capability introduce additional evaluation challenges

- FinFETs/Tri-gate devices
- Nanowire MOSFETs
- Organic transistors
- Ultra-thin body SOI

- Ge MOSFETs
- III-V MOSFETs
- Carbon nanotube FETs
- GaN, SiC,…

TESTABILITY
Two General Types of Electronics for Space Use

• Commercial-off-the-shelf (COTS) electronics
  o Designed with no attempt to mitigate radiation effects. COTS can refer to commodity devices or to application-specific integrated circuits (ASICs) designed using a commercially available design system.

• Radiation-tolerant electronics
  o Designed explicitly to account for and mitigate radiation effects by process and/or design

Examples from Space Electronics

- **COTS**
  - Random access memory
  - Flash memory and other non-volatile solutions
  - Data converters
  - High-speed amplifiers
  - Digital signal and multi-core processors
  - Field programmable gate arrays (FPGAs)

- **Radiation-Tolerant**
  - RHBD + RHBP using boutique foundries
    - Including pre-processed wafer starting materials
  - RHBD applied to AMS, IBM, Jazz, ONSemiconductor, or TSMC bulk or SOI complementary metal oxide semiconductors (CMOS)
  - Data converters, FPGAs, memory devices, logic, etc.

AMS = AustriaMicroSystems
TSMC = Taiwan Semiconductor Manufacturing Co.; SOI = silicon-on-insulator
RHBD = radiation-hardened by design; RHBP = radiation-hardened by process
Space Environment –
*Particle sources and abundance*
• Deep-space missions may also see neutrons and gamma rays from background or radioisotope sources
Solar Modulation

- 11- and 22-year solar activity cycles
  - 7 active years; 4 quiet years; polarity switch → 22-year cycle total
- Primarily affects cosmic rays and solar particles; not trapped particles

Data from the Solar Influences Data Analysis Center; http://sidc.oma.be/index.php
Galactic Cosmic Rays (GCRs)

- Originate outside the solar system (e.g., supernovae)
- Include all naturally-occurring elements
  - Drops off rapidly for Z > 26 (iron)
- Most energetic of all space environment radiation


https://creme.isde.vanderbilt.edu/

Solar Particle Events

Severe proton events from cycles 20-22

- Solar flares & coronal mass ejections (CMEs)
  - Impulsive vs. gradual; magnetic field vs. plasma eruption
- CMEs primarily responsible for major interplanetary disturbances
- Energies are lower than galactic cosmic rays (GCR)

Trapped Particles

Trapped Particles

- Note the extent of the trapped protons and outer zone electrons, as well as the penetration range of solar flare protons.

- L-value often describes the set of magnetic field lines which cross the Earth's magnetic equator at a number of Earth-radii equal to the L-value.

Trapped Particles – Protons

- Localized to Earth’s geomagnetic field
- Energies up to 100s of MeV
- $> 10$ MeV fluxes
  $\sim 10^5$ cm$^{-2}$ s$^{-1}$
- $L$-shell 1.15 – 10
  - Higher energy protons $< 20,000$ km
- Dipole offset


SPENVIS, http://www.spenvis.oma.be/, v4.6.5
SINGLE-EVENT AND TOTAL DOSE TESTING FOR ADVANCED ELECTRONICS
Trapped Particles – Protons

- South Atlantic Anomaly (SAA) – dominates Earth’s space environment below about 1000 km
- Due to tilt and displacement between rotational and geomagnetic axes

E.J. Daly, et al., IEEE TNS, April 1996.
Effects of Trapped Protons

Solar Anomalous Magnetospheric Explorer (SAMPEX)
Solid State Recorder

SAMPEX was NASA’s first Small Explorers mission


Cosmic Ray Upset Experiment (CRUX)
Advanced Photovoltaic and Electronics Experiment (APEX)

Micron 256k: Altitude: 1750km - 1850km

- Both the South Atlantic Anomaly and proton belts are visible in these on-orbit upset data

Trapped Particles – Electrons

- Localized to Earth’s geomagnetic field
- Energies up to 10 MeV
- > 1 MeV fluxes up to $\sim 10^6 \text{ cm}^{-2} \text{s}^{-1}$
- Two shells – inner and outer
  - Inner: L-shell 1 – 2.8
  - Outer: L-shell 2.8 – $\sim 10$
- Dominant feature for medium Earth orbit and geostationary vehicles


After SPENVIS website, http://www.spenvis.oma.be
Space Environment Impacts –

Radiation effects are caused by the deposition of energy in materials
Ions & Linear Energy Transfer (LET)

Iron in Silicon

LET Spectrum behind 2.5 mm of Aluminum

\[
S = - \frac{dE}{dx} \quad \Rightarrow \quad \text{LET} = \frac{1}{\rho} \frac{dE}{dx}
\]

Stopping power (S), depends on target material; LET does not
Photons Deposit Energy Too

- Incoming particles – electrons, protons, heavy ions, and photons – can deposit energy in semiconductor materials.

\[
1 \frac{\text{J}}{\text{kg}} = 1 \text{ Gy} = 100 \text{ ergs} = 100 \text{ rad}
\]

- Energy becomes “hot” electron-hole pairs


What is Total Ionizing Dose?

• Total ionizing dose (TID) is the absorbed dose in a given material resulting from the energy deposition of ionizing radiation.

• Total ionizing dose results in cumulative parametric degradation that can lead to functional failure.

• In space, caused mainly by protons and electrons.

Examples

<table>
<thead>
<tr>
<th>Metal Oxide Semiconductors Devices</th>
<th>Bipolar Devices</th>
</tr>
</thead>
<tbody>
<tr>
<td>Threshold voltage shifts</td>
<td>Excess base current</td>
</tr>
<tr>
<td>Increased off-state leakage</td>
<td>Changes to recombination behavior</td>
</tr>
</tbody>
</table>
Total Ionizing Dose

Fractional Hole Yield by Particle Type

Processes Involved in TID Damage

- Caused by the energy deposition of protons, electrons, energetic heavy ions, and photon-material interactions — *focused on insulators*

- Holes build up in deep traps and interface traps, which are manifest as electrical changes in device performance

What are Single-Event Effects?

- A single-event effect (SEE) is a disturbance to the normal operation of a circuit caused by the passage of a single ion through or near a sensitive node in a circuit.
- SEEs can be either destructive or non-destructive.

Examples

<table>
<thead>
<tr>
<th>Non-Destructive</th>
<th>Destructive</th>
</tr>
</thead>
<tbody>
<tr>
<td>Single-Event Upset (SEU)</td>
<td>Single-EventLatchup (SEL)</td>
</tr>
<tr>
<td>Multiple-Bit Upset (MBU)</td>
<td>Single-Event Burnout (SEB)</td>
</tr>
<tr>
<td>Single-Event Transient (SET)</td>
<td>Single-Event Gate Rupture (SEGR)</td>
</tr>
<tr>
<td>Single-Event Functional Interrupt (SEFI)</td>
<td></td>
</tr>
</tbody>
</table>

Single-Event Effects Processes

Short History of Single-Event Effects

After S. Buchner, SERESSA 2011 Course, Toulouse, France.


• First observation of SEUs on earth was in 1978. Observed in RAM caused by the alpha particles released by U and Th contaminants within the chip packaging material and solder. Vendors took specific actions to reduce it. T. C. May and M. H. Woods, "A New Physical Mechanism for Soft Errors in Dynamic Memories", Proceedings 16 Int'l Reliability Physics Symposium, p. 33, April, 1978.


Evaluation of Total Ionizing Dose in Advanced Electronics –
*Tolerance has gotten better, but device complexity increases faster*
How do you approach radiation testing advanced electronics?

Radiation testing protocols for advanced electronics

Engineering Characterization

Hardness Assurance
Common TID Testing Themes

- Difficulty of in-situ evaluation
  - “Test as you fly” implies application realism
- Component complexity creates “black boxes”
  - Does my test lack sensitivity/specificity?
  - Could refer to discrete devices or integrated circuits
- Component material systems now comprise most of the periodic table (equilibrium, dose enhancement,…)
- Existing test methods for bounding predictions rely on well-behaved results and controlled starting materials
  - Bimodal degradation/failure distributions
  - Part-to-part and lot-to-lot variability of commercial devices

“Lot” can be defined as the manufacturing or wafer/diffusion lot depending on context.
TID Testing

• Why do TID testing?
  o To determine the type and magnitude of parametric degradation and check for functional failures
  o To calculate the suitability for a radiation environment

• TID testing is carried out with an ionizing radiation source
  o Photons: $^{60}$Co, $^{137}$Cs, and ARACOR x-ray sources
  o Electrons: LINAC and Van de Graaff accelerators
  o Protons: cyclotron and Van de Graaff accelerators

• Limited device preparation required in most cases
Available TID Test Methods

- Qualification methods that define total ionizing dose testing of microelectronics:
  - MIL-STD-883, Test Method 1019 used in the US
  - ESCC Basic Specification No. 22900 used in Europe

- Specific methods cover radiation hardness assurance – this is *qualification*
  - Can be adapted for engineering characterization

- Both of the above methods have procedures to test for and measure enhanced low-dose-rate sensitivity (ELDRS), which can affect some types of bipolar/BiCMOS devices and integrated circuits
ELDRS Effects in Bipolar Devices

- First observed in bipolar devices and circuits in the early 1990s
- Amount of total dose degradation at a given total dose is greater at low dose rates than at high dose rates
  - True dose-rate effect as opposed to a time-dependent effect

\[ I_{B^+} \text{ vs. Total Dose for LM111 Voltage Comparators} \]

Steps to Perform a TID Test

Based on MIL-STD-883 Method 1019

Some Issues With $^{60}$Co & X-Rays

- Practical terms: x-rays get absorbed more readily than gamma rays. For example, in aluminum:
  - 50% attenuation @ 1 mm for x-rays and 5 cm for $\gamma$-rays


Photon Effects

Photon Cross Sections in Aluminum

NIST XCOM Database; http://www.nist.gov/pml/data/xcom/index.cfm
In-Situ Evaluation

- Can be difficult to route high-bandwidth and/or low-voltage signals long distances
- Can consider other irradiation sources

Black Box Components

Samsung DDR2 SDRAM

- Behavior indicates that failure dose not well correlated to observed degradation
- How do you track/predict potential failures?


Component Variability

- Components used are illustrative – many examples exist
- Bimodality complicates analysis and limits confidence

LM111 Voltage Comparator at 50 krad(SiO₂)

OP484 Quad Op Amp at 100 krad(SiO₂)


Component Variability

- **Sources of variability**
  - Process: defects, die position on wafer, implants
  - Design: how much margin is left?

LM111 Voltage Comparator at 50 krad(SiO₂)

OP484 Quad Op Amp at 100 krad(SiO₂)


Bayesian Analysis Approach

In this case, “lot” is the wafer or diffusion lot, not the packaging or manufacturing lot.

Possible TID Testing Solutions

Device complexity and dose rate sensitivity complicate TID evaluation and qualification

• Explore feasibility of non-photon radiation sources in some cases
• Develop flexible interrogation methods for advanced, large-scale integration devices
• Increase lot test size to maximum practical extent
• Leverage as much existing data as possible
• Track basic mechanisms research to maintain knowledge base on advanced material systems and latest simulation techniques
Evaluation of Single-Event Effects (SEE) in Advanced Electronics –
The death of averages
How do you approach testing advanced electronics?

Radiation testing protocols for advanced electronics

- Engineering Characterization
- Hardness Assurance
SEE Complexity


*These pictures are what got me into radiation effects.*
Common SEE Testing Themes

• Difficulty of in-situ evaluation
  o “Test as you fly” implies application realism

• Component complexity creates expensive “black boxes”
  o Many operational modes and on-board smarts
  o Test costs are spiraling upwards – “full” characterization no possible

• Advanced electronics have lead to:
  o Enhanced angular sensitivity due to process or design techniques
  o Sensitivity to low-energy protons and ??? (e.g., muons and delta rays)

• Parameter space is HUGE
  o How do you evaluate an integral with 10s or 100s of dimensions?
SEE testing

• Why do testing?
  1. To **determine the presence and characteristics** of single events
     » Destructive or non-destructive
     » Voltage and temperature dependence
     » Amplitude and width of SETs
  2. To **calculate the SEE rate** for a radiation environment

• SEE testing is usually done at **accelerator facilities**, which irradiate the whole device with ions. Some in **air** and some in **vacuum**.

• Package must be opened, de-processed, thinned…

• Other testing methods that provide spatial and temporal information include:
  o **Focused, collimated ion beam**
  o **Focused, pulsed laser beam**

After S. Buchner, SERESSA 2011 Course, Toulouse, France.
Available SEE Test Methods

• Test guideline documents that define SEE testing of microelectronic devices and circuits (last update):
  o ASTM F1192 (08/2006)
  o ESCC Basic Specification No. 25100 (10/2002)
  o JEDS57 (12/1996)
  o JESD89 (10/2007; Reaffirmed 01/2012)
  o MIL-STD-750, Test Method 1080 (01/2012)

• Do a reasonable job of defining procedures for heavy ion testing – HOWEVER…
  o Do not cover recently documented effects (e.g., angular sensitivities, heavy ion indirect ionization) or proton SEE
Steps to Perform a SEE Test

• Understand device process technology and application conditions – SEE testing is most always application-specific
  o Could the device under test be susceptible to destructive effects?
  o Is there a target environment for qualification (requirements) or is the test an engineering characterization?

• Identify a suitable test facility and consider systematic variables
  o Ion selection, pulsed laser sources, energy range, flux range, dosimetry, beam profile and purity, and accelerator technology

• Develop a test matrix that covers necessary application space within allowable costs – the following can have large ranges
  o Device function, data patterns, frequency, voltage/current, temperature, LET, energy, particle range, etc.

• Prepare devices for irradiation and travel to the test facility
Steps to Perform a SEE Test

• The majority of time before, during, and after a SEE test is spent
  1. Deciding what you want to measure and how;
  2. Verifying you can do 1.; and,
  3. Figuring out what you actually got.

• Because SEE testing is real-time, many aspects are dynamic, so contingency planning is essential

• Always have a backup plan
Device Preparation

- Thinning and polishing for backside irradiation is not trivial
- As with any commercial technology, destructive effects are always a concern – statistics?!?
- Repeatability concerns from lot-to-lot (packaging)

1 Gbit DDR2 SDRAM Die

Note cracks at edge

In-Situ Evaluation

High-Speed Test Fixture

IBM 5AM SiGe HBTs

• Special considerations for angle, bandwidth, and proton activation

• Similar approach with FPGA-based testers

Tilt \textit{and} Roll Angle Sensitivities

\[ \Omega = 2\pi \left[ 1 - \cos \left( \frac{a}{2} \right) \right] \]

- 90 nm CMOS, RHBD Latch

Device Sensitive Volumes


Tilt and Roll Angle Sensitivities

32 nm SOI CMOS latch cross sections – contours are based on data & simulation

<table>
<thead>
<tr>
<th>15 MeV/amu Xenon</th>
<th>Soft Latch</th>
<th>Stacked Latch (side-by-side)</th>
<th>Stacked Latch (end-to-end)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Relative Cross Section</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1.0</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0.9</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0.8</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0.6</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0.5</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0.4</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0.3</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0.1</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0.0</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>


- Non-destructive SEE continue to be the most difficult aspect of advanced CMOS radiation effects
  - Varied angular sensitivity (test considerations)
Low-Energy Proton Sensitivity

IBM 65 nm SOI SRAM – top-side irradiation

- First published low-energy proton soft errors in 2007
- Energy below Coulomb barrier – interactions are constrained to electromagnetic and nuclear elastic reactions
- Rapid cross section increase at grazing angles and energies below 2 MeV


Low-Energy Proton Challenges

- Increased LET variability at the Bragg peak – statistical/systematic error
- Energy/range straggling close the Bragg peak makes LET a stochastic process
- Problems increase with flip-chip irradiation
- Monte Carlo tools provide a possible solution

Data from H. Paul, http://www.exphys.jku.at/stopping/
Beyond Low-Energy Protons

400 keV Muons on a 65 nm SRAM

\[ \alpha \approx 10^{-17} \text{cm}^2/\text{bit} \]


28 GeV iron ions on SRAM structure and ensuing delta ray energy deposition.

# SEE Rate Calculation Development

<table>
<thead>
<tr>
<th><strong>Milestone</strong></th>
<th><strong>Date</strong></th>
<th><strong>Authors</strong></th>
</tr>
</thead>
<tbody>
<tr>
<td>First reported SEU in space</td>
<td>1975</td>
<td>Binder, Smith and Holman</td>
</tr>
<tr>
<td>LET distribution concept is introduced</td>
<td>1977</td>
<td>Heinrich</td>
</tr>
<tr>
<td>First reported alpha particle upset in ground-based ICs</td>
<td>1979</td>
<td>May and Woods</td>
</tr>
<tr>
<td>Development of heavy ion SEU rate prediction model based on distributions of path length and LET</td>
<td>1978, 1980</td>
<td>Pickel and Blandford</td>
</tr>
<tr>
<td>First observations of proton-induced SEU</td>
<td>1979</td>
<td>Wyatt, McNulty, Toumbas, Rothwell and Filz</td>
</tr>
<tr>
<td>Development of semi-empirical model for proton SEU rate</td>
<td>1983</td>
<td>Bendel and Petersen</td>
</tr>
<tr>
<td>CRÈME suite of codes combine environment and rate prediction tools in standardized package</td>
<td>1986</td>
<td>Adams</td>
</tr>
<tr>
<td>Development of Effective Flux approach for heavy ion SEU rate</td>
<td>1988</td>
<td>Binder</td>
</tr>
</tbody>
</table>

SEE Rates – Traditional vs. Monte Carlo

• Traditional rate calculation models and methods fall short in some cases – work well in others
  o Angular dependence & low-energy proton effects
  o Bipolar effects in SOI CMOS
  o Charge collection by diffusion
  o Heavy ion indirect ionization
  o Ion track structure effects
  o Thick sensitive volumes

• Solution requires representation of additional physics and a better physical description of the system under simulation
SEE Rates – Let’s roll dice

- Monte Carlo simulation provides a path forward since an analytical solution is not required. It can invoke:
  o Quantitative description of the relevant radiation environment(s)
  o Transport of the incident radiation through any materials or structures that surround the sensitive circuitry
  o Energy deposition in the electronic materials by the impinging radiation
  o Conversion of energy into charge
  o Charge transport and recombination in the semiconductor and insulator regions
  o Transistor-level response, including effects of charge deposited by incident radiation
  o Circuit response, including radiation-induced transients


Suggestions for SEE Testing and Rate Calculations

- Develop advanced skills to de-process and prepare devices for testing
  - Different requirements for protons, heavy ions, and pulsed laser irradiation
  - Mechanical and chemical methods
- Study facility capabilities and understand limitations
- Utilize test methods that yield intimate device control and data visibility
  - Need clear understanding of data capture and analysis requirements
Suggestions for SEE Testing and Rate Calculations

• Study the available SEE rate calculation methods and understand their limitations and what you’re asking the tool to return
  o The answer is only going to be as good as the question asked
  o This may mean running both analytical and Monte Carlo simulations for comparison purposes
Radiation Input is Vital!

Radiation issues are seldom black or white

“… a test result is insufficient in determining device applicability without knowledge of the circuit, subsystems, and system effects. This implies the philosophy of risk management as opposed to risk avoidance. [LaBel, et. al., *IEEE TNS*, 1998.]”

“Expert judgment” is essential…

Adapted from J. Stone, *IEEE NSREC Short Course*, 2009.