A Robust Strategy for Total Ionizing Dose Testing of Field Programmable Gate Arrays

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What is an FPGA?

- A Field Programmable Gate Array (FPGA) is a building block electronic device that consists of:
  - An array of logic modules,
  - An input/output ring, and
  - A programmable interconnect.
  - *All on a CMOS silicon base.*

- An FPGA may replace everything from simple logic to complex processors to ASIC devices in a space system.

- Configuration defines connectivity of logic, I/O, flip-flops, custom blocks, clocks…

FPGA-architecture

[Slide courtesy K. Label, 2006.]
A Bit About Synchronous Designs

- High speed digital designs often use “Synchronous Design Methodology” to produce a highly reliable, deterministic operation.
- All operations are synchronized to a master set of clocks operating at a precise speed to allow all logic to “settle” before capturing results.
- Degradation of timing margins may cause a failure if the delay through any logic path (we call this $t_{dly}$) exceeds the clock period.

Each flip flop has clk period > $t_{dly}$
Internal Structure

• Each individual logic function in the FPGA is constructed from a specific combination of switches inside a logic tile.

Radiation Effects

- Charge accumulated from total ionizing dose (TID) can degrade the performance of these switches and increase delay of the logic gates.
- As $\tau_{DLY}$ becomes greater than $\tau_{Clock}$, the critical law of synchronous design is broken.
- If the data is not settled during $\tau_{Clock}$ the flip flops will capture the wrong data and circuit operation will be disrupted!
- How do we test a complex device for total ionizing dose (TID) tolerance? How will radiation affect each of these elements?
Traditional Testing

• Typical TID tests measure increased delay in FPGA logic elements
  – How? Often by simply generating long chains of logic (i.e. inverters/buffers) and measuring delay from one input pin to another (this is asynchronous operation)
  – Is that bad?
    • Mixing different technologies (I/O vs logic)
    • Low measurement fidelity (you can only detect LARGE changes)
    • Not reflective of synchronous design used in final product!

• There must be a better way…
Proposed Method

• Measure logic delay ($\tau_{dly}$) internally at the smallest scale possible
  – Build a design with uniform layout (and uniform delay) between flip flops.
  – Determine maximum operating speed to deduce the true $\tau_{dly}$ between flip flops.
  – Irradiate, then re-measure to determine change in $\tau_{dly}$ due to radiation.

• Now we’re testing with a synchronous methodology comparable to a real design.
**What is $T_{dly}$?**

- The primary metric measured with this procedure
- DFF’s can serve as high-speed test points with a total delay of $T_{dly}$ between stages.
- When timing degrades in a single logic path, the entire circuit fails.

\[
\tau_{dly_{wsr_8}} > \tau_{dly_{wsr_0}}
\]

$\tau_{dly}$ = path delay from DFF to DFF

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Proposed Method (Visually)

Unoptimized design has varied delays between FF stages (longest delay will dominate!)

New design has fixed (known) delay between FF stages.

Advantages

- Measure delay *between two flip flops*, instead of between two I/O pins (10s of picoseconds, rather than 100s of nanoseconds).

- Detect a change in *any* logic path rather than measuring the cumulative change in all of them.
  - Worst-case measurement is preferable to averages (i.e. marketing data)
  - Remember, if only one path shows significant increase, your synchronous design may fail!

- Failure is defined in terms *a designer can use*. If designer builds in 10% margin, we can detect precisely when that will occur at the lowest levels possible.
Experimental Verification

- TID test to 45 krad (Si) with Microsemi ProASIC3 Flash-based FPGAs (A3PE1500).

We are measuring tiny increases in delay between flip flops, not gross changes in the entire FPGA.
A Designer’s Perspective

• Designer needs no radiation background. (What does it mean that a part is good to 30 krad? What happens then?)
• We can plot measured clock period directly compared to values calculated with static timing analysis (STA) software and tell the designer exactly what happens at each dose point.

Design margin is exhausted!
Summary

• Improved measurement fidelity (pico- instead of nano-seconds)

• Worst-case measurement -- Measure each individual logic path’s delay
  – Any degraded path is visible, instead of being averaged out by the rest

• Measure an isolated, single variable, rather than a combination of multiple factors
  – Confidence in results = better risk management

• Rad effects more easily communicated to design engineers in terms of clock period
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Questions?