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Update on Scaled CMOS Radiation Hardness Assurance

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Additional Acronym Definitions

- AFRL = Air Force Research Laboratory
- ASIC = application-specific integrated circuit
- CMOS = complementary metal oxide semiconductor
- FPGA = field programmable gate array
- FY = fiscal year
- LBNL = Lawrence Berkeley National Laboratory
- MOSIS = Metal Oxide Semiconductor Implementation Service
- NSREC = Nuclear and Space Radiation Effects Conf.
- NSWC/Crane = Naval Surface Warfare Center – Crane Division
- RHA = radiation hardness assurance
- SEE = single-event effect
- SEL = single-event latchup
- SEU = single-event upset
- SET = single-event transient
- TAMU = Texas A&M University (Cyclotron Facility)
- TAPO = Trusted Access Program Office
- TI = Texas Instruments
- TSMC = Taiwan Semiconductor Manufacturing Co.
- UCD = University of California at Davis
- VU = Vanderbilt University

Introduction

- Ultra-scaled complementary metal oxide semiconductor (CMOS) includes commercial foundry capabilities at and below the 45 nm technology node
- Radiation evaluations take place using standard products and test characterization vehicles (memories, logic/latch chains, etc.)
- NEPP focus is two-fold:
  - Conduct early radiation evaluations to ascertain viability for future NASA missions – leverage commercial technology development
  - Uncover gaps in current testing methodologies and mechanism comprehension – early risk mitigation

Introduction

- **Large source of collaboration with external partners:**
  - **Corporate**
    - **IBM Corp.**
    - **IMEC**
    - **Intel Corp.**
    - **Jazz Semiconductor (TowerJazz U.S. Subsidiary)**
    - **Texas Instruments**
  - **Government**
    - **Air Force Research Laboratory**
    - **Naval Research Laboratory**
    - **Sandia National Laboratories**
  - **University**
    - **Vanderbilt University**
    - **The Georgia Institute of Technology**

Scaled CMOS

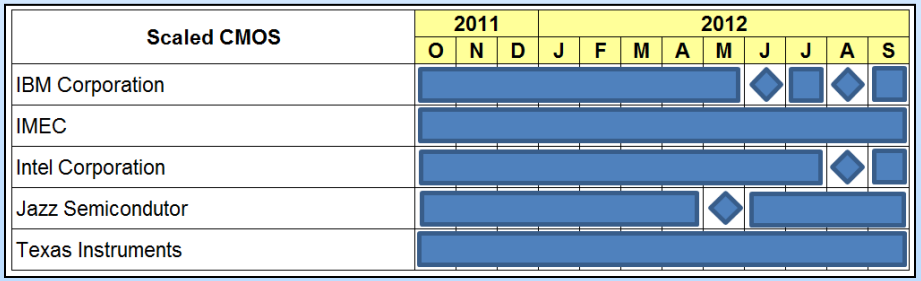
Description:

- Continue task to evaluate scaled CMOS technologies (≤ 45 nm) from IBM, Intel, and Texas Instruments,
- Determine inherent single-event effects (SEE) tolerance of Trusted Access Program Office (TAPO) product flows,
- Identify challenges for future SEE hardening efforts
- Investigate new SEE failure mechanisms and effects, and
- Provide data to NASA and DTRA modeling programs.
- Testing covers mostly non-destructive SEE using heavy ions, protons, and pulsed lasers.

FY12 Plans:

- IBM: start test campaign for 32 nm silicon on insulator (SOI) static random access memory (SRAM); start test campaign for 32 nm SOI single-event transient (SET) characterization vehicles; and, continue tests of 32 nm SOI latches using various radiation sources; employ new precision vertical mill to yield advanced flip-chip sample preparation for low-energy protons and pulsed laser testing. Other components/technologies as available.
- IMEC: support Vanderbilt efforts to gather single-event effects data on 20 nm fin-FETs; and support subsequent modeling efforts.
- Intel: start TID test campaign on 22 nm processors (3-D transistors).
- Jazz Semiconductor: complete test campaign on digital logic application-specific integrated circuits at 180 nm; support Vanderbilt single-event latchup (SEL) evaluations on 180 nm characterization vehicles.
- Texas Instruments: support Vanderbilt efforts to gather single-event effects data on 28 nm hardware; and support subsequent modeling efforts.

Schedule:



- All tasks are currently ongoing
- Diamonds indicate completed or scheduled tests

Deliverables:

- Quarterly status reports to NEPP and DTRA
- Test reports
- Updates to lessons learned
- Presentations at technical conferences
- Publications in journals and on NEPP website

Goals

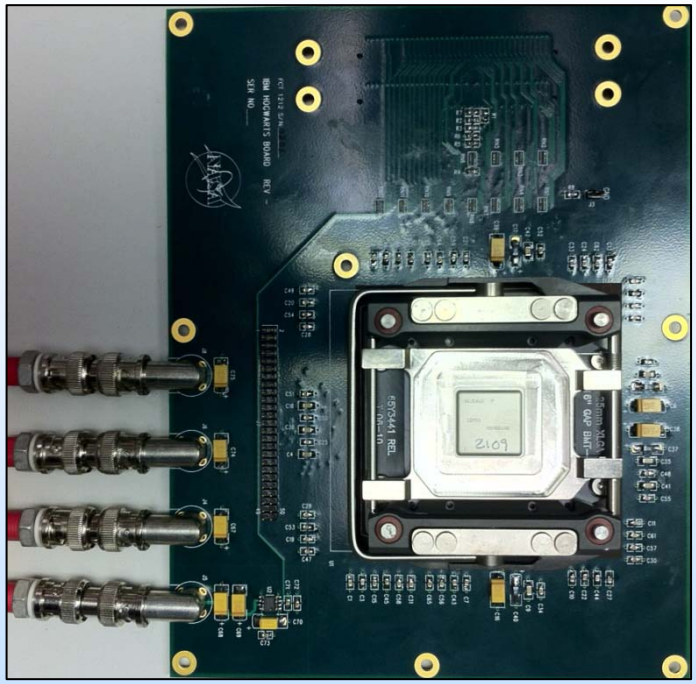
- IBM Corp.
  - Gather first single-event data sets on 32 nm SOI SRAM
  - Gather first single-event data sets on 32 nm SOI SET characterization vehicles
- IMEC
  - Support testing of 20 nm fin-FETs (FET = field effect transistor)
- Intel Corp.
  - Gather gamma total ionizing dose data on 22 nm processors – 3-D transistors
- Jazz Semiconductor
  - Gather single-event data on 180 nm digital logic ASIC for comparison to related designs in field-programmable gate arrays (FPGAs)
- Texas Instruments
  - Support testing of 28 nm characterization vehicles

Expected Impact to Community

- **Encourage early-adoption of advanced technologies**
  - **Promote technology development and leverage non-recurring engineering**
- **Identify new failure mechanisms**
  - **Reduce risk**
  - **Refine test methodologies and standards**
- **Strengthen existing and foster new relationships with industry**
  - **Maintain proactive (not reactive) stance for the radiation community**
- **Support Department of Defense foundry roadmaps for future rad-hard/tolerant devices**

IBM SOI CMOS T&E Highlights

128 Mb (64Mx2) SRAM in CMOS13S (32 nm SOI)

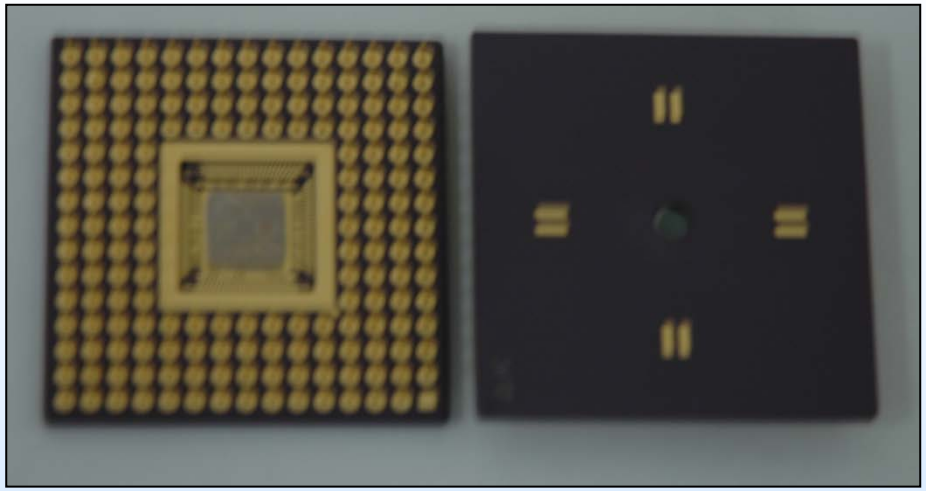


- **Similar in design to 45 nm SOI SRAM tested during FY09 & FY10**
- **Flip-chip land grid array requires mechanical thinning and polishing with new vertical mill**
  - **Similar process being applied to Xilinx FPGAs**

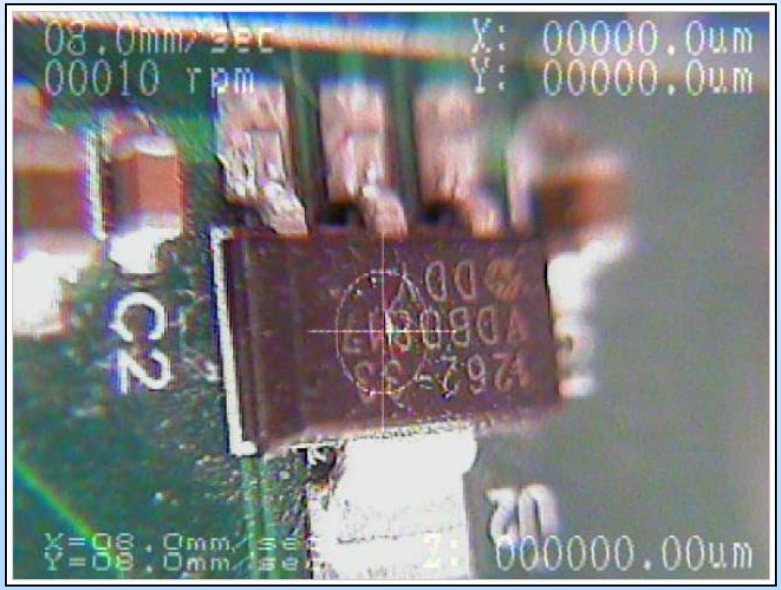
IBM SOI CMOS T&E Highlights

Test Capability Upgrades

ASAP-1 IPS



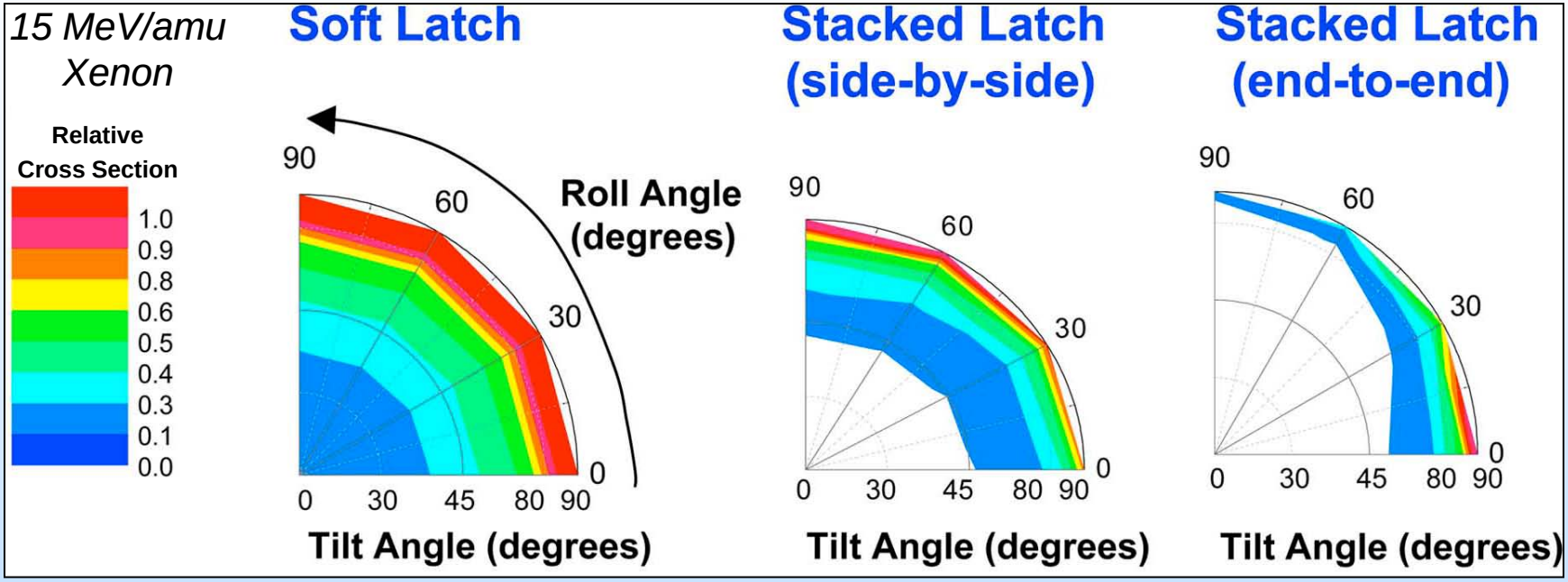
32 nm Terra SAIL macro



- Terra macro in cavity-down package made for pulsed laser and low-energy proton testing
  - XeF_2 etch
- Selected area sample prep machine from Ultratec (advertised at NSREC)
  - Grind and polish for decapsulation and thinning
- <u>40 nm vertical precision</u>

IBM SOI CMOS T&E Highlights

32 nm SOI CMOS latch cross sections – contours are based on data & simulation



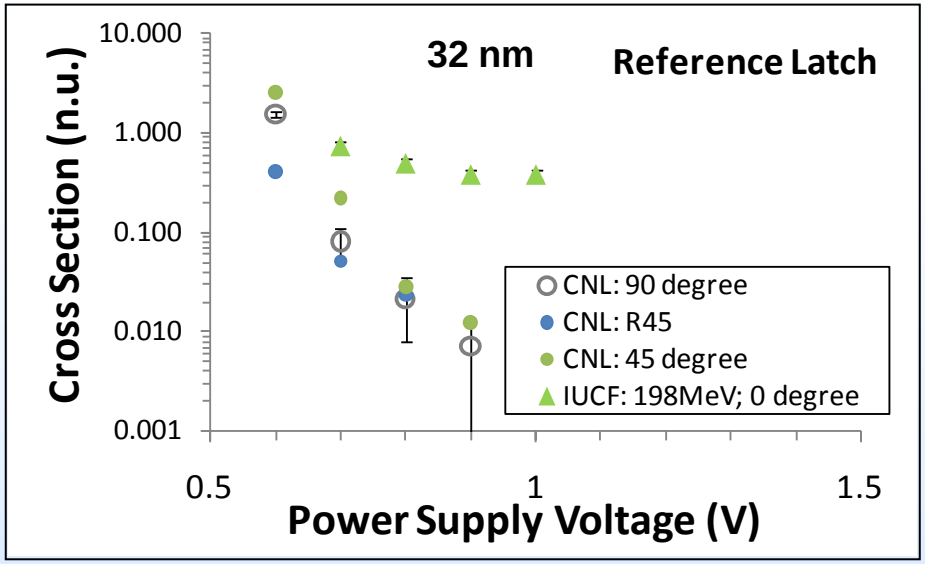
K. P. Rodbell et al., IEEE TNS, 2011.

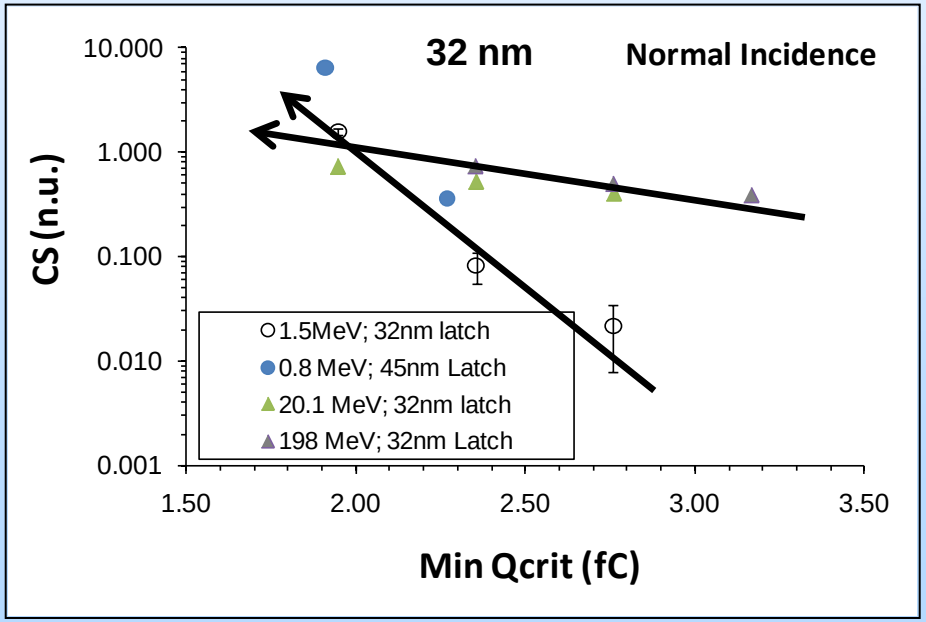
- **Non-destructive SEE continue to be the most difficult aspect of advanced CMOS radiation effects**
  - **Varied angular sensitivity (test considerations)**

IBM SOI CMOS T&E Highlights

- **Previous radiation investigations have focused on structures that characterize static data loss:**
  - **SRAM**
  - **Latches**
- **Moving to focus on SETs with specific test vehicles (MOSIS/TAPO via IBM and AFRL):**
  - **32 nm SOI pulse width measurement. Design based on B. Narasimham, *et al.*, IEEE TDMR, vol. 6, no. 4, pp. 542 – 549, 2006.**
    - **More traditional SET pulse width measurement technique that will complement AFRL/IBM test chip and previous radiation testing on IBM latches**
  - **32 nm SOI design cells based on C2 microprocessor, BlueGene/Q flavor – includes RHDB and control**
    - **What happens to SETs with hardened/soft latches when transients/errors are passed through multiplier and comparator stages? (Realism)**

Intel Bulk CMOS T&E Highlights



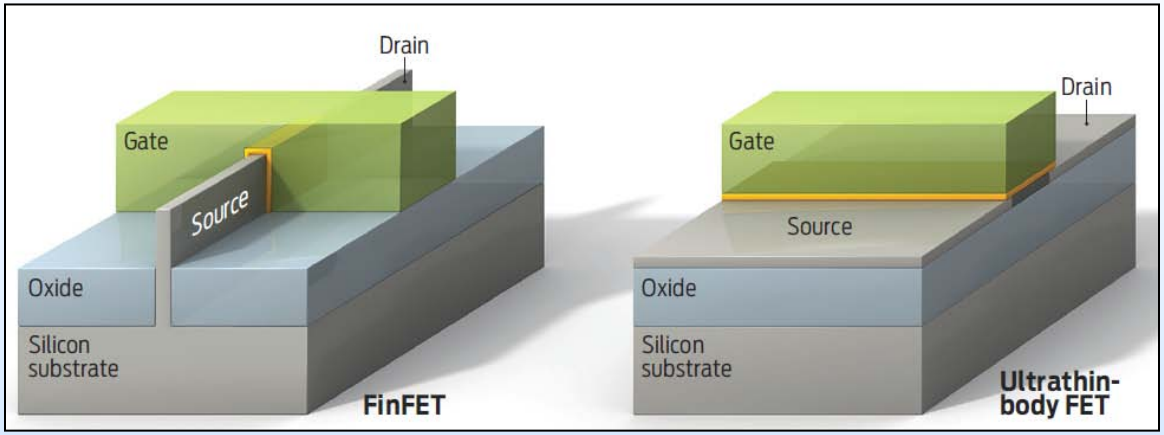


N. Seifert, et al., 2011 NSREC.

- **Low-energy proton testing**
- **Exponential Increase in cross section with decreasing power supply voltage**
  - **Expected to be of increased importance with scaling**
- **Critical charge determined to be primary factor relative to high-energy proton behavior**
- **Overall, Intel designs had limited sensitivity to low-energy protons**

Intel Bulk CMOS T&E Highlights

22 nm bulk CMOS Microprocessors



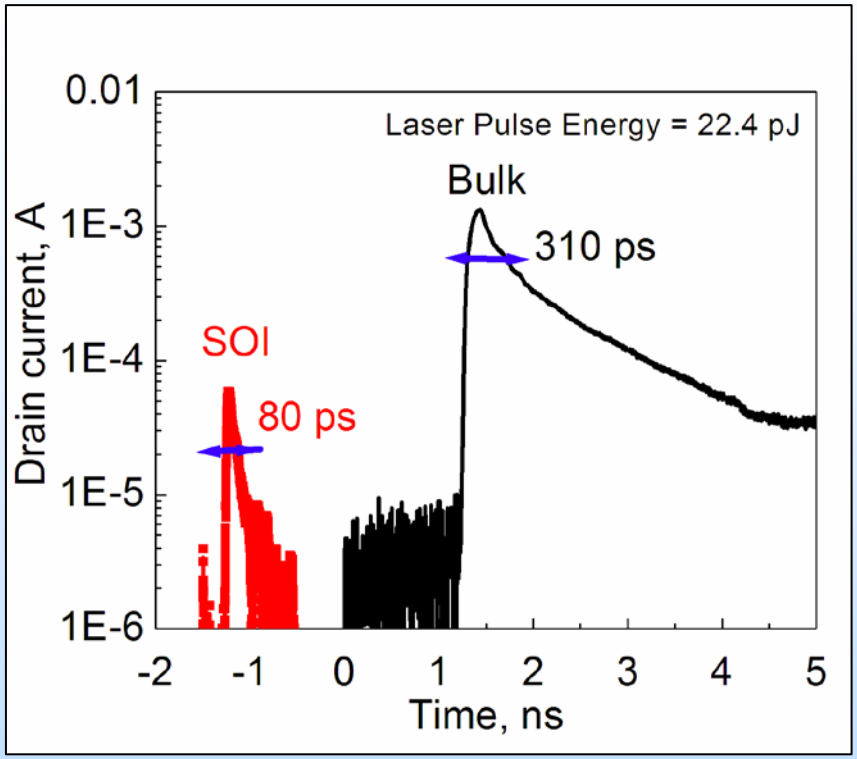
"Transistors go 3-D," *IEEE Spectrum*, vol. 48, no. 6, pp. 12-12, 2011.

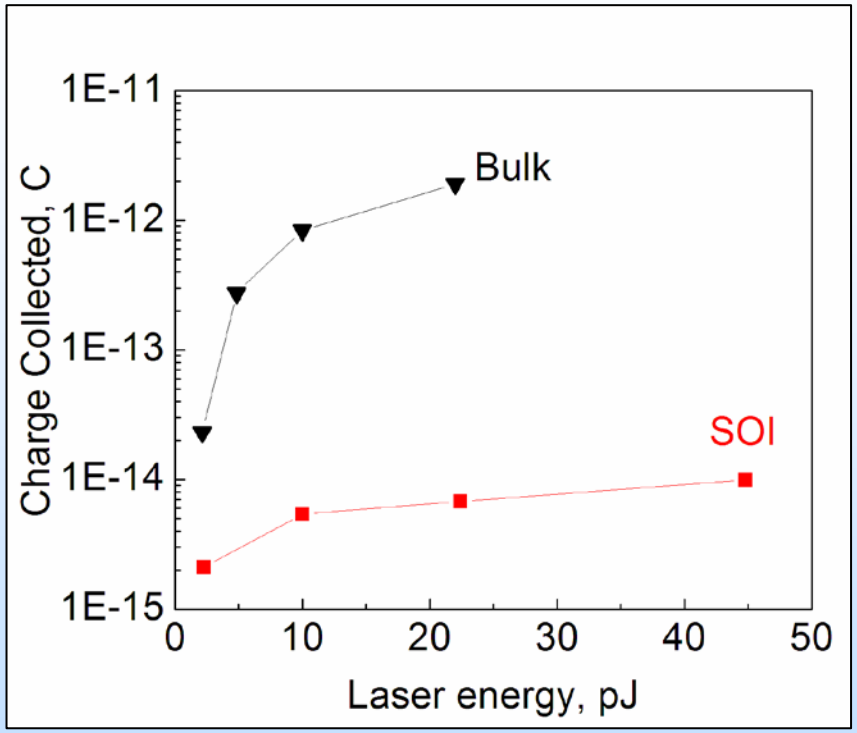
http://www.pcworld.com/article/253652/intels_ivy_bridge_3d_chips_may_launch_april_23.html

- **Commercially-manufactured tri-gate/FinFET devices**
- **Will be the first NASA radiation test of commercial 22 nm hardware**
- **Data will be FOUO and available to U.S. Government agencies upon request – Intel informed**

IMEC CMOS T&E Highlights

Bulk vs. SOI FinFET Pulsed Laser Data





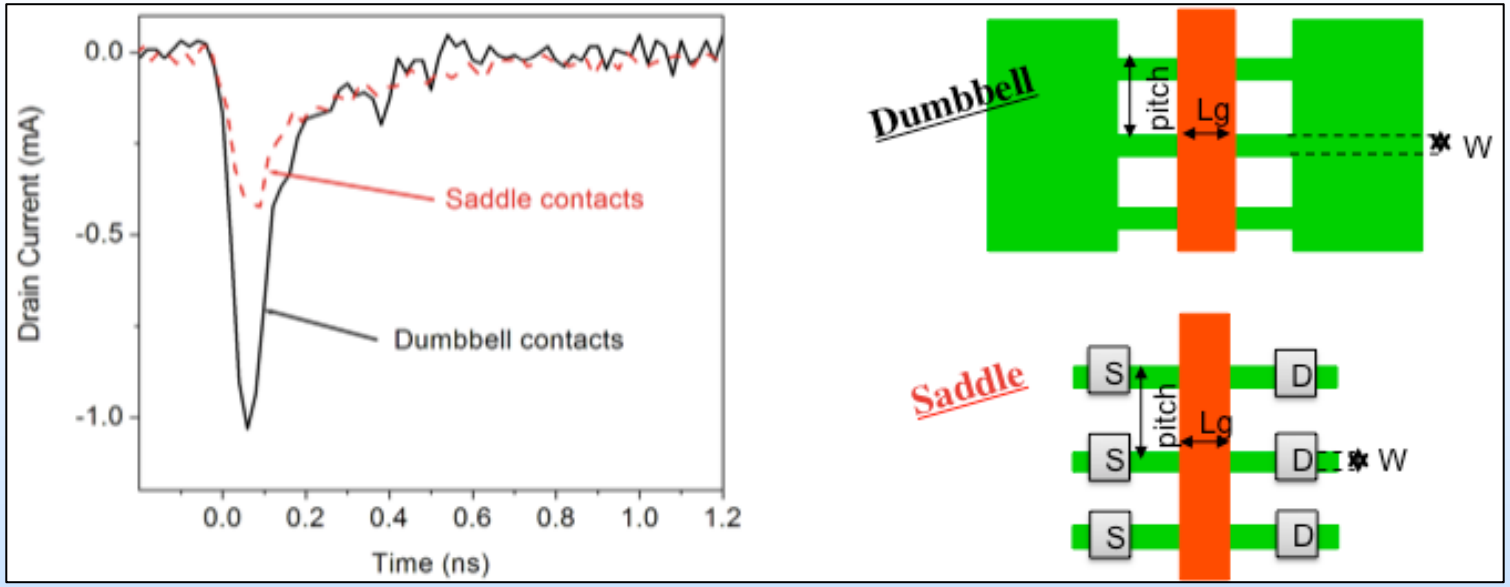
F. El-Mamouni, *et al.*, 2011 NSREC.

SOI: Lg=120 nm; FW=150 nm **Bulk: Lg=130 nm; FW=160 nm**

- **SOI FinFETs may be more advantageous than their bulk counterparts due to isolating effects of the buried oxide**

IMEC CMOS T&E Highlights
T&E Highlights

IMEC 20 nm FinFET Heavy Ion Current Transients

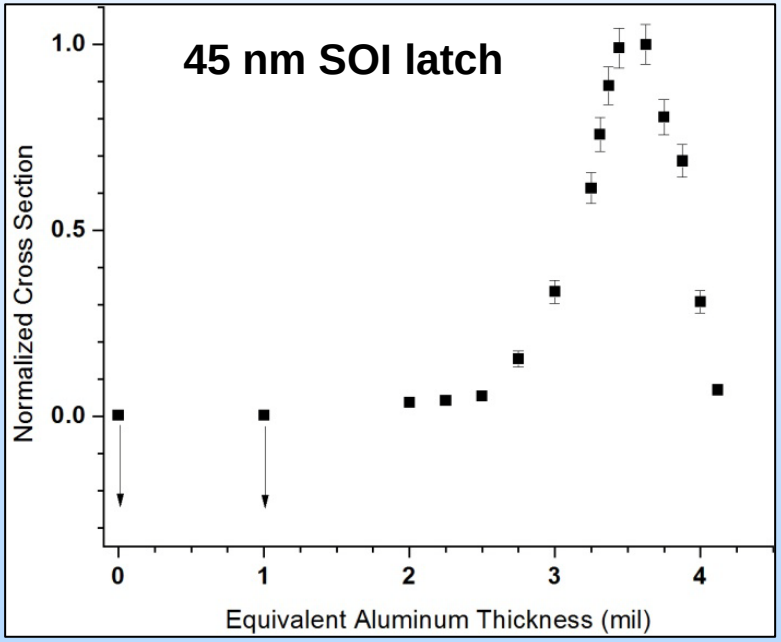


F. El Mamouni, *et al.*, Vanderbilt University, 2012.

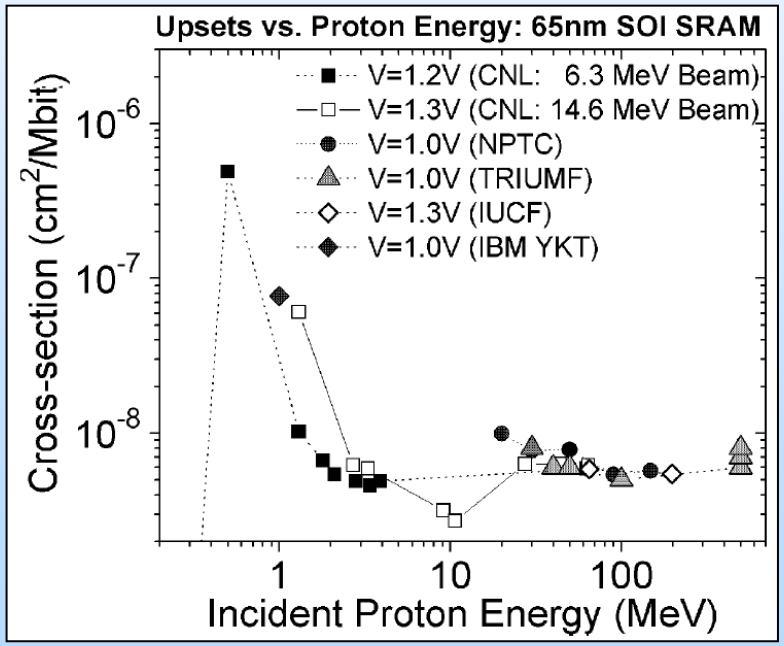
- Transients with (at least 40 %) smaller amplitudes are recorded in bulk FinFETs with saddle contacts in comparison to their FinFETs counterparts with dumbbell contacts
- Bulk FinFETs with saddle contact collect 17% less charge than their FinFETs counterparts with dumbbell contact
- Results to be presented at 2012 NSREC in Miami, FL

Low-Energy Proton RHA Highlights

- **Given a specific beam line setup, how do you go from degrader thickness to proton energy?**
  - **Capture energy and spatial mean & variance**
- **…in other words: how do you test with low-energy protons?**



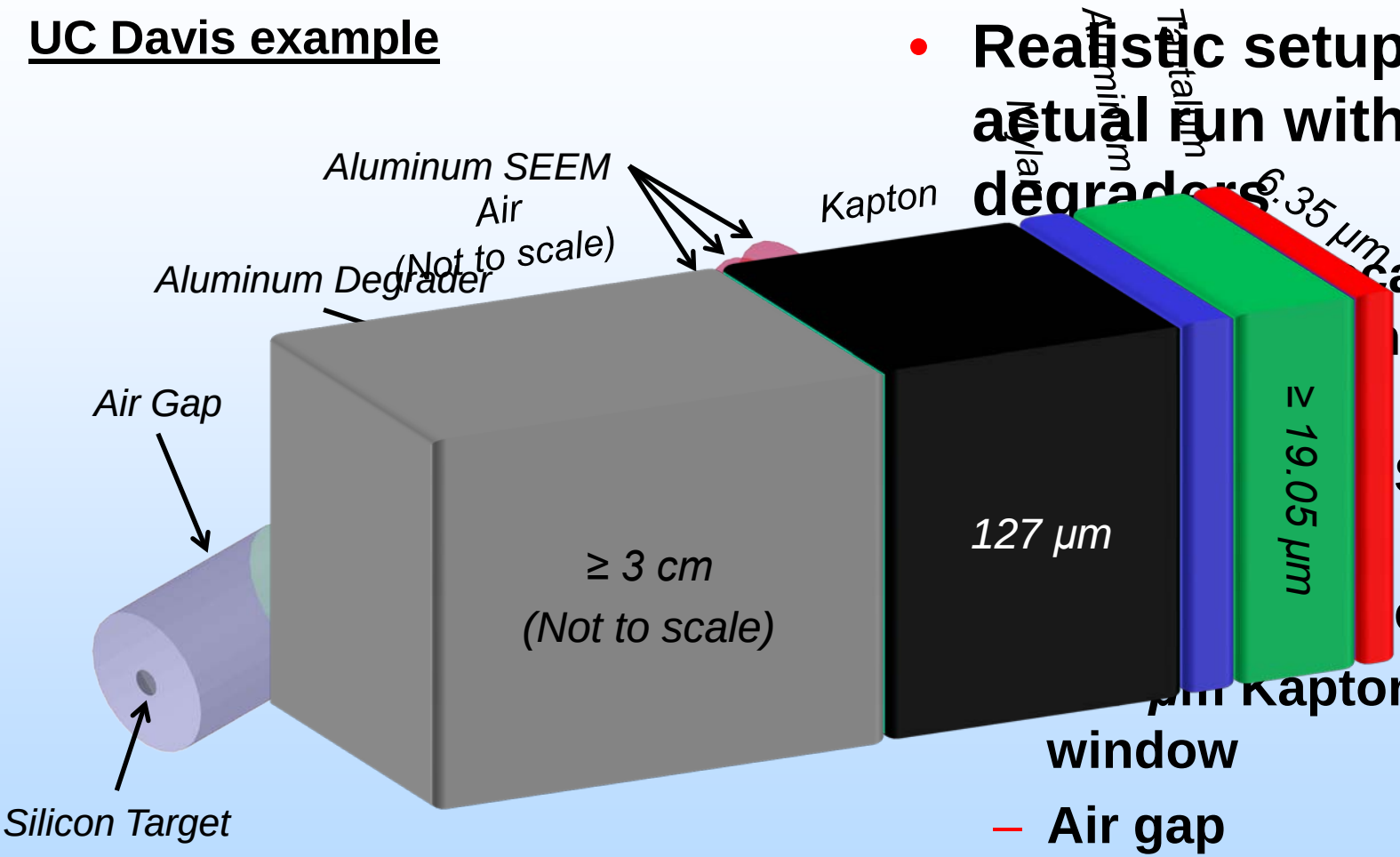
J. A. Pellish, et al., 2011 SEE Symposium.



D. F. Heidel et al., TNS, vol. 6, 2008.

Low-Energy Proton RHA Highlights

UC Davis example



- **Realistic setup for an actual run with degraders**

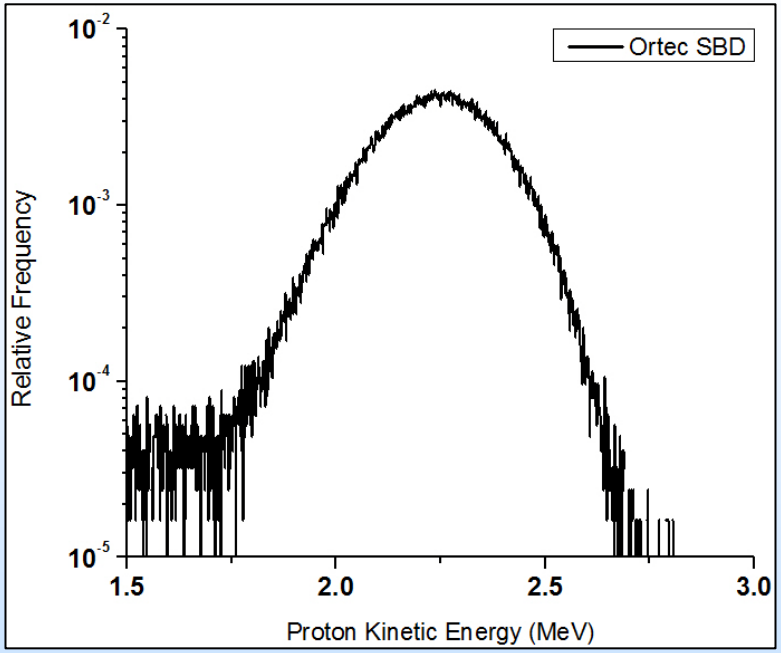
cattering
n (~4 m

SEEM

ers
µm Kapton exit window
- **Air gap**
- **Silicon target**

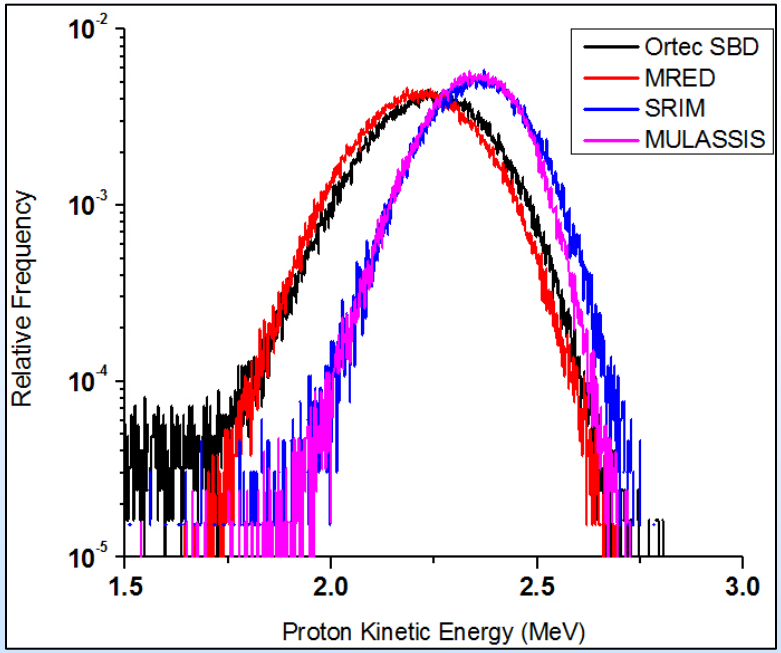
Typical planar stacked target (e.g., SRIM)

Low-Energy Proton RHA Highlights



Example SSBD Proton Energy Spectrum

SSBD = silicon surface barrier detector



<u>Degraded</u>

50.8 μm aluminum & 3.175 μm Mylar

J. A. Pellish, et al., 2011 IEEE NSREC.

- **<u>Measure</u> beam line characteristics – energy, angular dispersion**
- **<u>Simulate</u> experimental conditions when extrapolation is necessary**

FY12 Publications

2702 IEEE TRANSACTIONS ON NUCLEAR SCIENCE, VOL. 58, NO. 6, DECEMBER 2011

32 and 45 nm Radiation-Hardened-by-Design (RHBD) SOI Latches

Kenneth P. Rodbell, *Senior Member, IEEE*, David F. Heidel, *Senior Member, IEEE*, Jonathan A. Pellish, *Member, IEEE*, Paul W. Marshall, *Member, IEEE*, Henry H. K. Tang, *Member, IEEE*, Conal E. Murray, Kenneth A. LaBel, *Member, IEEE*, Michael S. Gordon, *Member, IEEE*, Kevin G. Stawiasz, *Member, IEEE*, James R. Schwank, *Fellow, IEEE*, Melanie D. Berg, *Member, IEEE*, Hak S. Kim, Mark. R. Friendlich, Anthony M. Phan, and Christina M. Seidleck

IEEE TRANSACTIONS ON NUCLEAR SCIENCE, VOL. 58, NO. 6, DECEMBER 2011 2711

The Susceptibility of 45 and 32 nm Bulk CMOS Latches to Low-Energy Protons

Norbert Seifert, *Senior Member, IEEE*, Balkaran Gill, Jonathan A. Pellish, *Member, IEEE*, Paul W. Marshall, *Member, IEEE*, and Kenneth A. LaBel, *Member, IEEE*

- **Summary of work on IBM latches, including RHBD techniques**
- **First published work between NASA/GSFC and Intel on SEE**

FY12 Publications

2968 IEEE TRANSACTIONS ON NUCLEAR SCIENCE, VOL. 58, NO. 6, DECEMBER 2011

Comparison of Single and Two-Photon Absorption for Laser Characterization of Single-Event Upsets in SOI SRAMs

James R. Schwank, *Fellow, IEEE*, Marty R. Shaneyfelt, *Fellow, IEEE*, Paul E. Dodd, *Fellow, IEEE*, Dale McMorrow, *Senior Member, IEEE*, Jeffrey H. Warner, *Member, IEEE*, Véronique Ferlet-Cavrois, *Fellow, IEEE*, Pascale M. Gouker, *Member, IEEE*, Joseph S. Melinger, Jonathan A. Pellish, *Member, IEEE*, Kenneth P. Rodbell, *Senior Member, IEEE*, David F. Heidel, *Senior Member, IEEE*, Paul W. Marshall, *Member, IEEE*, Kenneth A. LaBel, *Member, IEEE*, and Scot E. Swanson

– **Use of scaled CMOS technologies to compare pulsed laser irradiation techniques**

Venus Transit – 2012

Venus at the Edge

Image Credit: JAXA, NASA, Lockheed Martin

http://apod.nasa.gov/apod/ap120609.html