Single-Event Effects Testing of Embedded DSP Cores within Microsemi RTAX4000D FPGA Devices

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Motivation

• Perform an independent study to characterize DSP core single-event upset (SEU) behavior
• Test DSP cores across a large frequency range and across various input conditions
• Provide flight missions with accurate estimate of DSP core error rates and error signatures
Device Under Test

- **Microsemi RTAX4000D FPGA**
  - 0.15 μm CMOS logic fabric with anti-fuse configuration technology
  - Embedded multiply-accumulate DSP blocks
  - Flip-flops SEU-hardened via Localized Triple Modular Redundancy (LTMR) and output buffer triple-drive

Source: Figure 1-13, http://www.actel.com/documents/RTAXS_DS.pdf
DSP Blocks

• Functionality
  – 18x18 bit multiplier with 41-bit accumulator
  – Inputs and outputs can be registered to perform 125 MHz single-cycle multiply-accumulate functionality

• Hardening
  – SEU hardened by LTMR of all flip-flops
  – Single-event transient (SET) mitigated by temporal redundant circuit that is placed at the input data pin of each flip-flop

Source: IEEE TRANSACTIONS ON NUCLEAR SCIENCE, VOL. 57, NO. 6, DECEMBER 2010, pp. 3537-3546
Test Structure – DSP Chains

- Chains consist of 24 cascaded $AxB+C$ DSP blocks
- All chains are identical
- The chains are paired to perform internal checking
Test Structure – DSP Coefficient Control

- A and B (18-bit) parameters are selected by the tester
- Only the first-stage C (41-bit) parameter is selected by the tester
Test Structure – DSP Comparison Logic

- DSP blocks to be isolated by triplication of comparison logic
  - Eliminate SETs/SEUs contributed from other logic
DUT-Tester SEU Monitoring Interface

DUT – RTAX4000D

DSP0
DSP1

DSP2
DSP3

Tester

Error 0

Error 1

R0 R1 R2

AND

AND

To be presented by Chris Perez at the Revolutionary Electronics in Space (ReSpace) / Military and Aerospace Programmable Logic Devices (MAPLD) 2011 Conference, Albuquerque, NM, August 22-25, 2011, and to be published on nepp.nasa.gov web site.
Example DSP Upset

- Logic analyzer screenshot of actual SEU in DUT DSP cores captured by tester system
- Sampling clock is >2X frequency of maximum DSP operating frequency
Initial Phase Test Parameters

- For first round of testing, \( A_i, B_i \) set to counter for all cases
  - Each clock cycle, A and B parameters increment by 1
- C parameter remained variable
- Test matrix:

<table>
<thead>
<tr>
<th>Frequency</th>
<th>C Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>1 MHz</td>
<td>C = 0</td>
</tr>
<tr>
<td>15 MHz</td>
<td>C = +1</td>
</tr>
<tr>
<td>30 MHz</td>
<td>C = -1</td>
</tr>
<tr>
<td>60 MHz</td>
<td>C = count</td>
</tr>
<tr>
<td>120 MHz</td>
<td>C = count</td>
</tr>
</tbody>
</table>
Heavy Ion Testing at LBNL

- Energy: 15 MeV
- Fluence: up to 4.0E+7, OR until significant number of upsets observed
- Fluxes
  - 2.0E+5 to 2.3E+5 : Ne
  - 9.7E+4 to 1.1E+5 : Ar
  - 7.0E+4 to 1.0E+5 : Cu
- Angles of incidence tested: 0°, 45°, and 60°
- Effective linear energy transfer (LET) values tested: 3.94 to 29.94 MeV·cm²/mg
Initial Phase Heavy Ion Test Results: SEU cross section \( (\sigma_{SEU}) \)

**Frequency Effects**

- \( \sigma_{SEU} \) increases as frequency increases
- At low LET values, SEUs are minimal with low frequency operation
- As frequency increases, SEUs become more apparent

**Cross Sections for C = Counter**

\[
\sigma_{SEU} = \frac{\#upsets}{(Particle\ fluence)(\#DSPBlocks)}
\]

![Graph showing cross sections for different frequencies with LET values ranging from 3.49 to 29.94 MeV·cm²/mg.](image)
Initial Phase Heavy Ion Test Results: Coefficient Effects

- Choice of C parameter does not appear to have significant effect on $\sigma_{\text{SEU}}$
Comparison of NASA Radiation Effects and Analysis Group (REAG) results with Microsemi results

- At low LET, results are statistically similar
- As LET increases, differentiation becomes more pronounced

Source for Microsemi data: IEEE TRANSACTIONS ON NUCLEAR SCIENCE, VOL. 57, NO. 6, DECEMBER 2010, pp. 3537-3546

Are SETs effectively being filtered by delay chain of 750ps and guard-gate?
\[ P(f_s)_{\text{error}} \propto P_{\text{Configuration}} + P(f_s)_{\text{functional Logic}} + P_{\text{SEFI}} \]

- **Probability for Design Specific system SEU**
- **Probability for Configuration SEU**
- **Probability for Functional logic SEU**
- **Probability for Single Event Functional Interrupt**

**For RTAX-DSP target device...**

\[
P_{\text{configuration}} \rightarrow 0 \quad P_{\text{SEFI}} \rightarrow \text{low} \quad P_{\text{DFFSEU}} \rightarrow 0
\]

\[
P(f_s) \propto P(f_s)_{\text{SET}} \rightarrow \text{SEU} \propto \sum_{i=1}^{N} P_{\text{gen}}(i) \times P_{\text{prop}}(i) \times \tau_{\text{width}}(i) \times f_s
\]
Next Phase of Testing

- Future testing to validate expected cross section saturation and threshold LET
- May limit testing to worst-case conditions (120 MHz) to increase data points
- Test at higher LETs to observe if any potential DSP functional interrupts or global functional interrupts
- Test at all other input conditions (A_i, B_i coefficients set static instead of dynamic)
Acknowledgements/Closing

- RTAX-DSP FPGA devices remain a good choice for designers of DSP algorithms targeting FPGAs for space
- All upsets observed appear to stem from transient capture at output registers of DSP cores
- How effective is the implemented temporal filter for the DSP blocks?

- I’d like to thank Melanie Berg, Mark Friendlich, Hak Kim for their expertise, assistance during test planning, design, execution, and analysis
- Questions?