

Investigation of Current Spike Phenomena During Heavy Ion Irradiation of NAND Flash Memories

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Abstract—We have conducted a set of heavy ion irradiations to investigate previously reported current spikes. High current events were observed, however, none matches the current signature reported previously. Plausible mechanisms are discussed.

I. INTRODUCTION

We report the results of a heavy ion test intended to reproduce the destructive current spikes reported in [1, 2], but not observed in other studies [3]. We used the same part types, and duplicated the beam conditions. Although a total of 52 high current events were observed, none matched the 300-400 ms pulses described in [1, 2]. Our results seem to be explained nicely by the mechanisms proposed by Shindou et al, [4], and we will discuss our results in light of these mechanisms. To shed more light on the mechanisms underlying high current events, we have conducted pulsed laser experiments, using the NRL laser, to identify regions on the chip where high currents can be induced, by the laser, and presumably, also by heavy ions. We have also conducted heavy ion experiments using the Micro-RDC Milli-Beam system, which collimates the beam, so that only a small part of the die is exposed at any one time. The Milli-Beam experiment serve as an interesting check on both the laser experiments and on broad beam heavy ion exposures reported previously [1-3]. We will discuss all these results.

II. DESCRIPTION OF DEVICES UNDER TEST (DUTs)

The Micron samples in the broad beam exposures at the TAMU Cyclotron were 4G NAND flash (part number MT29F4G08AAAWP, lot date code (LDC) 748), which operate at 3.3 V, nominal, with the allowed range 2.7-3.6 V. These parts are single level cells (SLC). For the laser and Milli-Beam tests, we again used the Micron 4G, with part number MT29F4G08ABADAHC, which is basically the same

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part in a BGA (ball grid array) package, and with LDC 0M (2010, 26th work week). The parts have a single power supply, which means there is an on-chip charge pump to produce the higher voltages needed to write and erase. The parts have 4096 blocks, of which up to 80 can be “bad” initially—the manufacturer identifies the bad blocks, so that they can be screened out. In our samples, all had a few bad blocks, but none came close to 80. Within each block, the organization was 128Kx8, with 64 pages per block. Each page is 2Kx8, plus 64 redundant rows. Maximum operating frequency is 40 MHz.

We also used Samsung 8G NAND flash at TAMU (part number K9F8G08U0M, LDC 807), which are also SLC, with the same voltage single power supply, which means they have a similar charge pump. The organization is similar, with 4096 blocks, and up to 80 bad blocks allowed. Within each block, there are again 64 pages, but the page width is doubled, to 4Kx8, since the parts have twice the capacity of the 4G. Block size, then, is 256Kx8. Maximum operating frequency is 40 MHz.

III. EXPERIMENTAL PROCEDURE

In SEE testing, all exposures were with stored logical checkerboard (AA). For single bit upsets, zero-to-one errors are normally observed, but errors of the opposite polarity are often observed if they originate in the control logic. For example, one of the common SEFI modes is for an entire block, 128Kx8 bits, to be read as all zeroes. If the block had had all zeroes stored, no error would have been detected. The testing was performed at Texas A&M University Cyclotron, using the ions indicated in Table I.

TABLE I: IONS/ENERGIES AND LETs FOR THE TAMU TEST.

TAMU Ions	Energy/AMU	Energy (MeV)	Approx. LET on die (MeV·cm ² /mg)	Angle	Effective LET
Xe	15	1935	53.9	0, 50	53.9, 84
Au	15	2955	87.5	0, 50	87.5, 138

For SEE testing, bias and operating conditions included:

- 1) Static/biased irradiation, in which a pattern was written and verified, and then irradiated. Once the desired fluence was reached, the run was stopped.

The memory contents were read and errors tallied.

- 2) Dynamic Read, in which a pattern was written to memory and verified, then subsequently read continuously during irradiation. This condition allows determination of functional, configuration and hard errors, as well as bit errors.
- 3) Dynamic Read/Erase/Write, which again was similar to the Dynamic Read, except that a word in error was first erased and then rewritten. Because the Erase and Write operations use the charge pump, it is expected that the Flash could be more vulnerable to destructive conditions during these high voltage operations.

In this set of experiments, we have included an initial attempt to look at angular effects, which may include multiple bits grazed by the same ion, and other effects due to charge sharing by multiple nodes in the control logic. This test was done at 50 degrees, which was the highest angle we could use, without the DUT socket shadowing the beam.

In all cases, the power supply current was monitored, and recorded. Although the electronic recording system had better than 1 ms resolution, the results were entered into an Xcel spread sheet when they were recorded. The spread sheet could only accommodate 32000 points per run, so we entered about 1000 points per minute in the spread sheet. Current was also displayed on an oscilloscope trace, so that current level changes could be observed in real time.

In the laser test, we used only the Dynamic Read mode, because we knew the laser would not upset the bits.

In the Milli-Beam test at LBNL, we used only Xe ions in their 10 MeV cocktail. We exposed all the peripheral control circuits in Dynamic Read mode, and started through the circuit again in Dynamic R/E/W mode, but did not have time to finish the entire circuit.

IV. RESULTS

The purpose of this experiment was to duplicate the experimental conditions in [1, 2] to see if we could also duplicate the current spikes reported there. We used the same parts and the same beam conditions as [1, 2], but with the NASA LCDT (low cost digital tester) system, rather than the test system described in [1, 2]. The current spikes were described as having a typical pulse width of 300-400 ms. Although we observed 52 high current events in this experiment, they lasted for widely varying periods. None was as short as 300-400 ms, although four were less than an order of magnitude longer. Forty-eight of the 52 events are rectangular, stair step waveforms which are identified in [4] as being caused by localized SELs (Single Event Latchup), where a small part of the circuit latches up, but the rest of the circuit remains fully functional, because sufficient bias voltage is maintained. The stair step structure occurs because one localized region undergoes SEL, then another, and perhaps then yet another, each changing the DC current level. These events have duration ranging from a few seconds to several

minutes. In fact, many of them ended only because of operator intervention. An example is shown in Fig. 1. The power supply current limit on this run was 100 mA, so the shape of the waveform is not due to current limiting.

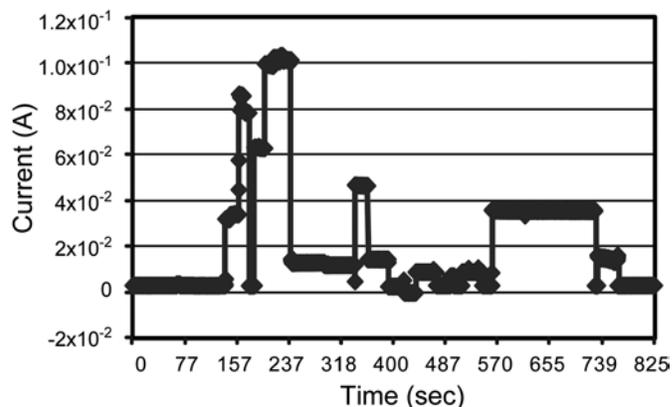


Fig. 1. Samsung DUT 1, Run 1, Static mode, Xe ions.

Two high current events were observed, with stair-step structure characteristic of LSEL[4]. Beam was turned off after the second high current event. Current level changes after the beam was off are due to actions performed to reset the part for the next exposure. Interval baseline-to-baseline was 37 sec for the first event, 57 sec for the second. DUT failed, losing both Erase and Program (write) functions.

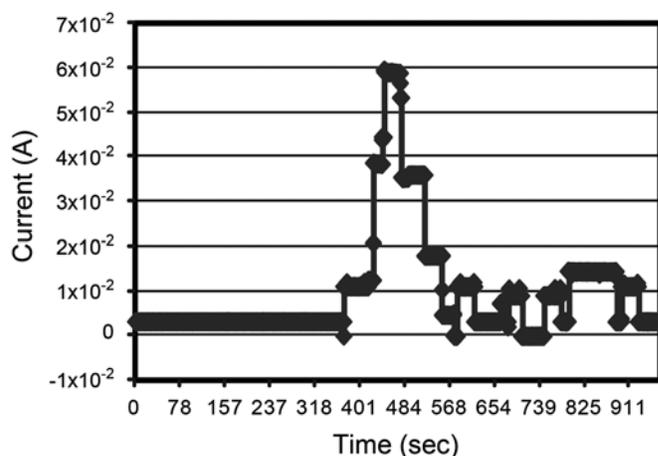


Fig. 2. Samsung DUT 3, Run 2, Xe ions, Dynamic Read mode.

In Figure 2, there is one high current event, with stair-step structure, with duration from baseline-to-baseline about three minutes. In this case, the DUT survived, an example of high current without failure.

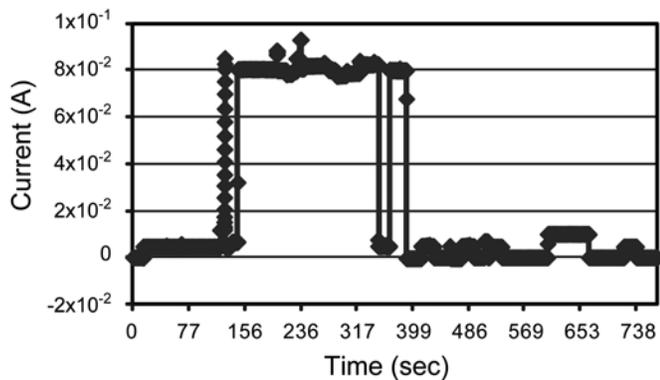


Fig. 3. Micron 4G NAND exposed to 2×10^6 Xe ions/cm² in Dynamic Read mode. DUT survived, and was used on the next shot.

There are two events shown here with rectangular waveforms, both of which reach a current of 80 mA in one step. There were a total of 48 waveforms in all the runs, we would characterize as rectangular, but, on other runs, some had multiple stair steps before reaching their peak current, as in Figures 1 and 2. Here, in Figure 3, the duration of these events is more than three minutes for the longer one, and about 25 sec for the shorter one. These are attributed to LSELs in [4], which we believe is also true here. The first high current event from Fig. 3 is the very shortest duration event of all 52 events. It is shown on an expanded time scale in Fig. 4.

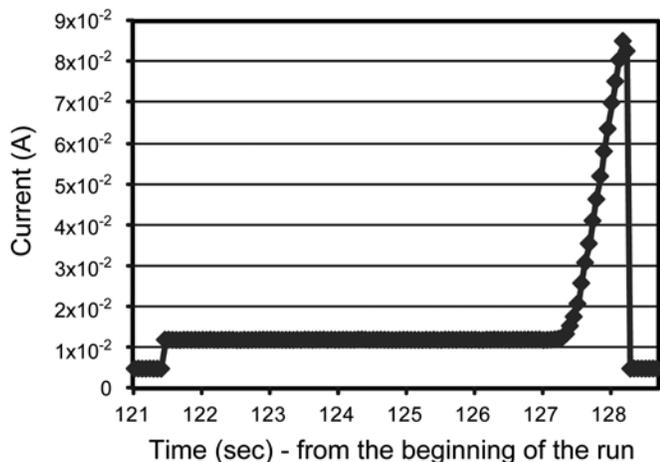


Fig. 4. Transient from Fig. 1 on an expanded time scale.

In [4] events similar to this are referred to as “pseudo-SELs”, meaning the current increases rapidly, as in a true SEL, but the mechanism is different. The mechanism is contention on the data bus lines. In this case, the DUT is receiving continuous commands to Read, and initially the current is at about 5 mA, which is the nominal Read current for this part. But there comes a point where the current jumps to about 10 mA, which is the nominal Write current for this part. It is not really clear whether the part is really trying to Write, or whether it is trying to do something else. But there was a watchdog timer error, which meant it had stopped responding to commands, which were to Read. After a few seconds where the Read circuitry was competing for control with whatever

else was active, the current increased rapidly. The contention was resolved when another Read command was received, and the current dropped back to the Read current level, and the DUT started to Read properly, again.

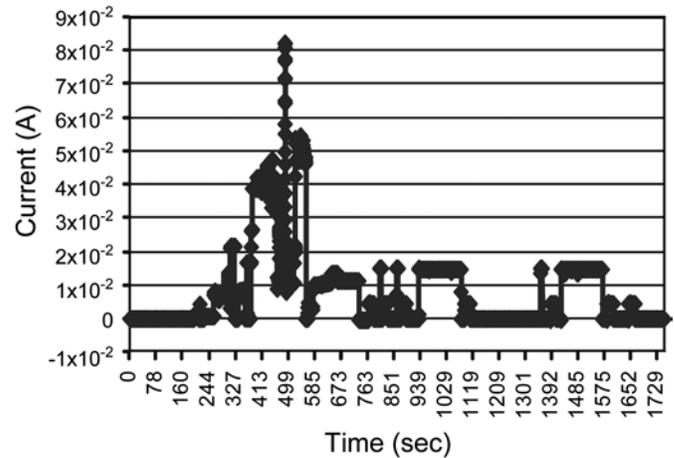


Fig. 5. Micron DUT 21, Run 5, Xe ions, Static mode. Erase and Write functions both failed.

In Figure 5, we show another example, with three high current events, the first lasting about two minutes, and the last lasting 37 sec. The second one, which is much shorter, is an apparent example of bus contention, and is shown on an expanded time scale in Fig. 6. However, it differs from the example in Fig. 4 because the DUT was in Static mode. This means the sample was not receiving any commands during the exposure. In Fig. 6, the baseline current initially is about 17 mA, compared to nominal current in Static mode for this part of <1 mA, which clearly indicates that there is activity not driven by commands from the test system. Bus contention results when two or more portions of the control logic are on at the same time, when they are not both supposed to be on, and they end up fighting for control. In this case, after the high current ends, the baseline current drops to about 12 mA. Since this value is lower than the current before the contention, it suggests that some activity stopped as a result of the contention.

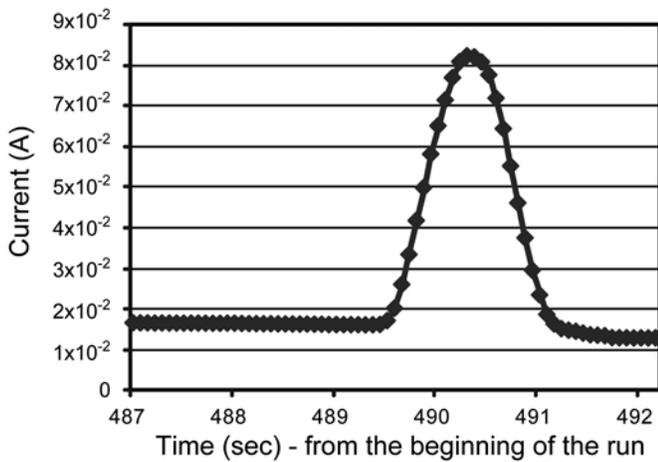


Fig. 6 Micron DUT 21, Run 5, Xe ions, Static mode. Second high current event, shown on an expanded scale.

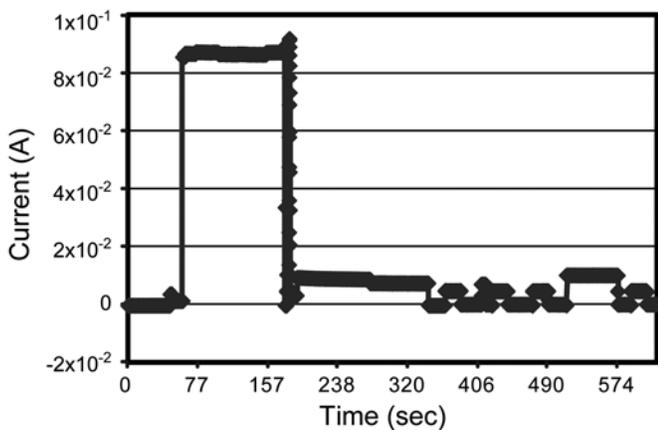


Fig. 7. Micron DUT 20—Run 9. Static mode, with fluence 1×10^6 Xe ions/cm². There are two high current events on this Run, although they appear to run together on this scale.

In Fig. 7, we show another current trace with two high current events, one lasting about two minutes, and a much shorter event which is difficult to resolve on this scale. It is shown on an expanded time scale in Fig. 8. In Fig. 8, the baseline current is about 10 mA, initially, compared to normal Static mode current less than 1 mA. The higher than expected initial current suggests activity driven by SETs. Then there is apparent bus contention, presumably because there are parts of the circuit on that are not supposed to be on at the same time. After the contention is resolved, the current drops to about 3 mA, suggesting that some of the SET-driven activity stops, consistent with the discussion of Figures 5 and 6.

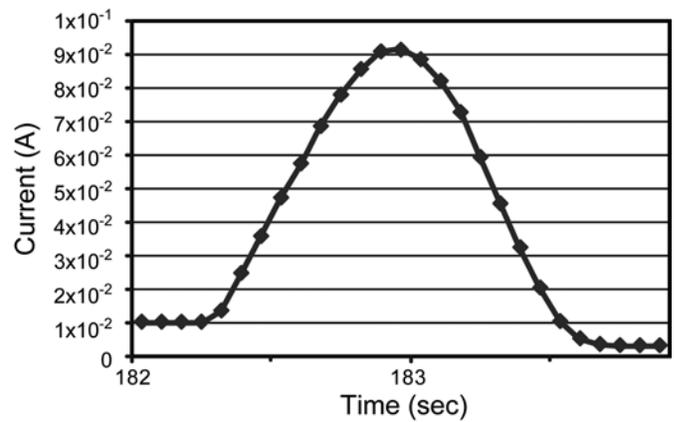


Fig. 8. Micron DUT 20—Run 9. Static mode, with fluence 1×10^6 Xe ions/cm². High current transient with an expanded time scale. Full width is about 1.2 sec, FWHM is about 0.7 sec.

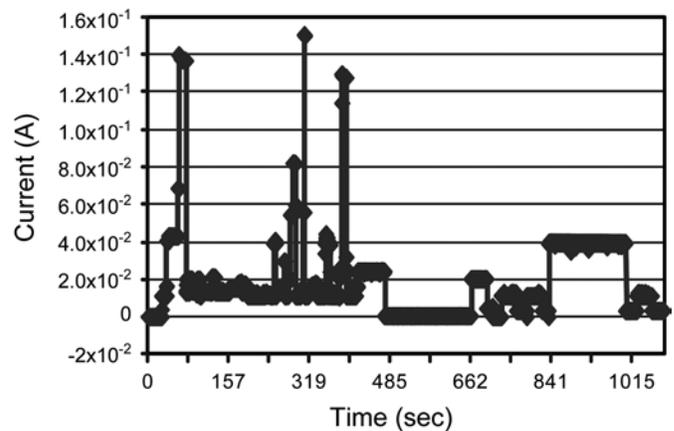


Fig. 9. Samsung DUT 4—Run 18. Dynamic Read mode, with fluence 3×10^6 Au ions/cm². Watchdog timer error, and DUT failed, losing both erase and write functions.

In Fig. 9, we show a current trace with five events where the current exceeds 40 mA. The event with the shortest duration, and also the highest current level is shown on an expanded scale in Fig. 10. The current is above 60 mA for about 1.4 sec, but the trace has the stair-step structure and square corners characteristic of LSEL.

In Fig. 11, we summarize the 52 high current events that we observed in the TAMU heavy ion experiment. The duration, baseline-to-baseline, for each high current event is tabulated, and the results are shown in the Figure. None of the events lasts less than 1 sec, and most last tens of seconds or minutes. Although it is not indicated in the Figure, many ended when they did because of operator intervention, and not spontaneously. None was in the range of 300-400 ms, although a few were less than an order of magnitude longer.

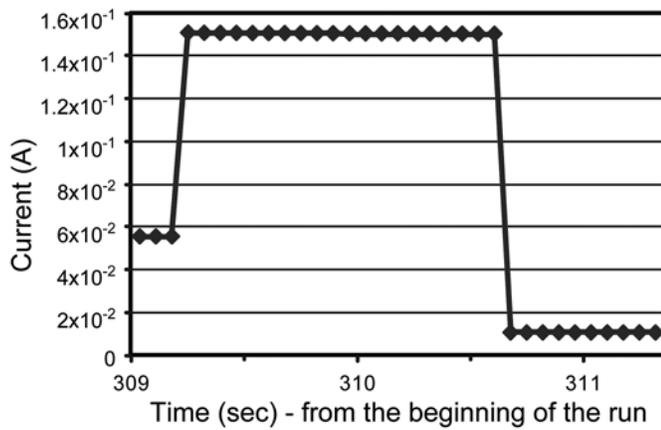


Fig. 10. Highest peak current event in Fig. 9, shown on an expanded time scale. Total duration of the entire trace is about 2 sec.

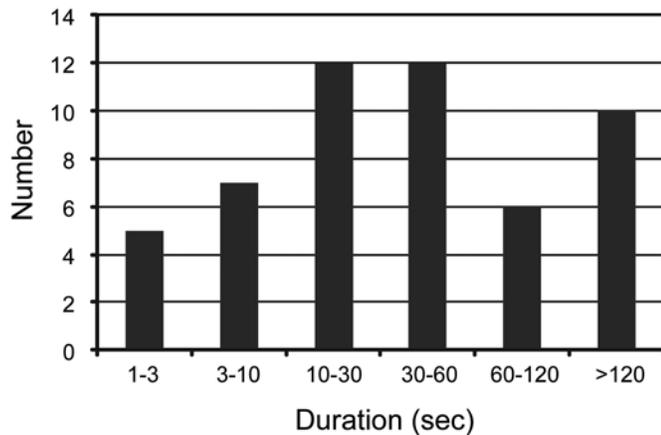


Fig. 11. Duration in seconds of all 52 high current events observed in this experiment.

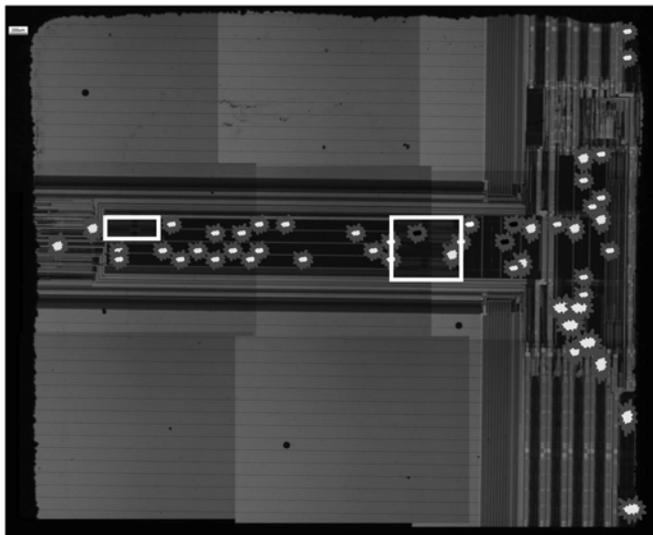


Fig. 12. Results of the pulsed laser test on the Micron 4G NAND. Red (dark) spots indicate the location of high current events, while light spots indicate locations where SEFIs without high current were observed. White rectangles indicate regions believed to be charge pumps.

In Fig. 12, we show the results of the pulsed laser test at NRL. Dark spots indicate locations where high current, 80 mA or more, was observed. Light spots indicate locations where SEFIs, without high current, were observed. There are

38 locations where high currents were triggered by the laser, including almost anywhere in the peripheral control logic. Note, however, that there are no high current events in the regions believed to be the charge pumps (white rectangles). This result is very difficult to reconcile with the conclusion in [1, 2], that the high currents are coming from the charge pumps.

In Fig. 13, we show the results of the Micro-RDC Milli-Beam experiment. In this test we collimated the beam so that only an area of 100 μm by 100 μm was exposed on each beam run. We used Xe ions at a fluence of 10⁷ ions/cm² on each exposure. That is, we exposed the entire chip to a fluence of 10⁷ Xe ions/cm² over the course of the entire run, but only a small portion of the die was exposed at one time. Locations of the numbers indicate the locations where SEFIs, requiring a DUT reset, or power cycle, or both, were observed. The numbers refer to the beam run on which the SEFI occurred. In all, there were 820 beam runs, and about 125 SEFIs in the entire run. The SEFI locations correlate very well with the locations where high currents or other SEFIs were observed in the laser test. The striking difference from the laser test, and also from the broad beam TAMU results, was that no current above 20 mA was observed at any point in the entire run. We will discuss the implications of this result later.

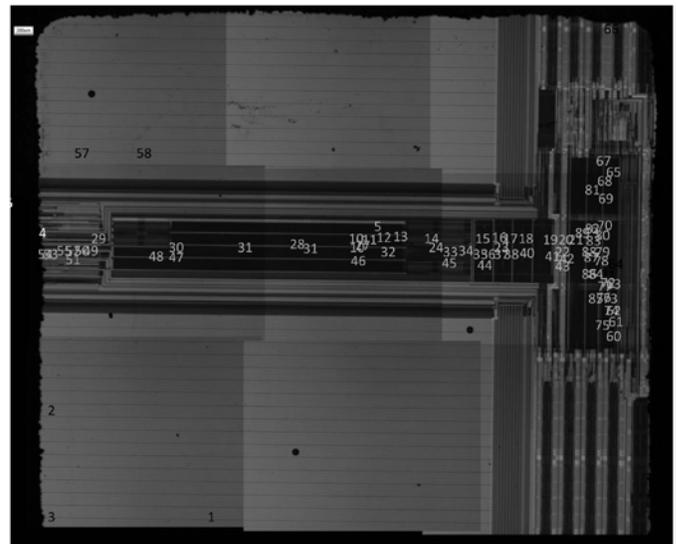


Fig. 13. Results of the Milli-Beam test. Locations of the number indicate where the Milli-Beam caused SEFIs; numbers refer to the beam run on which the SEFI was observed.

V. DISCUSSION

None of the high current events match exactly those described in [1, 2], which were said to be typically 300-400 ms. Furthermore, Fig. 14 from Irom and Nguyen [1] shows a trace with ten such high current spikes in one run. When we tried to duplicate their results in Fig. 14, the closest agreement was shown in Figs. 3 and 4. That is, nine of the ten spikes were not observed at all, and one that was observed had a different pulse width. On most other runs, all ten spikes disappeared. Therefore, we believe the mechanism in our experiment was

just different than that observed in [1, 2].

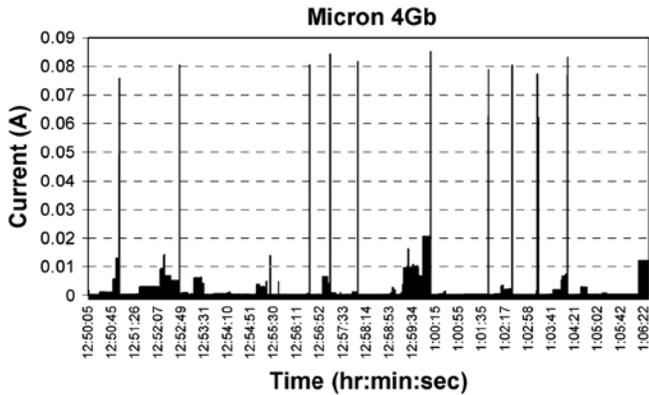


Fig. 14. Current spectrum for Micron Technology 4 Gb NAND flash. Data is taken with 181Ta ion at LET 77.3 MeV - cm²/mg at the TAM facility, figure from Irom and Nguyen [1].

We also note that the beam conditions used in [1] were 107 Ta ions/cm², with an LET of about 77 MeV/mg/cm². The flux at this LET in geosynchronous orbit is about one particle/cm² every 2000 years. That is, one particle/cm² since the birth of Christ! Under present conditions, a fluence of 107 particles/cm² corresponds to an interval of 2x10¹⁰ years, which is greater than the age of the universe. In Fig. 14 from [1], there are ten current spikes, which means the mean time between events would be on the order of two billion years. Therefore, we conclude that even if we had duplicated the current spikes in a ground test, it would not make them real in space.

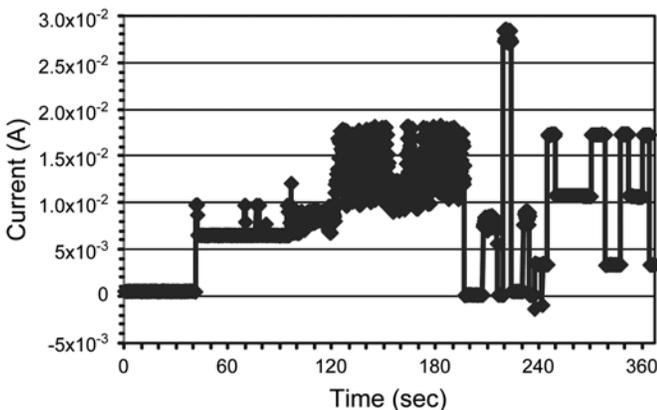


Fig. 15. Micron 4G, Xe ions, Dynamic Read/Erase/Write mode. DUT failed, losing the Erase function.

In [1, 2], it is asserted that the current spikes are destructive, meaning that they cause functional failures. In Figures 2 and 3, we have already shown two examples of high currents that were not destructive. In Fig. 15, we show an example where a Micron 4G, in R/E/W mode failed, losing the ability to Erase. But there was no current level higher than the normal write current when the beam was on, so this failure is not associated with any high current. In Fig. 16, we show results for the Samsung 4G NAND, irradiated with Xe ions. The test mode is R/E/W, where the part is read, and, if an error is detected, the

block is erased and rewritten. In Fig 15 (a), the part is reading (10 mA is the normal Read current), until errors are detected. Then the current goes back and for the between the Read current value, and the Write current, which is about 18 mA. In Fig. 16 (a), the ions were incident at high angle (45°), and no failure occurred—this current trace is an example of how the current should look. In Fig. 16 (b), on the other hand, the trace looks similar initially, but after Reading for a short time, the current increases to nearly 60 mA, and stays at nearly that level. Afterwards, the DUT could not Write, but normal current levels could be restored by telling it to do something other than Write. In this case, the ions were normally incident, and similar failures were observed in a small fraction of the shots, but only if the ions were normally incident. The clear angular dependence is the signature of SEGR, single event gate rupture. Basically, the ion blows a hole in the gate oxide of a transistor, which creates a short circuit, and the short circuit causes high current. That is, the high current is the result of the oxide failure, and not the cause of it. There are examples, where high currents and functional failures are correlated, meaning they occur on the same shot. But with all these counter-examples, where high currents do not cause functional failures, it is important to remember that correlation does not prove cause-and-effect. Functional failures in flash memory occur when the DUT can no longer Erase, or Write, which is usually assumed to be because the charge pump no longer puts out the voltage necessary for those operations. But the results in Fig. 12 suggest the high currents do not come from the charge pump. Therefore, there is no clear evidence that the high currents actually cause functional failures, even when they are correlated.

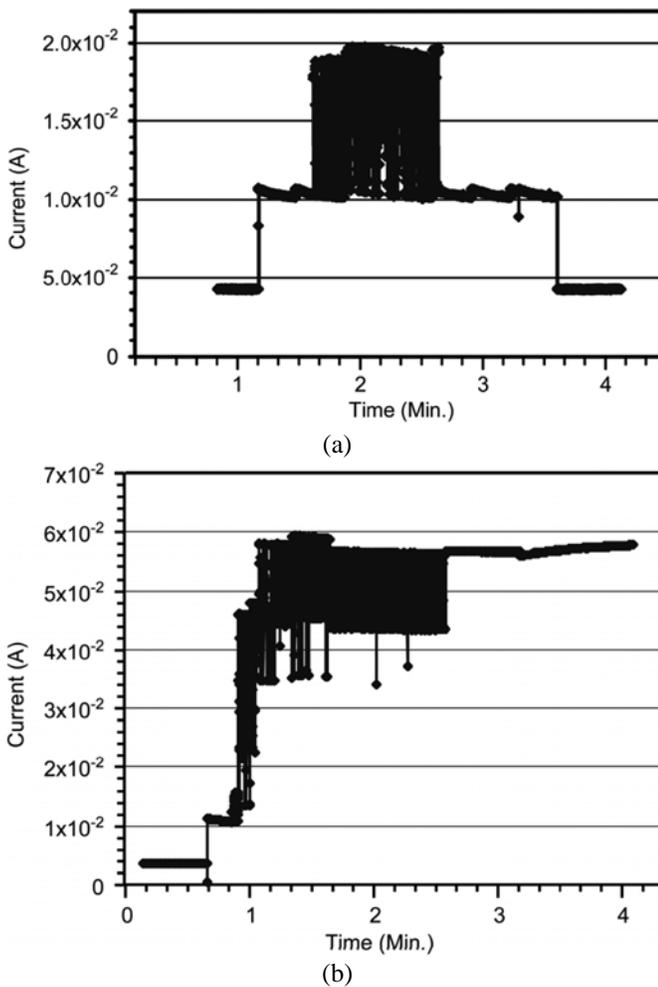


Fig. 16. Samsung 4G NAND irradiated with Xe ions in Read/Erase/Write mode: (a) 45 degree incidence, without failure; and (b) normal incidence with Write mode failure.

High current events, similar to what we observed in the TAMU experiments reported here, have been observed in a number of experiments by others [4-6]. None of these results were obtained on flash memories, which suggests that the effects reported here are not unique to flash memories. Shindou et al. [4] reported two kinds of high current events, one of which they call localized single event latchup (LSEL). An example is shown in Fig. 17, with the same stair-step structure that we observed, and have shown in several examples. The other kind of high current event they called “Pseudo-SEL”, and they attributed it to contention on the data signal lines. In [4], the authors were testing a test chip designed to check out a standard cell library, so they had every kind of combinational logic standard cell, but apparently, no charge pump. But the two kinds of high current events they discuss seem to account for all 52 of the high current events observed in our TAMU experiments.

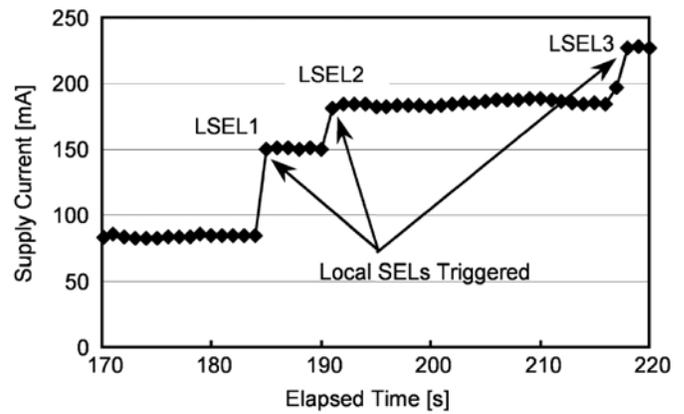


Fig.17. Stair-step increase in current, from LSEL current paths turning on, one after another, after Shindou et al. [4].

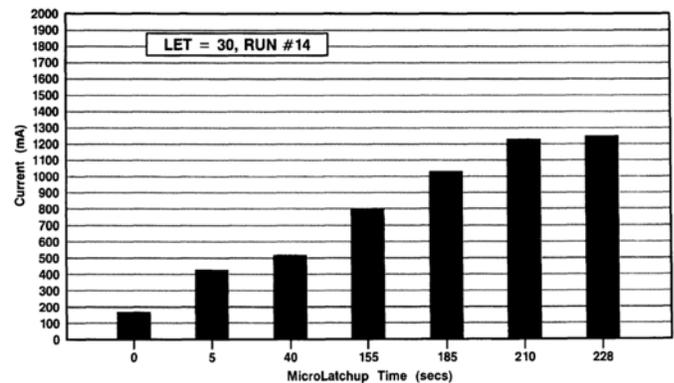


Fig. 18. Micro-latchups (or LSEL) observed in Intel 386 processor [5].

In Fig. 18, we show another example of stair-step current increases from LSELs in the Intel 386 processor [5]. This paper was the very first paper ever published in the IEEE Radiation Effects Data Workshop, in 1992. Like Shindou et al [4], it was on a logic chip, with no charge pump. In Fig. 19, we show another example, on an SDRAM [6]. Fig. 19 shows a series of clock pulses, but the baseline current increases in a stair-step manner from LSELs. SDRAMs, like flash memories, are complex circuits, with large amounts of combinational logic, embedded in the form of an on-chip controller. It appears that LSEL and bus contention can be expected in SEE testing of anything containing combinational logic. This means that the effects observed in our TAMU experiments are not unique to flash memories.

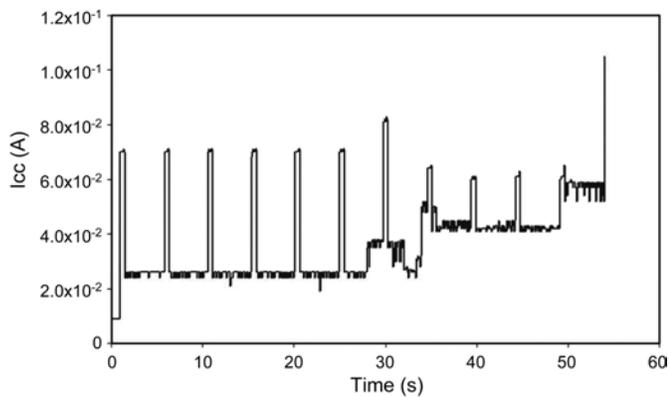


Fig. 19. Results from Poivey, et al. [6] in SEE testing of an SDRAM. Spikes here are clock pulses, but the baseline current increases in a stair-step manner from LSELS.

We noted that the results of the experiment with the Micro-RDC Milli-Beam correlated well with the NRL pulsed laser results, in the locations where SEFIs occurred, but not in the current values at those locations. In the laser test, we ran the beam at full power, to make sure we saw some effect. But equating laser power to effective LET is very difficult. We plan further testing where we will vary the laser power, and also the lens used to focus the beam. We expect that, with more careful control, the laser will come closer to matching the Milli-Beam results. The Milli-Beam results also call into question broad beam heavy ion results in [1, 2]. In those tests, the die was typically hit in about 104 location/sec, with results qualitatively far different than when the die was only hit in one location at a time. In space, the flux of ions is so low, the die will never be hit in more than one location at a time. What is the value of a ground test that produces results which can never be duplicated in space?

VI. CONCLUSION

We attempted to replicate the current spike results in [1, 2], and did observe high current events, but the waveforms and pulse widths were generally much different. Only 4 of 52 events had a pulse width within 10x of that reported in [1, 2], but the frequency of occurrence is also much different. There were only four events that did not have rectangular waveforms in 38 shots in this experiment, and never more than one on a given shot. In [1], the authors observed ten spikes or more in one shot, multiple times. It is also true that the mechanisms described by Shindou et al. [4] were observed in combinational logic, but they seem to explain very nicely all 52 of our high current events. Similar things have also been observed in other kinds of circuits [5,6], without charge pumps. Therefore, there is no reason to believe that the kinds of high current events reported here are unique to flash memories.

We have also presented laser test results and Milli-Beam test results, and compared them to broad beam heavy ion results. The differences have significant implications for future testing procedures.

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