National Aeronautics
and Space Administration

Challenges of Developing Qualification Methods for Double-Data-Rate (DDR) Class Memories - Part 1

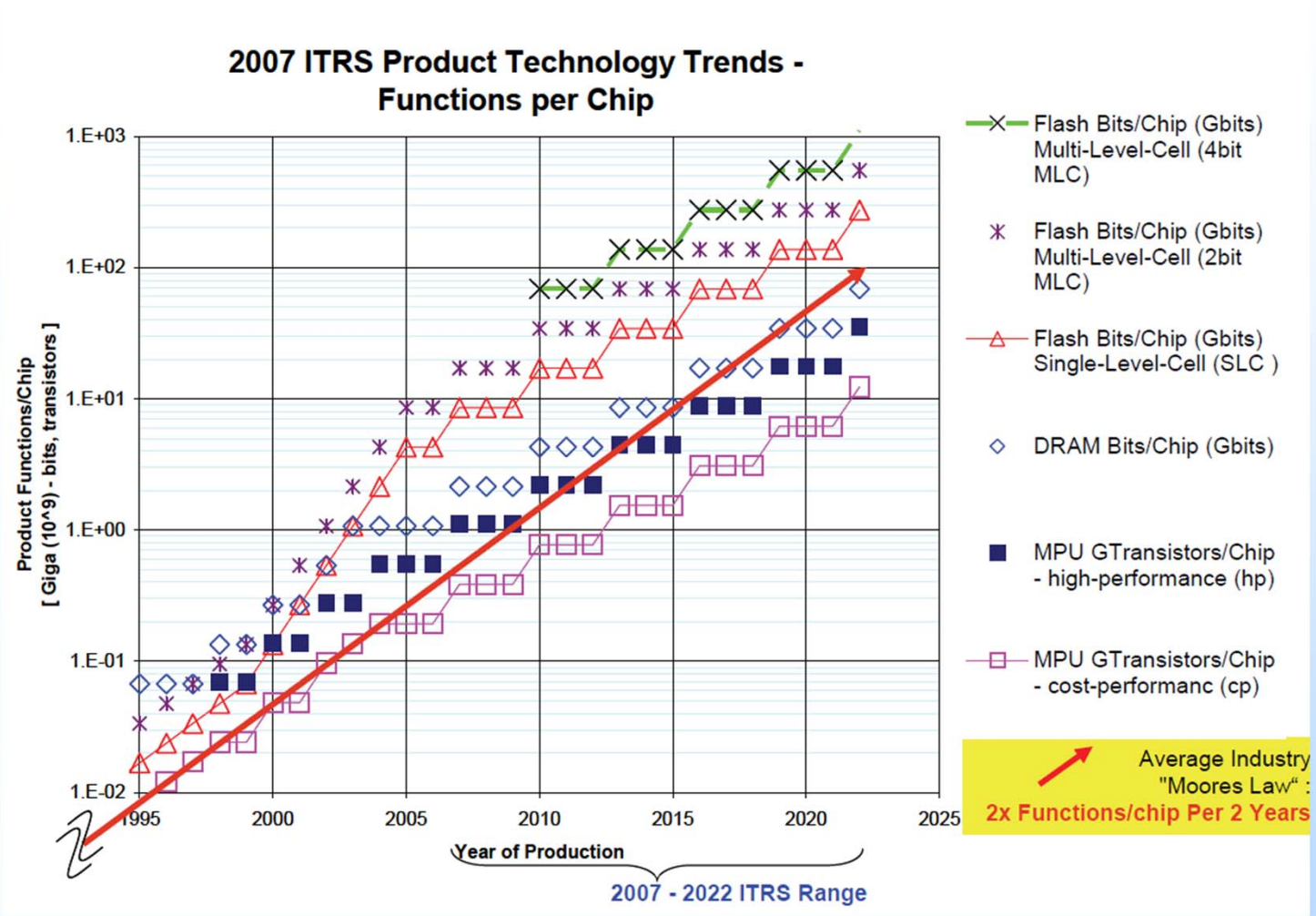
Ray Ladbury

Radiation Effects and Analysis Group
NASA Goddard Space Flight Center
Greenbelt, MD 20771 USA

Acknowledgements

- Defense Threat Reduction Agency
- GSFC Radiation Effects and Analysis Group
  - Dakai Chen, Megan Casey, Alyson Topper, Tim Irwin and Joe Portner
- Micron Technology, Inc.
  - Brian Bradford and Daniel Craig
- Samsung.
  - Jaci Chang
- Triad Spectrum
  - Ray Chao, Gary Ng, Mike Mikula

SDRAMs—Still on the Bleeding Edge



– **How do we ensure reliability in space of devices that push the envelope even on Earth?**

Introduction

- **Terrestrial: DDR SDRAMs have a variety of failure modes**
  - **Electromigration (EM) and Stress migration (SM), Hot Carrier Effects (HCE), Time-Dependent Dielectric Breakdown (TDDB), and so on**
    - **Exacerbated by increased voltage and temperature—also the basis for accelerated life/reliability testing**
- **Space Radiation Environments pose added challenges**
  - **Total-Ionizing Dose (TID) Degradation**
  - **Single-event Effects (SEE)**
- **NEPP approach: Start with Industry Standards and supplement/improve where needed**
  - **Industry reliability testing well developed**
  - **TID testing standards yield good results**
  - **But…what if TID/SEE performance and wear out are not independent?**
- **This year's task: Look for evidence of synergy between TID damage and damage during reliability testing.**

Introduction

- **Strategy: Use Triad Spectrum DDR2/3 tester to measure degradation in Dual In-Line Memory Modules (DIMMs) exposed to TID, thermal and overvoltage stresses**
  - **Examine synergies between standard reliability tests and TID**
  - **Test parts are 1-Gbit DIMMs from Samsung and Micron**
    - **Micron DDR2—MT47H128M8HQ, DDR3—MT4JTF12864AZ**
    - **Samsung DDR2—M379T2863FB3-CF7, DDR3—MV-3V2G4 modules**
  - **Flight projects are using DDR2 now; expect DDR3 soon**
- **Collaboration/Cooperation**
  - **Micron has facilitated reliability test development**
  - **Waiting on similar information from Samsung**
  - **Triad Spectrum very helpful in developing new test capabilities**
  - **Looking at potential for collaboration with JPL combining reliability and TID testing**

SDRAM Subtask

Description:

– This is a continuation task for evaluating the effects of scaling (<100nm), new materials, etc. on state-of-the-art (SOTA) mass volatile memory (VM) technologies—mainly SDRAM. The intent is:

– To determine inherent radiation tolerance and sensitivities,

– Identify challenges for future radiation hardening efforts,

– Investigate new failure modes and effects, and

– Provide data to DTRA/NASA technology modeling programs.

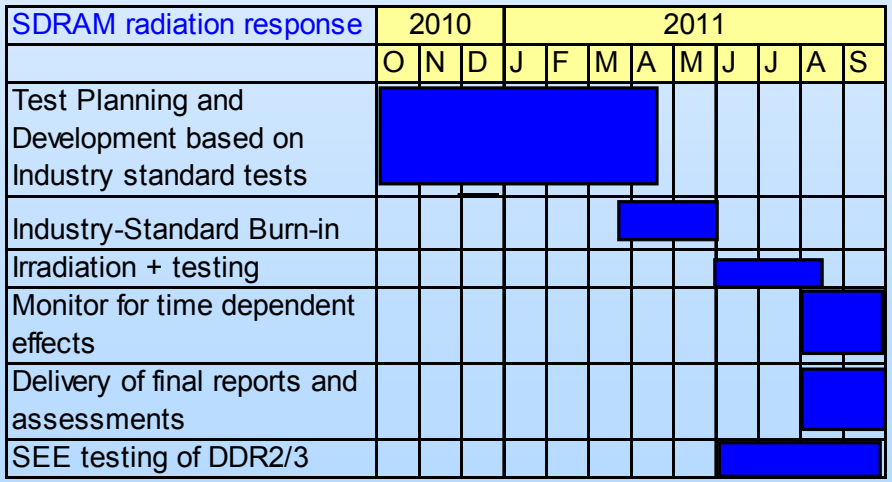
–Testing includes total dose, single event (proton, laser, heavy ion), proton damage (where appropriate) and reliability. Test vehicles will include a variety of volatile memory devices as available, including DDR2 SDRAMs and commercial SRAMs… and DDR3 devices

–Emphasis for 2011 will be synergistic degradation resulting from aging and total ionizing dose (TID) response, but SEE testing also planned.

FY11 Plans:

– Probable test structures
  – DDR2 and DDR3 SDRAM from Samsung and Micron
  – DDR2 SDRAMs from Elpida (courtesy of 3D Plus)
  – TID/reliability tests will use the new Triad Memory tester
– Test focuses
– Evaluate potential synergistic effects of TID and SDRAM aging
    – Use thermal and voltage acceleration methods
    – Evaluate degradation due to aging/stress
    – Compare TID response of stressed to unstressed parts
– SDRAM SEE response for current generation DDR2 and DDR3 SDRAMs if funding, tester capability and time allow.

Schedule:



Deliverables:

-Updated guidelines for Solid-State Recorders (SSRs) and other SDRAM applications
- Test reports
-Report evaluating susceptibility of DDR2 and DDR3 SDRAMs to TID degradation, along with any evidence for synergistic effects with other degradation mechanisms (reliability issues).

NASA and Non-NASA Organizations/Procurements:

Beam procurements: TAMU, IU, NRL, GSFC/REF
Partners: 3D Plus, JPL, Micron, Samsung

Goals

- **Assess TID capability of SOTA DDR2 and DDR3**
  - **Current generation parts ~48 nm min. feature size**
  - **Previous tests (~90 nm) failure occurred ~150-250 krad(Si)**
- **Independently assess reliability/life testing**
  - **Work with vendor to reproduce standard test regime**
  - **Assess degradation in performance and functionality**
- **Look for Evidence of Synergy**
  - **Rationale—TID, TDDB and HCE all depend on and modify oxide properties**
  - **Also, all these stresses erode margins, affect timing—critical for operation of DDR devices**

Expected Impact to Community

- **Increase confidence for use of DDR devices in space environments**
  - **Validate life testing for conditions of use in space**
  - **Validate reliability test methods**
- **Identify new failure mechanisms**
  - **Reduce risk**
  - **Refine test methodologies and standards**
- **Determine whether TID and reliability can be assessed independently**
  - **Do synergies exist, and are they important for assessing reliability or for qualification strategies?**

Status/Schedule

- **Samsung**
  - **Initial TID testing of Samsung DDR2 completed**
    - **Biased and Unbiased**
    - **Test levels >1 Mrad(Si)**
  - **DDR3 DIMMs procured and being tested**
    - **Performing tests with Triad tester to establish baseline performance and timing criticality**
- **Micron DDR2 and DDR3 test parts procured**
  - **Currently undergoing baseline testing to establish pre-rad behavior and timing**
- **Life/Stress test regime under development**
  - **Working with Triad to exploit all capabilities of DDR2 and DDR3 testers**
    - **Triad has contributed new software to allow greater overvoltage**

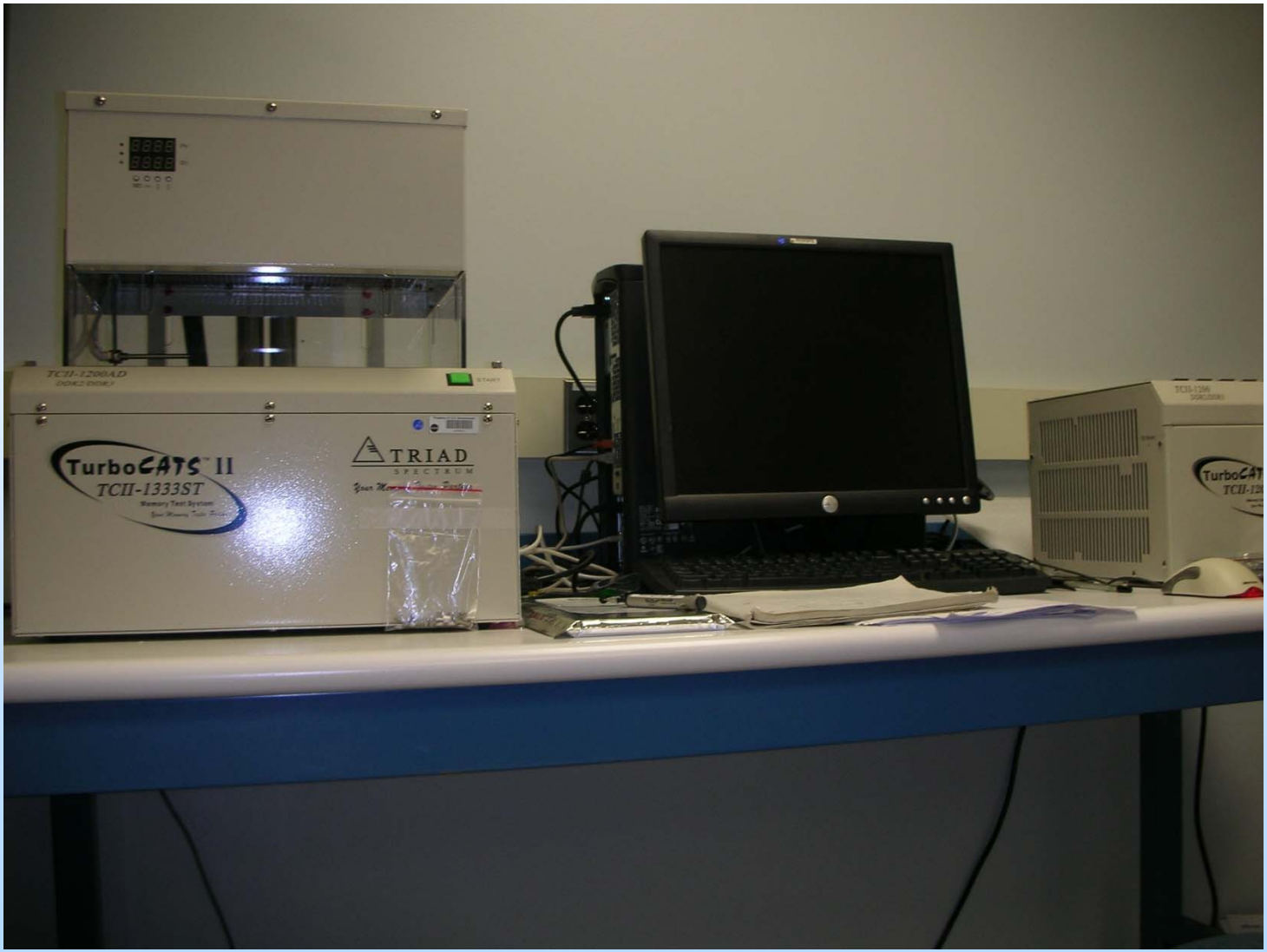
Technical Highlights

Getting to Know the Triad

- **Issues with testing DDR SDRAMs**
  - **Little insight into how parts are operating**
    - **Most parametric measurements amount to current drawn during a particular operation**
    - **Changed sensitivity to timing an also indicate degradation of Clock, Data, Address and other control signals**
    - **Failures may manifest for some tests or modes of operation even though others indicate no change.**
- **Triad Tester provides**
  - **Automatic measurement of operating currents**
  - **Control of timing parameters**
  - **Functional tests to investigate specific DDR functions**
    - **Marching Ones, Hammer test, Data retention, Autorefresh…**
- **Goal: Assess most diagnostic tests for DDR damage in the parts as well as DDR TID performance**

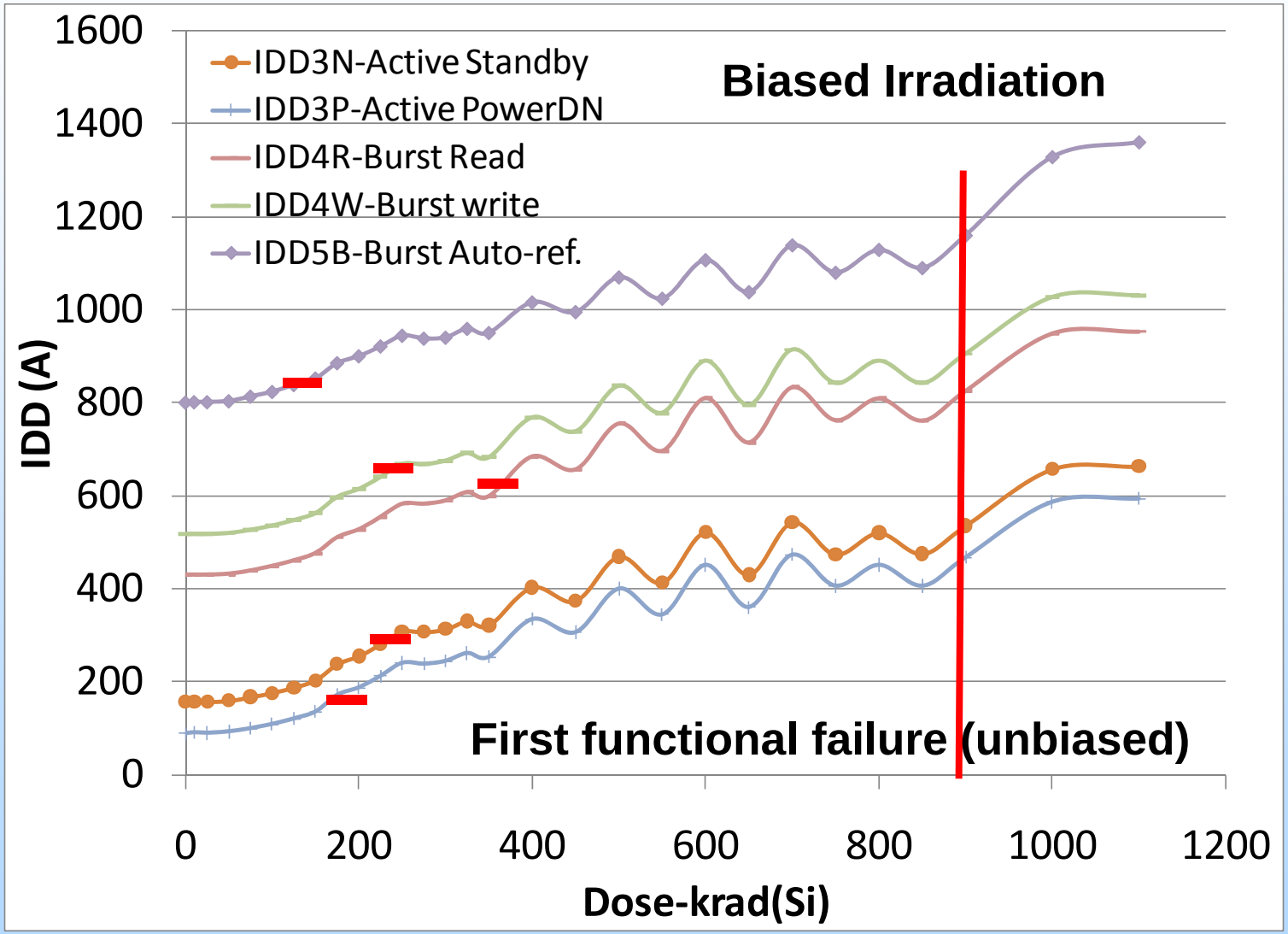
Technical Highlights

Getting to Know the Triad



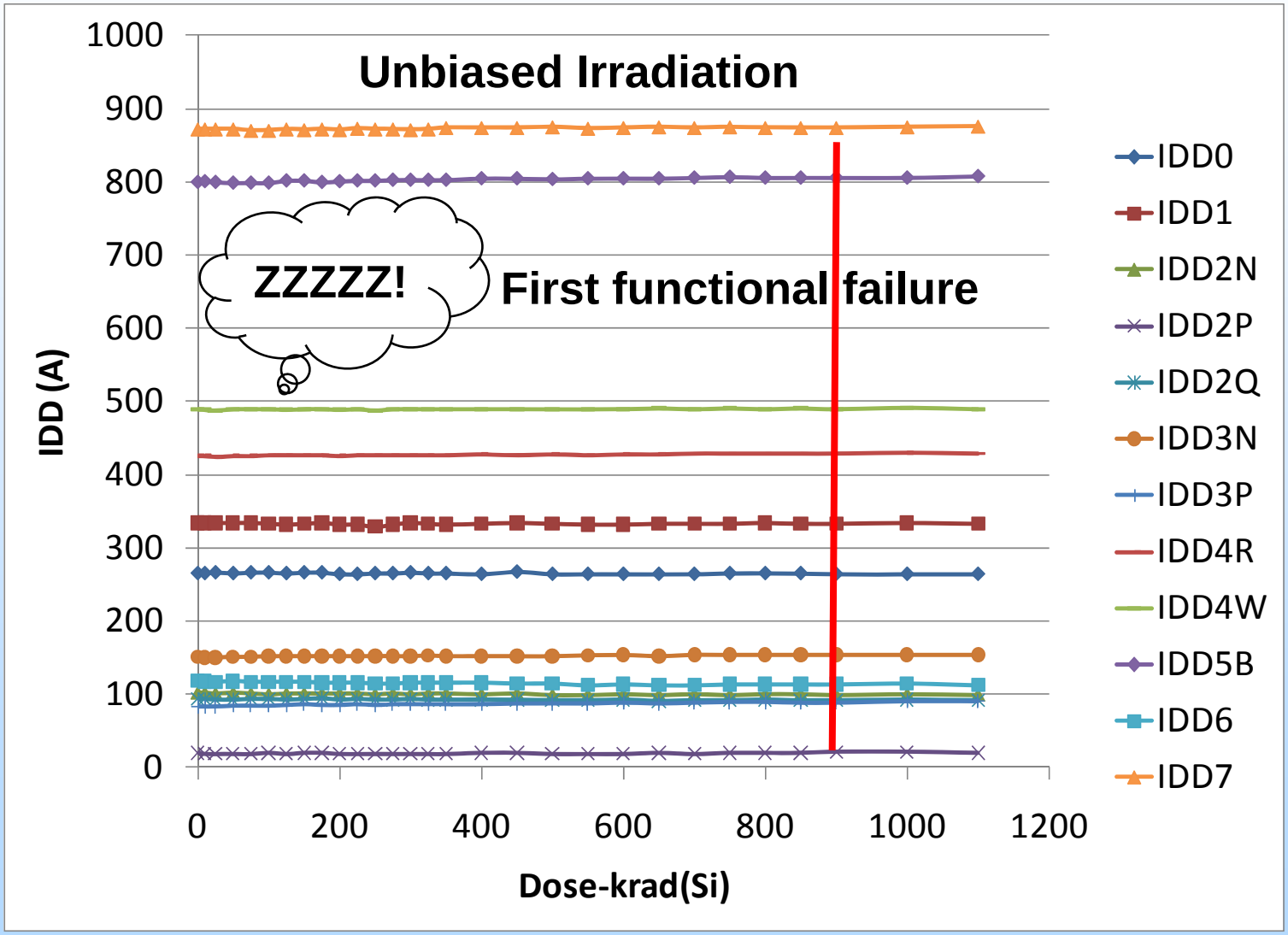
Technical Highlights

Samsung DDR2 SDRAM



Technical Highlights

Samsung DDR2 SDRAM



Technical Highlights

Samsung DDR2 SDRAM

- **Unbiased data—almost no change in operating currents**
- **But, first functional failure is for unbiased. What gives?**
  - **First failure occurs for Hammer test—repeated read/write cycles to the same memory location (900 krad(Si))**
  - **At 1 Mrad(Si) unbiased also fails Marching pattern**
  - **Biased—fails hammer test@ 1 Mrad(Si), Marching @ 1.1 Mrad(Si)**
- **Biased vs. unbiased**
  - **IDD behavior is very different**
  - **Functional failures occur at very similar levels**
  - **Functional failures LOOK like weak memory cells**

Combined Effects Testing

- **Industry standard accelerated life test protocol**
  - **Temperature Acceleration—Arrhenius factor=exp($-E_a/kT$)**
    - **Usually, 0.7 MeV<E_a <0.9 MeV**
    - **Some research contends E_a for SDRAMs is lower, suggesting thermal acceleration factors are low**
  - **Voltage Acceleration—Acceleration factor=exp($\beta V/V_0$)**
    - **β depends on the degradation mechanism**
      - **Hot-Carrier Effects have the highest acceleration factor (by far)**
    - **Issue: DDR SDRAMs have internal voltage regulation**
- **Other Considerations**
  - **Parts should be operated realistically during accelerated test**
    - **Clock Frequency**
    - **Logical State**
    - **Data Pattern/Retention**

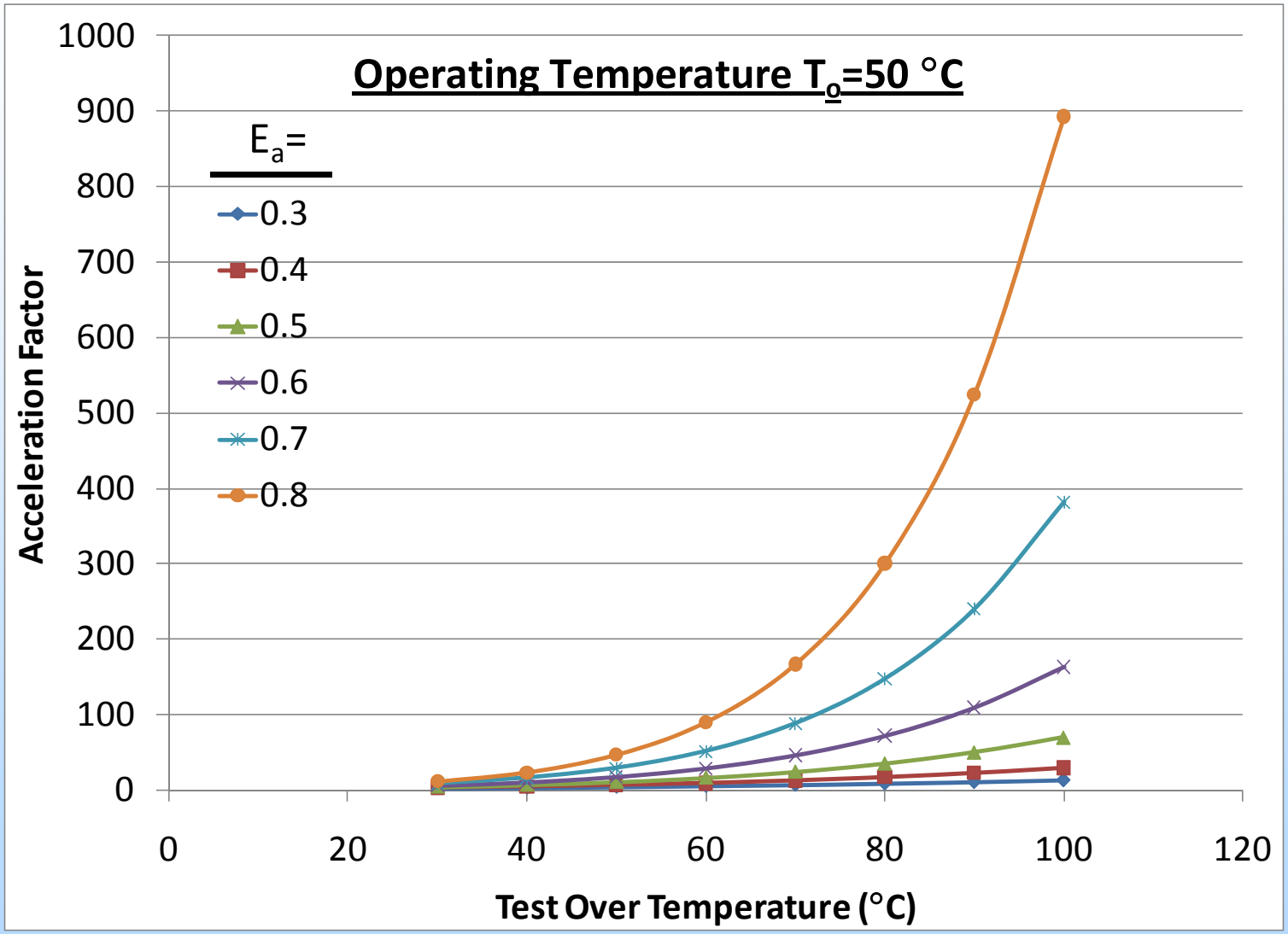
GSFC Acceleration Strategy

- **Use Triad tester to operate parts**
  - **Marching Pattern to simulate normal operation**
  - **Heater keeps parts at uniform temperature**
- **Challenges and Resolution**
  - **Triad was not designed for continual operation**
    - **Developed strategy to operate 20 hours on/4 hours off**
  - **Triad tester did not allow overvoltage**
    - **Worked with Triad engineers to give voltage control to user**
    - **Supply voltage must be raised to the point where internal voltage regulation fails**
  - **Tester heater only designed to operate up to 85 °C**
    - **Working to see if higher temperatures are feasible**

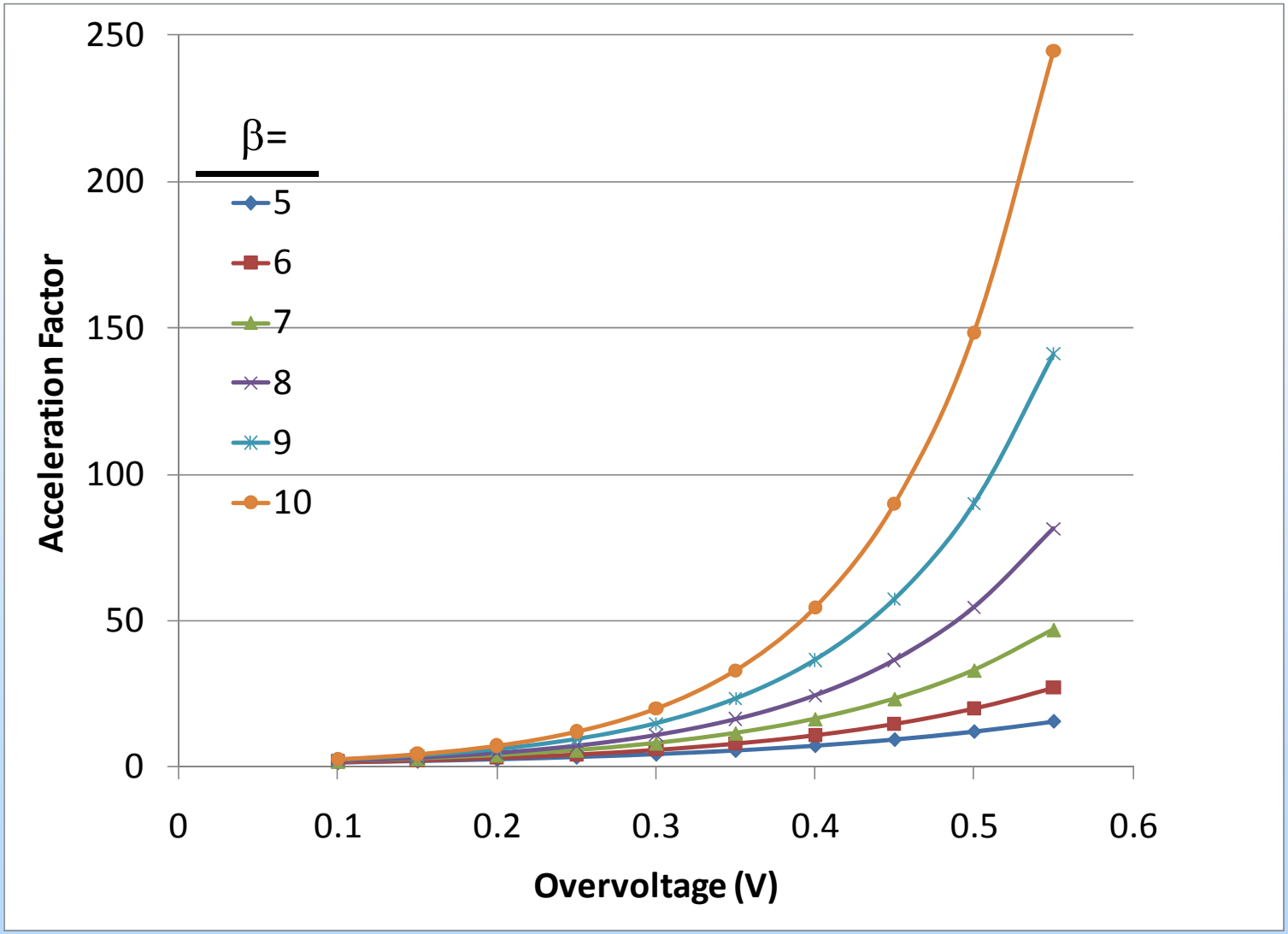
Acceleration Regime

- **Accelerated Test Time~1000-1500 hours**
  - **Operating life~10 years=87600 hrs**
  - **Total AF~87.6**
- **Temperature**
  - **Arrhenius model: $AF=\exp(E_a/kT_o-E_a/kT_t)=(\exp[\Delta(1/kT)])^{E_a}$**
    - **SDRAM E_a estimates 0.3 eV$\leq E_a \leq$ 0.9 eV, best estimates 0.6 eV$\leq E_a \leq$0.7 eV**
    - **For T_t=85 °C, T_o=25 °C, 7$\leq$AF$\leq$355, most likely AF~100**
    - **For T_t=85 °C, T_o=50 °C, 2.8$\leq$AF$\leq$23.6, most likely AF~11**
    - **Vendor T_t=125 °C, so AF~80 for T_o=50 °C—working to see if we can get there**
- **Voltage effect is more complicated**
  - **Different models for TDDB, EM and HCE, for example**
  - **General: $AF\sim\exp[\beta(V_t-V_o)]$, $5\leq \beta \leq 10 \rightarrow$ need $0.1V<\Delta V<0.4$ V**
  - **Caution: HCE increase rapidly with ΔV, so a large voltage acceleration factor may exaggerate these effects**

Temperature Acceleration



Voltage Acceleration



What Will the Results Mean?

- **Accelerated test goal: provide parts with "typical" aging damage to see if TID response differs from virgin parts**
  - **Using both thermal and overvoltage acceleration should do this**
    - **Caveat: Thermal and overvoltage effects not independent—e.g. HCE anneal**
    - **Argues for using moderate thermal and overvoltage rather than extremes**
- **Null result implies synergistic effects not significant**
  - **~900 krad(Si) hardness of DDR2s implies effects would have to be quite significant for TID to be a limiting factor**
- **Positive result implies synergy between TID and aging**
  - **Attempt to deconvolve the mechanisms**
    - **Look at overvoltage and temperature separately—Triad tester should be invaluable for localizing portions of device susceptible to synergy**
    - **Look at strength of synergy vs. voltage and temperature**
    - **Other questions: Effect of dynamic operation during irradiation?**
- **Product: Guideline for Bounding TID + Aging Damage**

Conclusions (so far)

- **Not surprisingly for deep submicron CMOS**
  - **DDR2/3 parts show good TID hardness**
  - **Static Bias seems to affect peripheral/support/control circuitry rather than memory cells**
    - **Affects mainly standby/Power Down and Burst operation**
    - **Difficulty of controlling devices makes dynamic operation during irradiation challenging**
- **Acceleration factors to simulate 10-15 years operation achievable with moderate overvoltage and temperature**
  - **Want accelerated test to resemble high-temperature operating life test, but not over-emphasize any one failure mechanism**
  - **Accelerated degradation should resemble typical "aging"**
- **Preliminary results should be available end of FY11**