TERMINAL SOLDER DIP TESTING FOR CHIP CERAMIC AND TANTALUM CAPACITORS

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ABSTRACT
Thermal shock (TS) associated with soldering conditions is one of the major causes of first turn-on failures of tantalum capacitors and fracturing of Multilayer Ceramic Capacitors (MLCCs) that results in latent defects and might cause failures with time during application. The probability of damaging of the parts and failures are typically greater for manual soldering that is often used to assemble circuits for high-reliability space systems. This work analyzes deficiencies of the existing resistance to soldering heat tests and describes a terminal solder dip (TSD) testing that is argued to be the most adequate test simulating TS conditions caused by manual soldering. Different types of MLCCs and tantalum capacitors, including regular chips, microchips, and polymer cathode capacitors were used in this study. Results of TSD testing are described and analyzed to evaluate the robustness of parts to soldering stresses, demonstrate the effectiveness of the test, and select adequate test conditions. Mechanisms of fracturing of MLCCs and damage to tantalum capacitors caused by soldering are discussed.

INTRODUCTION

Damage to surface mount ceramic and tantalum capacitors during soldering is considered one of the prime reasons of failures of these parts during operation. In case of ceramic capacitors, soldering-induced thermal shock (TS) creates transient mechanical stresses that might exceed the strength of materials and result in cracking [1]. Thermo-mechanical stresses in tantalum capacitors might cause damage to thin tantalum pentoxide dielectric that reduces breakdown voltages and results in first turn-on failures of the parts [2-3].

Although soldering-induced damage might not lead to immediate failures of capacitors, it can cause degradation of characteristics with time (hours to months) resulting eventually in field failures. In this regard, microcracks in capacitors generated during assembly can be considered as a "time bomb" [4] that causes increased leakage currents, opens, or intermittent contacts as degradation develops or cracks propagate with time during application.

Cracking in ceramic capacitors is an old problem. It appeared in the 1970s when the first surface mount technology (SMT) chip capacitors were introduced to the market and began to be employed in NASA applications [5-6]. According to J. Maxwell [7] this problem will continue to be with us in the foreseeable future. Two main factors contribute to the problem: brittleness of ceramic materials and thermal and mechanical stresses associated with the assembly process. Both factors are intrinsic to chip ceramic capacitors and explain the persistence of the problem. A breakdown of about 40 different mechanical failures of capacitors shows that 25% were caused by flex cracking, 23% by thermal shock cracking, and 34% were due to manufacturing defects [8-9].

Volumes of literature have been written over the years about cracks in ceramic capacitors, mechanisms of their formation, and factors affecting the probability of their occurrence. Based on these studies, a substantial progress in the quality of materials and manufacturing processes has been made. This, as well as development of detailed application guidelines, resulted in a significant decrease in cracking-related failures and allowed for application of chip capacitors in high-reliability systems including space instruments. Still, failures related to cracking in capacitors after assembly onto printed wiring boards (PWB) do occur, and further analysis and improvement in screening and qualification techniques are necessary.

To decrease the probability of fracturing during soldering, one should both reduce the level of stress and select capacitors with high resistance to soldering stresses. Assuring that capacitors are not abused during soldering is the purpose of the workmanship control that should ensure compliance with the existing guidelines for assembly. These guidelines are based on decades of industry practice that are well-developed and documented. However, the level of testing that is typically used to assure the robustness of MLCCs to soldering stresses is not sufficient.

Manual soldering of capacitors, which is often used during assembly or rework for space projects, might be more stressful compared to the standard solder reflow processes due to a greater temperature gradients in the part and is known to have a high risk of damaging the parts that is increasing with the size of capacitors [7]. All manufacturers are warning against manual soldering of large MLCCs and

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provide detailed guidelines to reduce the risk of cracking in case a rework or hand-soldering have to be used.

Two types of qualification tests that evaluate the robustness of MLCCs to soldering stresses are used in the relevant military standards: thermal shock testing and resistance to soldering heat (RSH) test. Analysis of the currently used requirements to TS testing shows that they do not create any substantial temperature gradients in chip capacitors and do not simulate soldering conditions. Existing requirements for RSH testing mostly follow the guidelines for safe soldering conditions, do not represent typical manual soldering stresses, and are not sufficient to reveal potentially weak lots of capacitors.

A solder dip test as it is described in MIL-STD-202 provides the most severe thermal shock conditions that are close to stresses related to manual soldering. However, clamping of the parts or mounting in a fixture for plunging into molten solder might have a strong effect on test results [1]. Plunging a part into a solder pot that is clapped with tweezers of different type and size, unknown pressure, and position might change test results substantially. A recent GEIA-STD-0006 (2008) [10] developed with the purpose of setting industry-wide requirements for solder dip to replace the finish on electronic parts emphasizes that the controls needed on a manual dip process are not well enough understood to be included in an industry standard.

In this work, a terminal solder dip testing technique that closely simulates TS conditions during manual soldering is suggested. Experimental results obtained using this technique for various solid chip tantalum and ceramic capacitors are described, and conditions for testing of the parts intended for manual soldering are recommended.

EXPERIMENT

During TSD testing one terminal of each capacitor is clamped in a fixture and another dipped for 5 seconds into a pot of molten solder preheated to a certain temperature. After dipping the part cools at room conditions for ~3 minutes. In most existing guidelines for manual soldering, the temperature of the soldering iron is limited to ~300°C; however, in many cases in practice the temperature can reach 350°C and higher. For this reason, in our experiments, the set temperature varied from 300°C to 350°C. Solder dipping and cooling procedures were carried out 10 times for each part after which the parts were inspected under microscope and tested electrically. For tantalum capacitors, anode and cathode sides were tested separately. From 10 to 20 samples were used to characterize capacitors to the TSD stress. Throughout the testing, the parts were periodically examined optically using the vicinal illumination technique [11].

Electrical testing included measurements of capacitance (C), dissipation factor (DF), equivalent series resistance (ESR), leakage current (DCL), and breakdown voltages (VBR). Both surge current and scintillation breakdown voltages [12] were measured for tantalum capacitors. To increase the sensitivity to cracking, DCL measurements for MLCCs were carried out at twice-rated voltages. For tantalum capacitors leakage currents were monitored at rated voltages and DCL readings were taken after 1,000 seconds of electrification.

A methanol test was used to reveal cracking of ceramic capacitors [13]. During this testing, the parts were preheated to 85°C for 15 minutes and then immersed into methanol at room temperature for 3 minutes. DCL measurements were repeated after removal from the methanol bath and drying the part for ~1 minute.

TEST RESULTS FOR TANTALUM CAPACITORS

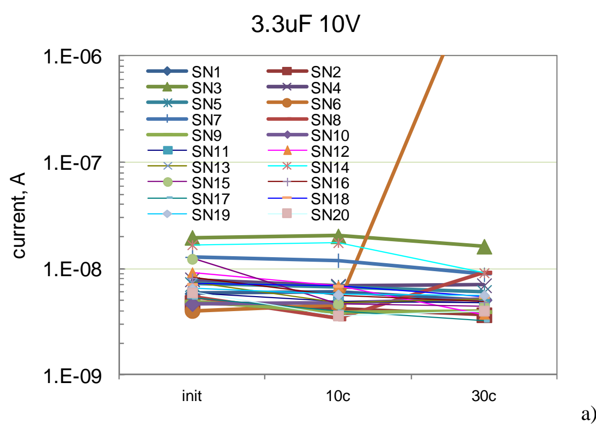
Six types of commercial and six types of military-grade chip tantalum capacitors were used in this study (see Table 1). In the first set of tests, three part types (Gr.1, 2, and 3) were tested at 300°C (TSD_300). No substantial degradation of AC (C, DF, ESR) and DC (DCL and VBR) characteristics were observed except for one part in 4.7 μF/10V group of capacitors had increased dissipation factor.

Table 1. TSD test results for tantalum capacitors.

Gr.	Part Type	C, μF	VR, V	Test cond.	AC	DCL	VBR	Results/Comments
1	CWR09	3.3	10	TSD_300, 10c	0/20	0/20	0/20	No degradation of AC and DC characteristics
2	Commercial	4.7	10	TSD_300, 10c	**1/20**	0/20	0/20	1 part increased DF
3	CWR11	15	10	TSD_300, 10c	0/20	0/20	0/20	No degradation of AC and DC characteristics
4	CWR11	22	6	TSD_300, 10c TSD_300, 30c	0/20 0/20	0/15 0/15	- 0/15	No degradation of AC and DC characteristics
5	Com	22	15	TSD_300, 10c TSD_300, 30c	0/20 0/20	0/20 0/20	- 0/20	No degradation of AC and DC characteristics
6	CWR11	15	10	TSD_300, 10c TSD_300, 30c	0/20 0/20	0/20 0/20	- 0/20	No degradation of AC and DC characteristics
7	CWR09	3.3	10	TSD_300, 10c TSD_300, 30c	0/20 0/20	0/20 **1/20**	- 1/20	1 DCL failure and another part had low VBR
8	Commercial	33	35	TSD_300, 10c TSD_300, 30c	0/20 0/20	0/20 0/20	- 0/20	No degradation of AC and DC characteristics
9	Commercial	220	6	TSD_300, 10c TSD_300, 30c	0/20 0/20	0/20 0/20	- 0/20	No degradation of AC and DC characteristics
10	CWR09	6.8	35	TSD_350, 10c	0/20	**3/20**	0/20	Degradation of DCL
11	Commercial	6.8	35	TSD_350, 10c	0/20	0/20	0/20	No degradation of AC and DC characteristics
12	Commercial polymer	1	50	TSD_300, 10c; TSD_325 10c; TSD_350, 10c	0/20 **6/20** **18/20**	0/20 **2/20** 0/20	0/20 0/20 0/20	Degradation and failures of DCL and ESR

To increase the level of stress in the second set of tests, the number of cycles at TSD_300 was increased to 30. AC characteristics and DCL were measured after 10 and 30 cycles, and breakdown voltages were measured after 30 cycles. No degradation or failures were noticed in five out of six part types; however, one lot of CWR09 capacitors had two out of 20 parts with substantially degraded characteristics after 30 TSD_300 cycles.

Examples of variations of leakage currents in capacitors during solder pot cycling for two types of capacitors are shown in Figure 1. No degradation of DCL was observed in all capacitors except for one sample out of 20 from 3.3 μF 10 V CWR09 group that failed DCL measurements after 30 cycles.



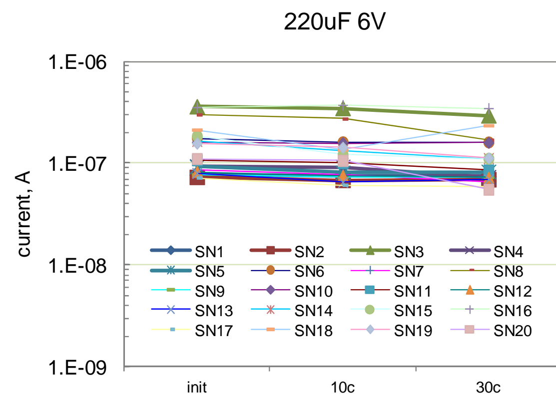


Figure 1. Variations of leakage currents during solder pot cycling test for 20 samples from Gr.1 (a) and Gr.9 (b) tantalum capacitors. Different marks correspond to different sample numbers.

Distributions of surge current breakdown voltages and scintillation breakdown voltages for 2.2 μF 15 V and 3.3 μF 10 V capacitors measured before and after 30 solder pot cycles are shown in Figure 2. Analysis of data for 2.2 μF 15 V capacitors shows no significant difference before and after TSD for both distributions. However, one sample out of 10 tested 3.3 μF 10 V capacitors had a substantially reduced surge current breakdown voltage. Additional tests showed that capacitors from this lot degraded after manual soldering tests during which the parts were resoldered onto a PWB three times with periodical measurements of leakage

currents. Results of the TSD testing confirmed that the lot of 3.3 µF 10 V CWR09 capacitors has high susceptibility to soldering-induced stresses.

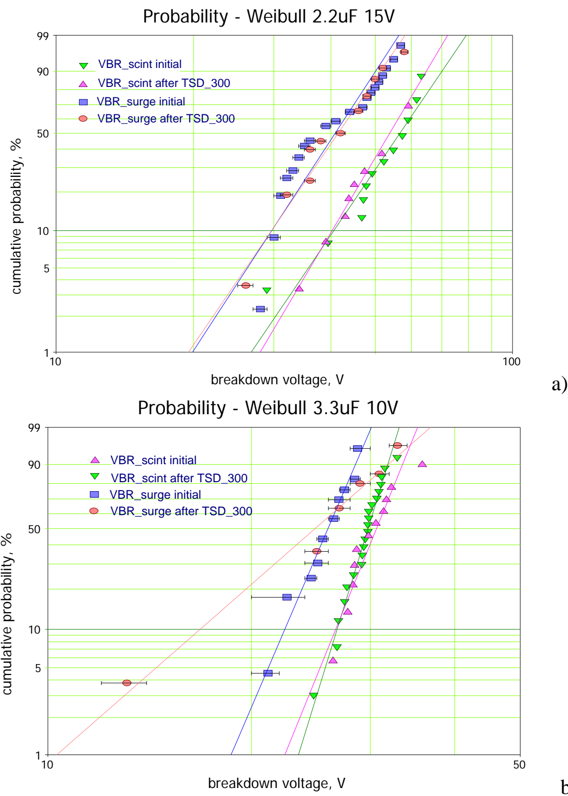
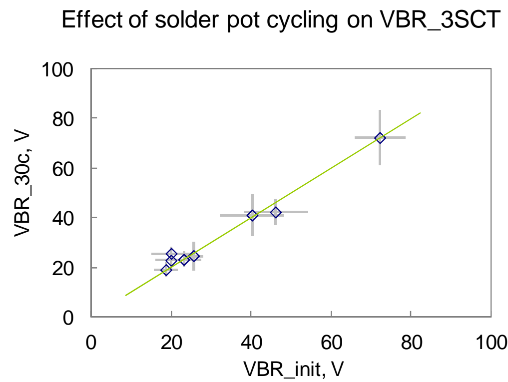


Figure 2. Effect of 30 TSD cycles at 300°C on distributions of surge current (VBR_surge) and scintillation breakdown (VBR_scint) voltages for 2.2 µF 15V (a) and 3.3 µF 10V (b) capacitors.

All other tested lots had a tight correlation between surge current and scintillation breakdown voltages measured before and after TSD_300 (see Figure 3).

To further increase the level of stress, one military and one commercial type of 6.8 µF 35 V capacitors that referred below as type M and type C capacitors were tested at 350°C. Each test group had 20 samples. No degradation of AC characteristics or any substantial changes in breakdown voltages were observed. Leakage currents in type C capacitors measured before and after TSD_350 were closely correlated (see Figure 4). However, leakage currents in type M parts increased substantially, more that an order of magnitude for some parts, thus indicating degradation in tantalum pentoxide dielectric caused by the soldering simulation. This degradation did not result in exceeding the specified limit for DCL, hence the parts did not fail formally. However, a substantial increase in leakage currents indicates a potential impact on reliability of the parts.



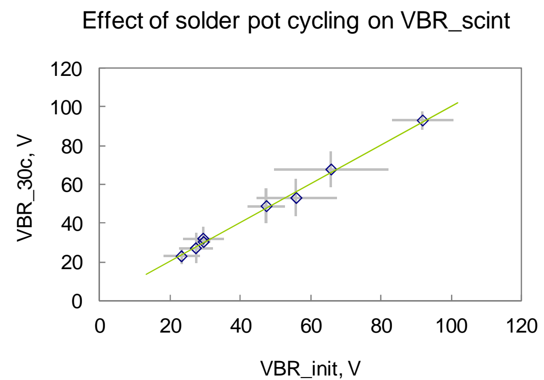


Figure 3. Correlation between surge current (a) and scintillation (b) breakdown voltages before and after TSD_300 for eight types of solid tantalum capacitors.

To evaluate the susceptibility of chip polymer tantalum capacitors to soldering thermal shock, 20 samples of 1 µF 50 V capacitors were stressed by TSD testing at temperatures of 300°C, 325°C, and 350°C. At each TSD condition the parts were stressed first at the anode side and then at the cathode side. Measurements showed relatively minor changes in capacitance, with some decrease in dissipation factors and substantial degradation of ESR that resulted in parametric failures (the specified limit for ESR is 0.3 Ohm) after TSD_350 (see Figure 5). Two parts had a significant, up to two orders of magnitude, increase in leakage currents. Analysis of data shows that more significant degradation of AC characteristics occurs during cathode side TSD testing compared to the anode-side.

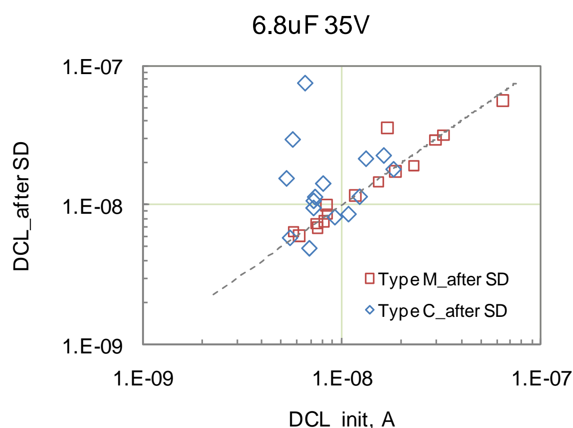
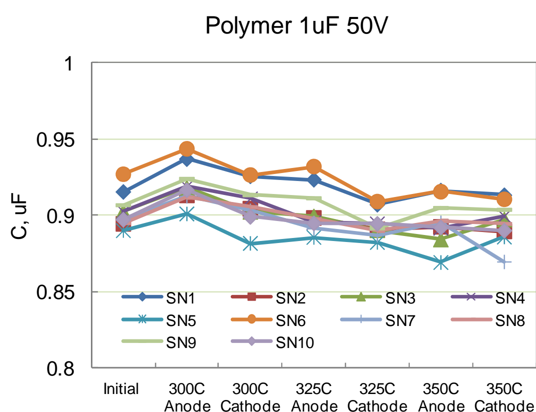


Figure 4. Effect of 10 solder dip cycles at 350˚C on leakage currents.



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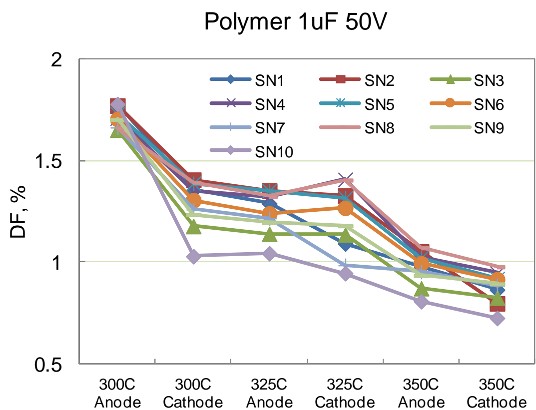

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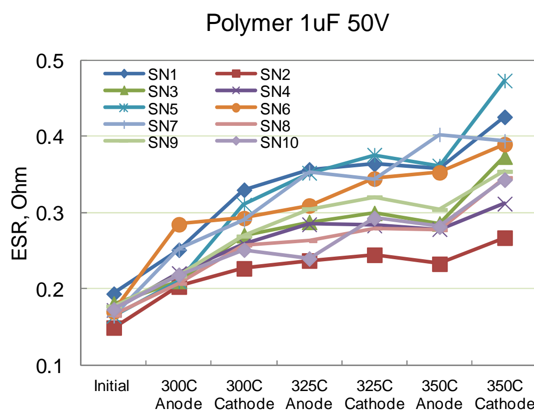

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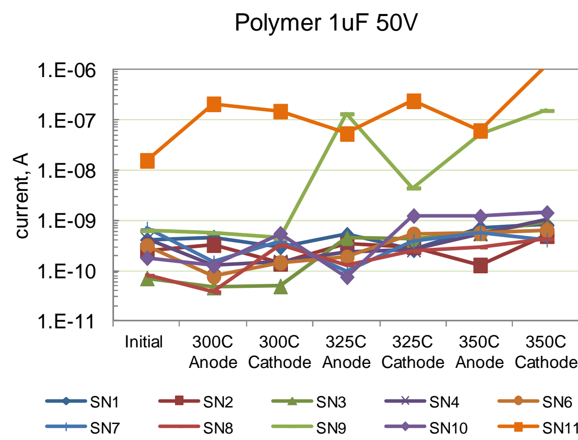


d)

Figure 5. Variation of capacitance (a), dissipation factor (b), ESR (c), and DCL (d) during terminal solder dip testing of 10 samples of 1 µF 50 V polymer tantalum capacitors. Different marks correspond to different sample numbers.

TEST RESULTS FOR MICROCHIP TANTALUM CAPACITORS

Microchip tantalum capacitors are manufactured using new technologies that allow for production of small size solid tantalum capacitors (down to EIA case size 0402) with volumetric efficiency much greater than for regular chip capacitors [14-15]. Seven types of microchip tantalum capacitors (see Table 2) manufactured by two vendors were tested using various TSD conditions. Capacitors from Gr. µ1 to Gr. µ4 were tested consequently by 10 TSD cycles at temperatures 300ºC, 325ºC, and 350˚C. Capacitors from Gr. µ5, µ6, and µ7 were stressed with 10 TSD cycles at the anode side and 10 cycles at the cathode side at 350˚C only.

Table 2. TSD test results for microchip tantalum capacitors.

Gr.	Mfr.	C, μF	VR, V	Size, LxWxH, mm³	Test cond.	AC	DCL	VBR	Results/Comment
μ1	A	33	10	3.2x1.6x1.6	TSD_300, 10ca+10cc TSD_325, 10ca+10cc TSD_350, 10ca+10cc	0/10 **1/10** **2/10**	0/10 0/10 0/10	0/10 0/10 0/10	Degradation of C, ESR, DF and DCL
μ2	A	33	10	2.1x1.4x1.4	TSD_300, 10ca+10cc TSD_325, 10ca+10cc TSD_350, 10ca+10cc	**1/10** **1/10** **1/10**	**1/10** 0/10 **2/10**	0/10 0/10 0/10	Degradation of C, ESR, DF and DCL
μ3	A	1	35	2.1x1.4x1.4	TSD_300, 10ca+10cc TSD_325, 10ca+10cc TSD_350, 10ca+10cc	**1/10** **3/10** **5/10**	0/10 **1/10** **2/10**	0/10 0/10 0/10	Degradation of ESR
μ4	A	10	10	2.1x1.4x1.4	TSD_300, 10ca+10cc TSD_325, 10ca+10cc TSD_350, 10ca+10cc	0/10 0/10 0/10	0/10 0/10 **1/10**	0/10 0/10 0/10	Degradation of DF and ESR at TSD_350
μ5	B	10	16	3.2x1.6x1.7	TSD_350, 10cc	0/20	0/20	0/10	No degradation
μ6	B	47	10	3.5x2.8x1.5	TSD_350, 10cc	0/20	0/20	0/10	No degradation
μ7	B	4.7	6.3	1.6x0.85x0.85	TSD_350, 10cc	0/20	**1/20**	0/10	Degradation of DCL

Capacitance in parts from Gr. μ1 and Gr. μ2 decreased substantially through the testing and after TSD_350 lost on average 7.5% and 17.6% of the initial values. Variations of capacitance in Gr. μ3 and Gr. μ4 parts were less, ~1.4% and 0.5%.

A significant, on average by 62% and 127%, increase in dissipation factors was observed in Gr. μ1 and Gr. μ2 capacitors, and one out of ten parts in Gr. μ2 failed DF after 300˚C testing. Values of ESR and DF for capacitors from Gr. μ4 degraded ~ 30% after 350˚C testing, but all parts remained within the specified limits. No substantial variations in DF were observed in Gr. μ3 parts up to 325˚C; however, after testing at 350 ºC two out of 10 parts increased DF significantly and approached the specified limit of DF_{max} = 8%.

Variations of ESR and DCL through the testing for Gr. μ1 and Gr. μ4 capacitors are shown in Figure 6. Equivalent series resistances gradually increased for Gr. μ1 and Gr. μ2 parts rising from 40% to 230% for Gr. μ1 and more substantially, from 1.7 to 5.5 times for Gr. μ2 capacitors.

Due to a more stringent requirement for Gr. μ1 (1 Ohm maximum compared to 5 Ohm max for Gr. μ2), one part in this group failed after 325˚C and another one after 350˚C testing. The part that failed DF in Gr. μ2 failed also ESR increasing to approximately 8 Ohm after 300˚C and up to 20 Ohm after 350˚C test. This substantially exceeds the specified limit of 5 Ohm.

One out of ten parts in Gr. μ3 failed ESR after 300˚C, two more failed after 325˚C, and 50% of the parts failed with ESR in the range from 9 Ohm to 33 Ohm after testing at 350˚C. Contrary to that, all parts in Gr. μ4 had ESR well below the 6 Ohm limit even after 350˚C testing. Most of the capacitors in this group were stable up to 325˚C and showed some degradation (from 10% to 50%) only after cathode side testing at 350˚C. For the majority of parts exhibiting degradation, variations of ESR were greater during cathode side solder dipping compared to the anode side. This suggests that, similar to regular chip capacitors, degradation of AC characteristics in microchip capacitors is due to formation of cracks and delaminations in the cathode layers.

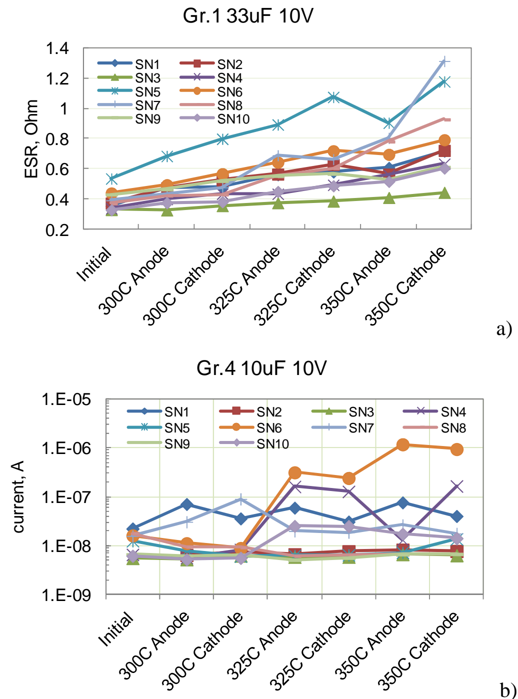


Figure 6. Variations of ESR (a) and DCL (b) through the terminal solder dip testing at 300˚C, 325ºC, and 350˚C for 10 samples in each group. Different marks correspond to different sample numbers.

All parts in Gr.1 had leakage currents below the specified limits even after TSD_350. However, two capacitors increased DCL more than 5 times after 350°C anode-side testing. Most of Gr. μ2 capacitors had some increase of leakage currents through the testing and DCL variations were much more significant during anode side dipping compared to the cathode-side. One part in Gr. μ2 failed marginally the maximum allowable DCL after 300°C testing and another one failed after 350°C testing. Most of the parts in Gr. μ3 had relatively stable leakage currents, but one part failed after 325°C and another after 350°C testing. Only one part failed marginally at ~ 1.05 μA after TSD_350 in Gr. μ4, but two capacitors increased DCL more than an order of magnitude after anode-side testing at 325°C.

Results of TSD_350 testing of capacitors from Gr. μ5, μ6, and μ7 showed no failures or notable parametric degradations. Capacitance, dissipation factor, ESR, and leakage currents remained stable and did not change any substantially compared to the pre-stress levels. Some decrease in capacitance (~ 5%) most likely is due to moisture desorption from pores at the Ta_2O_5/manganese interface [16] and is common for all chip tantalum capacitors. One out of 20 capacitors in Gr. μ7 increased DCL approximately 4 times; however, the level of leakage current remained within the nanoampere range, which is well below the specified limit of 160 nA.

To assess the effect of solder dip stresses on breakdown voltages, all parts from 7 groups were subjected to step stress surge current test after 350°C TSD stress. None of the capacitors failed at the rated voltages and no substantial variations in the distributions of VBR were observed. A close correlation between the initial and post TSD_350 values of breakdown voltages is shown in Figure 7. This indicates that microchip tantalum capacitors are capable of withstanding manual soldering thermal shock conditions.

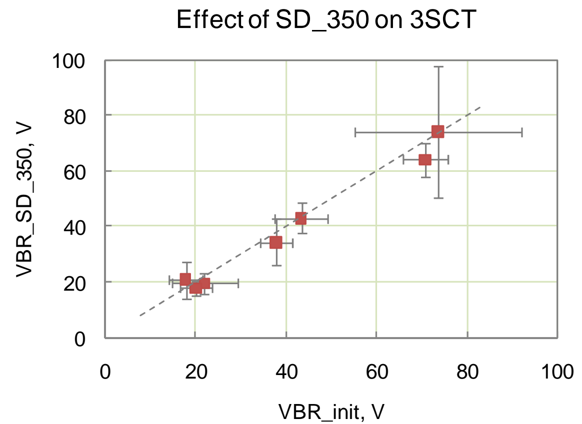


Figure 7. Correlation between initial and post-350°C terminal solder dip testing surge current average breakdown voltages.

TEST RESULTS FOR CERAMIC CAPACITORS

Twelve different lots of X7R MLCCs from five vendors were used in this study (see Table 3). Lots LT11 and LT12 in this table refer to the same part types of CDR35 capacitors but with different lot date codes. Note that lot date code A of these parts was used to manufacture a circuit card and had multiple fractures after manual soldering. The board was reworked using the same soldering technique but another lot of capacitors (lot B), and this time no fracturing was observed. This could be due either to a more careful processing of the lot B or to a different susceptibility of these lots to TS-induced cracking. We hoped that TSD testing will help to answer this question.

Table 3. Terminal Soldering Dip test results for ceramic capacitors.

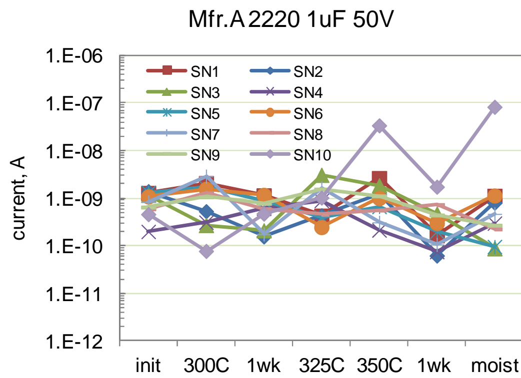
Lot	C, μF	VR, V	Mfr.	EIA size	Test cond.	AC	DCL	Visual exam	Results/Comment
LT1	1	50	M	2220	TSD_300 100c	0/20	0/20	0/20	No cracks or degradation
LT2	100	6.3	M	2220	TSD_300 100c	0/20	0/20	0/20	No cracks or degradation
LT3	2.2	50	C	2225	TSD_300 100c	0/20	0/20	0/20	No cracks or degradation
LT4	10	50	T	2220	TSD_300 100c	0/20	0/20	0/20	No cracks or degradation
LT5	47	16	T	2220	TSD_300 100c	0/20	0/20	0/20	No cracks or degradation
LT6	22	25	T	2220	TSD_300 100c	0/20	0/20	0/20	No cracks or degradation
LT7	1	50	A	2220	TSD_300 10c TSD_325 10c TSD_350 10c	0/10 0/10 0/10	0/10 0/10 **1/10**	- **2/10** **7/10**	A crack in the failed sample
LT8	1	50	B	2225	TSD_300 10c TSD_325 10c TSD_350 10c	0/10 0/10 0/10	0/10 0/10 0/10	- 0/10 0/10	No cracks or degradation
LT9	0.1	100	A	1825	TSD_300 10c TSD_325 10c TSD_350 10c	0/10 0/10 0/10	0/10 0/10 0/10	- 0/10 0/10	No cracks or degradation
LT10	0.1	100	P	1825	TSD_300 10c TSD_325 10c TSD_350 10c	0/10 0/10 0/10	0/10 0/10 0/10	- **2/10** **4/10**	Shallow cracks did not cause DCL failures
LT11	0.1	100	C, lot A	1825	TSD_350 10c	0/20	**1/20**	**11/20**	Substantial cracking and electrical failures
LT12	0.1	100	C, lot B	1825	TSD_350 10c	0/20	0/20	0/20	No cracks or degradation

Ten samples from each lot were subjected to terminal solder dip tests at solder pot temperatures varying from 300°C to 350°C. In the first set of experiments 6 types of large (2220 to 2225 size) capacitors were tested by TSD_300 for 10 cycles initially and then, as no degradation was observed, the parts were stressed additionally for 20 and then for 70 TSD cycles, so the total number of cycles was 100. None of the parts had cracks or parametric failures during this testing. For this reason the following tests included TSD at solder pot temperatures of 325°C and 350°C.

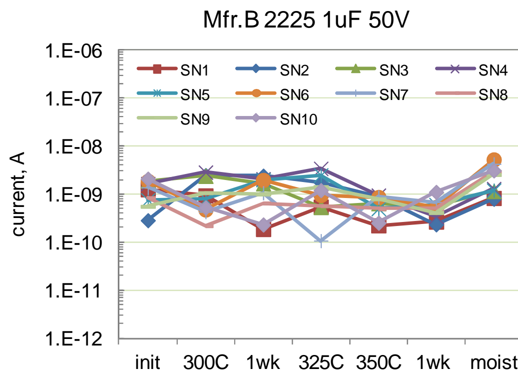
Figure 8 shows results of testing for LT7 and LT8 capacitors. No significant difference in leakage currents was observed as a result of TSD_300 test, and the currents remained stable after repeat measurements in one week of storage that was carried out to enhance moisture sorption in possible cracks. Then the test was carried out at molten solder temperatures of 325°C and 350°C. Ten additional solder dip cycles at 325°C did not result in degradation, but one out of ten samples in LT7 increased DCL almost by two orders of magnitude after TSD_350. All other parts in this group remained stable and did not degrade even after storage in humid environments (3 days at room temperature and 98% RH).

Capacitors from LT8, LT9, and LT10, had no changes in currents after 10 solder dip cycles at 350°C. Variations of capacitance and dissipation factors were consistent with the de-ageing process caused by exposure of the parts to temperatures exceeding the Curie point of X7R ceramic used in these parts (~125°C).

Microscopic examinations did not reveal any cracks in capacitors from LT8 and LT9 and confirmed the presence of cracks near terminals in the failed sample from LT7. Typical views of TSD-induced cracks in LT11 are shown in Figure 9. The cracks appeared as circular segments at the corners of capacitors at terminals that touched molten solder. Similar cracks are often observed after manual soldering of the parts.



a)



b)

Figure 8. Variations of leakage currents during terminal solder dip testing for 10 samples of LT7 (a) and LT8 (b) 1 μF 50V capacitors. Different marks correspond to different sample numbers.

One part from LT11 failed DCL measurements after TSD_350 and visual examinations showed 55% fracturing in parts from lot A and 0% for lot B. Lot A failed also post_TSD methanol testing. This confirms that excessive fracturing of capacitors from lot A that was observed after manual soldering is due to insufficient robustness of these parts.

The results show that different lots of MLCCs, including those manufactured and tested to military specifications, might have different susceptibility to fracturing under the same manual soldering conditions. It confirms also that TSD testing is an effective technique for selecting parts that might sustain TS stresses associated with manual soldering.

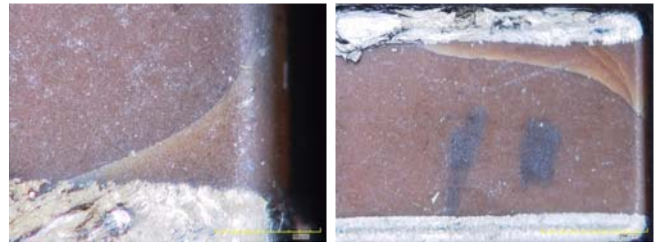


Figure 9. Cracks induced by the terminal solder dip testing at 350°C in LT11 capacitors.

DISCUSSION

Simulations of soldering-induced stress by TSD testing showed that normal quality tantalum capacitors can sustain multiple thermal shocks at a solder temperature of 300°C. The observed failures were lot-related and occurred mostly at temperatures exceeding 300°C. Analysis showed that tantalum capacitors might fail in two modes: catastrophic that results in a sharp increase of leakage currents or decrease in breakdown voltages, and parametric that is mostly due to an increase of ESR. Both types of failures can be explained by thermo-mechanical stresses that are caused by mismatch of the coefficients of thermal expansion (CTE) between the molding compound and tantalum anode slug. In the first case these stresses result in damage to a Ta_2O_5 dielectric, and in the second, in formation of delaminations between cathode layers. The first type of failures occurs mostly during anode-side thermal shocks, and the second is prevailing during cathode-side TSD testing. In the case of polymer tantalum capacitors, ESR failures might be also due to degradation of electrical characteristics of the conductive polymer at high temperatures.

Results of measurements of thermo-mechanical characteristics of tantalum slugs and plastic packages carried out in the course of this work showed that average CTE of the slug is 6.2 ppm/°C, which is close to literature data for tantalum (6.3 ppm/°C). Measurements on the packages resulted in values of CTE that depending on part type varied from ~ 6.5 ppm/°C to ~ 15 ppm/°C. Considering high stiffness of the tantalum slug, the difference between the CTE for the package and anode slug might result in substantial internal stresses in the part that can cause fracture of a relatively fragile sponge-like structure of the slug. Failures related to cracking of the Ta_2O_5 dielectric are more likely to happen during anode-side soldering induced thermal shocks.

Degradation of ESR is likely a result of stress-induced delamination between the cathode layers. This delamination and fracturing is more likely to occur between the graphite layer that cover manganese cathodes and silver epoxy because this interface have a relatively poor adhesion due to the presence of thin silicone film that is used to improve moisture resistance of the parts.

Similar to regular chip tantalum capacitors, degradation of capacitance in microchips after TSD can be explained by desorption of moisture from the Ta_2O_5/manganese interface. It was shown in our previous work [16] that moisture accumulation at the surface of tantalum pentoxide dielectric can increase capacitance in different parts by 3% to 13%. These variations are reversible and occur even at relatively low levels of humidity that are typical for storage at room conditions. Losses of capacitance during TSD testing of more than ~ 15% indicate excessive voiding and indicate insufficient control over the cathode formation process.

The results show that microchip tantalum capacitors can be robust enough to sustain severe thermal shock stresses associated with manual soldering. All three lots of microchip capacitors from Mfr.B passed TSD_350 without failures or any significant variations in AC or DC characteristics. However, all four lots from Mfr.A had failures after TSD_350, which indicate the necessity to take extra measures if these parts are to be soldered manually.

Results of TSD testing of MLCCs showed no failures in 120 samples from six lots of large, 2220 size, ceramic capacitors tested by 100 terminal solder dip cycles at a solder pot temperature of 300°C. Additional testing of large-size MLCCs (EIA size from 1825 to 2225) showed no failures in 40 parts after 10 cycles at 300°C and 325°C, and only one failure occurred after testing at 350°C. This is in agreement with the results of Chan et al. [17] who also did not observe failures in parts stressed by solder dip testing at 275°C and some decrease in breakdown voltage appeared after testing at 425°C only.

Contrary to tantalum capacitors where the difference in CTE between materials used can explain soldering-related failures, TSD testing of MLCCs results in failures that are due to temperature gradients across the parts and relevant transient stresses that depend on the rate of heat transfer during thermal shock tests.

During solder dip, a ceramic capacitor experiences a hot thermal shock with an instant temperature increase that results in large transient compressive stresses at the surface and relatively small tensile stresses in the bulk of the specimen. Although this test provides good heat transfer conditions and results in formation of significant thermo-mechanical stresses, the probability of fracture and crack formation is relatively low. This is mostly due to a high compressive strength of ceramic materials that is typically in the range from 1 GPa to 4 GPa and is approximately an order of magnitude greater than the tensile strength [18]. This explains a substantial increase of the critical temperature during TSD testing over the data reported in literature [17, 19]. In the referred studies the critical temperatures were measured during cold thermal shock testing that creates tensile stresses at the surface, and hence requires much smaller temperature gradients to cause fracture. Still, the critical temperature for hot TS (~350°C) is only 2 to 2.5 times greater than for cold TS (~150°C) and is not proportional to the difference in compressive and tensile stresses. This likely indicates that fracturing of MLCCs depends on the level of built-in mechanical stresses in the parts and on the concentration of the surface flaws that can vary from lot to lot depending on the materials and processes used.

Another factor that likely mitigates the effect of solder dip stresses and makes MLCCs generally robust enough to soldering induced TS is increased thermal conductivity of capacitors along the metal plates. Our estimations showed that, for the base metal electrode (BME) capacitors made with nickel, the effective thermal conductivity increases 2 to 6 times. For the precious metal electrode (PME) parts made with silver/palladium, this increase is larger, from 9 to 20 times, and substantially reduces temperature gradients and transient stresses in the parts.

Terminal solder dip testing provides more adequate test conditions compared to the conventional solder dip test. During the TSD test, one terminal of the capacitor is clamped in a fixture while the other is touching the molten solder. This eliminates local pressure to the body of ceramic capacitors or to plastic package of tantalum capacitors. This also stabilizes temperature at the clamped terminal and creates a temperature gradient at another terminal that is adequate to manual soldering conditions. Our data show that normal-quality lots of large-size MLCCs and tantalum capacitors can withstand TSD at 300°C, and the best lots can sustain TSD at 350°C without failures.

Considering that during manual assembly a soldering iron is typically set to 300°C, and to assure a safety margin, a terminal solder dip test at 325°C is recommended as a qualification procedure to assure robustness of the parts to manual soldering stresses. This test can be carried out using 20 samples that are subjected to 3 anode-side and 3 cathode-side cycles for tantalum capacitors or 3 cycles at the same terminal for ceramic capacitors. A lot is considered acceptable if all parameters of capacitors remain within the specified limits, all tantalum capacitors pass surge current testing at the rated voltage, variations of capacitance does not exceed 15%, increase of DF and ESR is less than 50%, and DCL does not increase more than three times.

CONCLUSION

1. A simple testing technique, terminal solder dip (TSD) test, that simulates thermal shocks stresses during manual soldering of ceramic and tantalum capacitors is described.

2. Extensive TSD testing showed that normal quality capacitors can sustain multiple thermal shocks (up to 100 cycles) at 300˚C, and some lots are capable to withstand testing at 350˚C.

3. No substantial differences in the susceptibility to cracking and failures between commercial and military-grade capacitors were observed.

4. Damage and failures of tantalum capacitors during soldering-induced thermal shock are due to the difference between CTE of tantalum slug and plastic package whereas failures of MLCCs are due to the temperature gradients across the part and related transient mechanical stresses.

5. A relatively high robustness of MLCCs toward terminal solder dip stresses compared to cold thermal shock testing is due to a high compressive strength of ceramic materials and increased thermal conductivity along the internal electrodes.

6. Degradation of ESR in tantalum capacitors was greater during cathode side solder dip compared to the anode side. Contrary to that, degradation of leakage currents and breakdown voltages occurred mostly after anode side solder dip testing. Large-size MLCCs (EIA size up to 2225) are failing mostly due to formation of corner cracks that might result in increase of leakage currents.

7. TSD testing is recommended as a qualification test for chip tantalum and ceramic capacitors that have to be manually soldered onto PWBs.

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