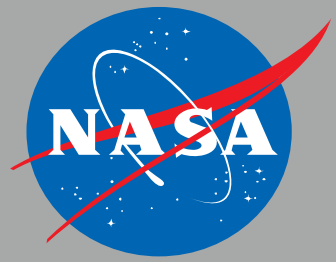


# Advanced Electronic Packaging

## The Assurance Challenges

**October 15, 2013**

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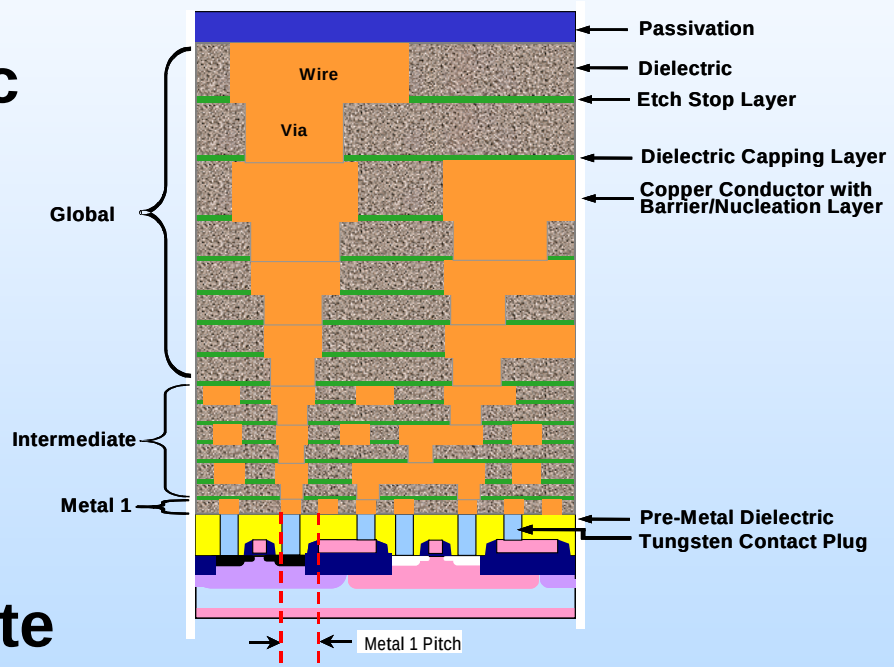
To be presented by Michael J. Sampson at the Trilateral NASA/Japan Aerospace Exploration Agency (JAXA)/European Space Agency (ESA) Safety and Mission Assurance Meeting, Washington, DC, October 15, 2013.

# Acronyms, Abbreviations Etc.

| | |
|---|---|
| Appx | Appendix |
| BME | Base Metal Electrodes |
| CCGA | Ceramic Column Grid Array |
| CLGA | Ceramic Land Grid Array |
| DLA | Defense Logistics Agency |
| EEE | Electrical, Electronic, and Electromechanical |
| FOD | Foreign Object |
| FPGA | Field Programmable Gate Array |
| GSFC | Goddard Space Flight Center |
| HDI | High Density Interconnect |
| HST | Hubble Space Telescope |
| IC | Integrated Circuit |
| I/O | Input Output |
| LGA | Land Grid Array |
| MIL-PRF-38534 | Performance Specification Hybrid Microcircuits General Specification For |
| MIL-PRF-38535 | Performance Specification Integrated Circuits (Microcircuits) Manufacturing General Specification For |
| NASA | National Aeronautics and Space Administration |
| Pb | Lead Metal |
| PBGA | Plastic Ball  Grid Array |
| RoHS | Restriction of Hazardous Substances |
| Sn/Pb | Tin/Lead |
| rev | revision |
| | |

# Outline

- What is Electronic Packaging?
- Why Package Electronic Parts?
- Hermetic and Non-hermetic
- Packaging Challenges
- Area Arrays
- Advantages of Hermetic
- Increasing Complexity
- Class Y Concept and Update
- Major Xilinx Package Change

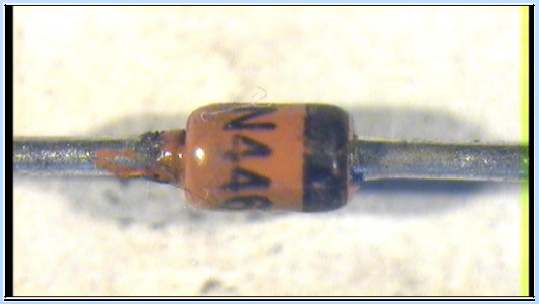


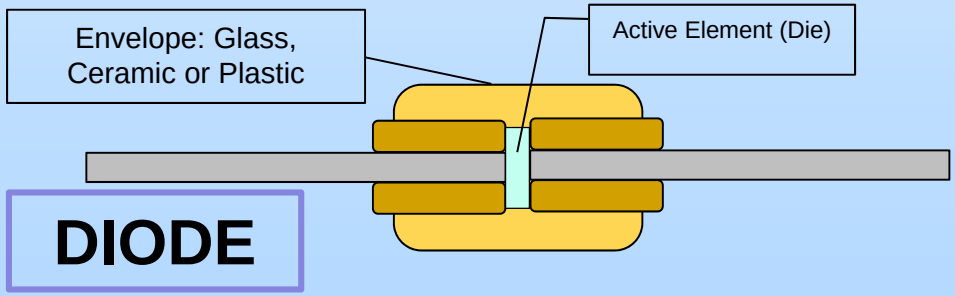
# What is Electronic Packaging?

- **Within NASA, electronic "packaging" can have two basic meanings:**
  - **First (Part) Level: The "envelope" of protection surrounding an active electronic element, and also the termination system to connect it to the outside world**
  - **Second and Higher Levels: The assembly of parts to boards, boards to slices, slices to boxes, boxes to systems, instruments and spacecraft**
- **This discussion focuses on the first**

# Why Package Electronic Parts?

- **To protect the active element against:**
  - **Handling**
  - **Shock and vibration**
  - **Contamination**
  - **Light penetration or emission**
- **To provide a suitable system to make connection between the element and the printed wiring board**
- **To prevent conductive parts of the element from coming in contact with other conductive surfaces, unless intended**





# Package Options – Hermetic?

- Hermetic packages have been the preferred option
- Few hermetic options for latest package technologies
  - Development of new hermetic options unattractive
    - Very high Non Recurring Expenses
    - Very high technical difficulty
    - Very low volume
    - Demanding customers
- Market is driven by consumer products
  - Low cost
  - High volume
  - Rapid turnover
  - "Green"
  - Minimized size

= Non hermetic, mostly plastic

# Continuous Packaging Challenges

- I/O s, increasing number, decreasing pitch
- Heat Dissipation, (especially in space)
- Manufacturability
- Materials
- Mechanical
- Installation
- Testability
- Inspectability
- RoHS (Pb-free)
- (Space Environment)

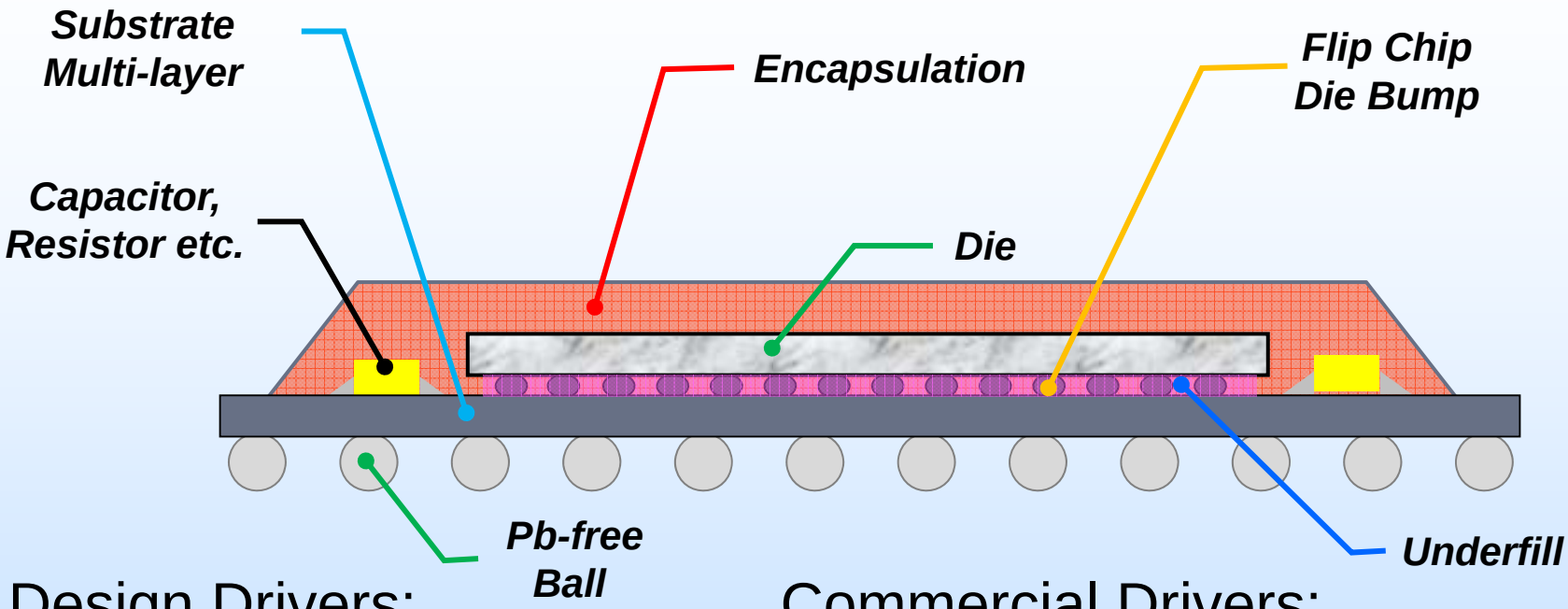
*Lunar Reconnaissance Orbiter (LRO), Built at GSFC, Launched with LCROSS, June 18,2009*

# Space Challenges for Complex Non-hermetic Packages

- **Hard Vacuum**
- **Foreign Object Debris (FOD)**
- **Shock and vibration**
- **Thermal cycling**
- **Thermal management**
- **Thousands of interconnects**
- **Low volume assembly**
- **Long life**
- **Novel hardware – “one offs”**
- **Rigorous test and inspection**

***ONE STRIKE AND YOU’RE OUT!***

# Commercial, Non-hermetic Package (PBGA*)




## Design Drivers:

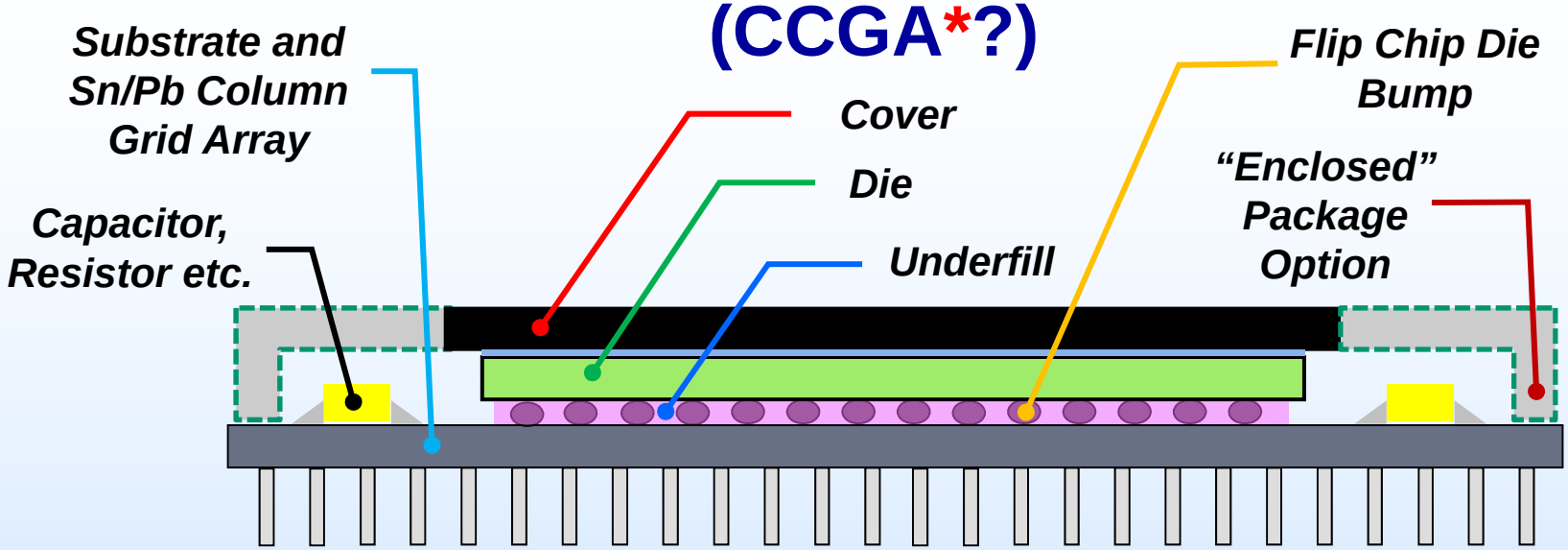
- High I/O count
- Large die
- Environmental protection
- Performance/Speed
- Ancillary parts

## Commercial Drivers:

- Low cost
- High volume
- Limited life
- Automated installation
- Compact

** PBGA: Plastic Ball Grid Array*

# Non-hermetic Package, With"Space" Features (CCGA*?)




| Space Challenge | Some Defenses |
|---|---|
| Vacuum | Low out/off-gassing materials. Ceramics vs polymers. |
| Shock and vibration | Compliant / robust interconnects - wire bonds, solder balls, columns, conductive polymer |
| Thermal cycling | Compliant/robust interconnects, matched thermal expansion coefficients |
| Thermal management | Heat spreader in the lid and/or substrate, thermally conductive materials |
| Thousands of interconnects | Process control, planarity, solderability, substrate design |
| Low volume assembly | Remains a challenge |
| Long life | Good design, materials, parts and process control |
| Novel hardware | Test, test, test |
| Rigorous test and inspection | Testability and inspectability will always be challenges |

* Ceramic Column Grid Array

# Hermeticity

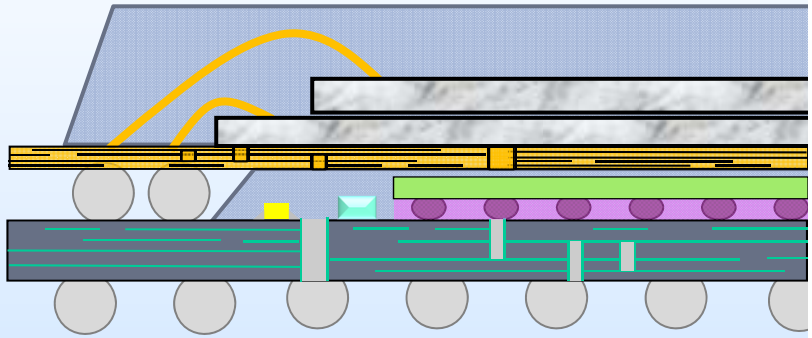
- **NASA prefers hermetic packages for critical applications**
- **Hermeticity is measureable, assuring package integrity – although testing is difficult**
- **Just 3 tests provide assurance for hermetic package integrity:**
  - **Hermeticity – nothing bad can get in**
  - **Residual or Internal gas analysis – nothing bad is inside**
  - **Particle Impact Noise Detection – no FOD inside**
- **NON-HERMETIC PACKAGE INTEGRITY IS HARD TO ASSESS - NO 3 BASIC TESTS**
- **Non-hermetic packages expose materials interfaces that are locked away in hermetic ones**

# But What is Hermetic?

- **Per MIL-PRF-38534 Appx E and 38535 Appx A, hermetic packages must consist of metals, ceramic and glass in combinations ONLY, *no polymerics***
- **Meets aggressive leak rate test limits**
  - **Verifies low rate of gas escape/ atmospheric interchange**
  - **Even so, small volume packages meeting "tight limits" theoretically exchange their atmosphere very quickly:**
    - **0.001 cc, exchanges 93% in 1 month at $5X10^{-8}$ atmosphere/cc/sec!**
    - **1.0cc, 96% in 10 years at $1 X 10^{-8}$**
  - **Even large packages with quite small leaks can surprise**
    - **10 cc, 96% in 1 year at $1 X 10^{-6}$ !**
- **For applications in space vacuum why care?**
  - **Risk for contamination on the ground**
  - **Risk for outgassing in vacuum**

# Non-hermetic Package Variations

- **Current and future package options mix and match elements in almost infinite combinations**
- **Elements include:**
  - **Wire bonds**
  - **Ball interconnects (flip chip)**
  - **Solder joints**
  - **Conductive epoxies**
  - **Vias**
  - **Multi-layer substrates**
  - **Multiple chips, active and passive (hybrid?)**
  - **Stacking of components**
  - **Embedded actives and passives**
  - **Polymers**
  - **Ceramics**
  - **Enclosures/encapsulants**
  - **Thermal control features**
  - **ETCETERA**



# More Complexity is Coming

- **Stacking of chips to provide a third dimension of density and complexity**
  - **Stacking of Field Programmable Gate Arrays (FPGAs) – soon?**
  - **Stacking of memory die is "old hat"**
  - **Through-silicon vias instead of bond wires**
    - **Maintain speed and allow lots of I/Os**
    - **High volumetric efficiency**
  - **Significant manufacturability challenges**
    - **Material and dimensional interfaces**
    - **Exposure to installation stresses and process solvents**
    - **Testability**
  - **Significant usability challenges**
    - **Design complexity**
    - **Handling, testing, rework/replace, risk management**
    - **Cost versus benefit trades**

Amkor Technology®

http://www.amkor.com/go/packaging

### Fine Pitch Copper Pillar Flip Chip

Copper pillar bump is a next generation flip chip interconnect which offers advantages in many designs while meeting current and future ROHS requirements. It is an excellent interconnect choice for applications where some combination of fine pitch, ROHS / Green compliance, low cost and electromigration performance are required.

### 3D - Through Silicon Via (TSV) Wafer Finishing & Flip Chip Stacking Solutions

Through Silicon Via (TSV) interconnects are emerging to serve a wide range of 3D packaging applications and 3D IC architectures that demand higher levels of performance and silicon integration.

### Package on Package (PoP | PSfvBGA | PSfcCSP | TMV® PoP)

Amkor has expanded its comprehensive PoP (Package on Package) family and aligned the roadmap across the supply chain to ensure that PoP will continue to scale with the industry's miniaturization, higher density and performance enhancement requirements.

### Flip Chip BGA (fcBGA)

Amkor Flip Chip BGA (fcBGA) packages are assembled around state-of-the-art, single unit laminate or ceramic substrates. Utilizing multiple high density routing layers, laser drilled blind, buried, and stacked vias, and ultra fine line/space metallization, fcBGA substrates have the highest routing density available.

### Flip Chip Packaging Technology Solutions

Since being the first OSAT to provide FCiP solutions in 1999, Amkor has continued to introduce innovative packaging solutions utilizing Flip Chip interconnect, and offers the broadest range of FCiP solutions on the market. SuperFC®, FCBGA, FCmBGA, FlipStack CSP, fcLBGA, fcLGA and fcCSP are qualified and are in production.

### FCmBGA (Flip Chip Molded Ball Grid Array)

Amkor's flip chip molded BGA (FCMBGA) package enables thinner packaging and improves thermal performance while reducing system cost.

### fcCSP (Flip Chip CSP)

Amkor Technology is now offering the Flip Chip CSP (fcCSP) package -- a flip chip solution in a CSP package format. This package construction utilizes Pb-Free (or Eut. SnPb) flip chip interconnect technology, in either area array or peripheral bump layout, replacing standard wire-bond interconnect.

### FlipStack® CSP

The FlipStack® CSP family utilizes Amkor's industry leading ChipArray® Ball Grid Array (CABGA) manufacturing capabilities, in combination with Amkor's fcCSP technology. This broad high volume infrastructure enables the rapid deployment of advances in die stacking technology across multiple products and factories to achieve lowest total cost.

# MIL-PRF-38535, Class Y

- **Space grade but non-hermetic – Class Y**
- **New class for M38535, monolithic microcircuits**
- **Class V will be defined as space-grade, hermetic only**
- **Addition to Appendix B, "Space Application"**
- **Package-specific "integrity" test requirements proposed by manufacturer, approved by DLA* and government space**
- **The Package Integrity Test Plan must address:**
  - **Potential materials degradation**
  - **Interconnect reliability**
  - **Thermal management**
  - **Resistance to processing stresses**
  - **Thermo-mechanical stresses**
- **Allows great flexibility in package style**
- **Final draft of M38535K in final review**

* MIL spec qualifying activity Defense Logistics Agency, Land and Maritime

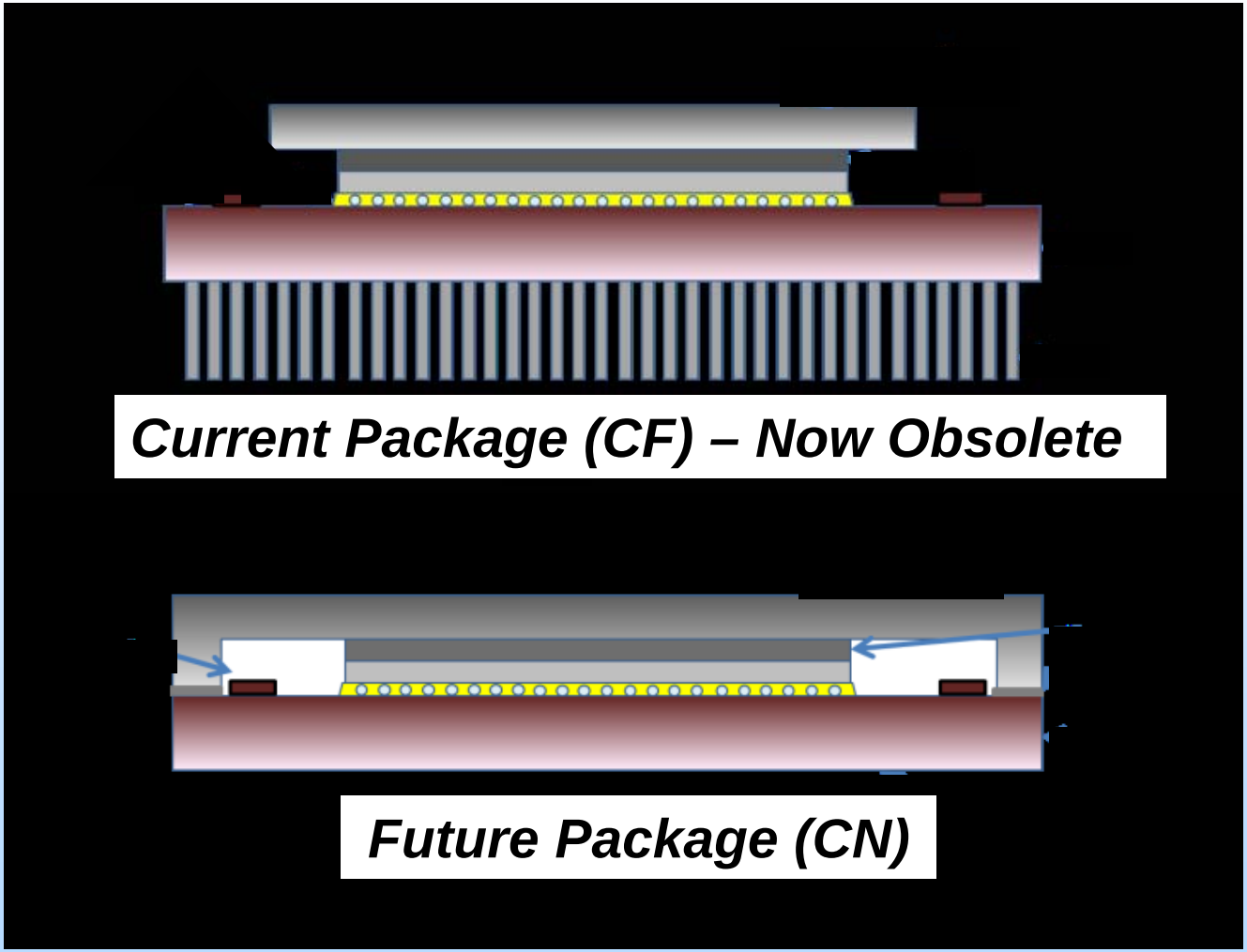
# Current Sticky Points

- Use of Base Metal Electrode (BME) capacitors
  - Used for decoupling in Xilinx, Virtex 4 and 5 FPGAs
  - Increasingly used with high speed integrated circuits
  - Not yet accepted by US space users
- Electrical testing post column attach (for CCGAs)
  - Very difficult without causing destructive damage
  - Room temperature electricals perhaps
  - But tri temperature electricals and burn-in? NO
- Solder bump and column attachment testing
  - Shear, pull etc.
- And others
- Trying to find compromise resolutions but could further delay revision K
- Until rev K is released, MIL certification audits cannot occur and the “hidden” problems cannot be seen

# Potential Class Y Suppliers

- **The front runners**
  - **Aeroflex :**
  - **Xilinx:**
  - **BAE:**
  - **Honeywell:**
  - **E2v (Grenoble, France):**
- **Others**
  - **Texas Instruments**
  - **Microsemi Actel**
  - **Intersil**
  - **Cypress**
  - **3D**

# Xilinx Package Change



# So What Will Change?

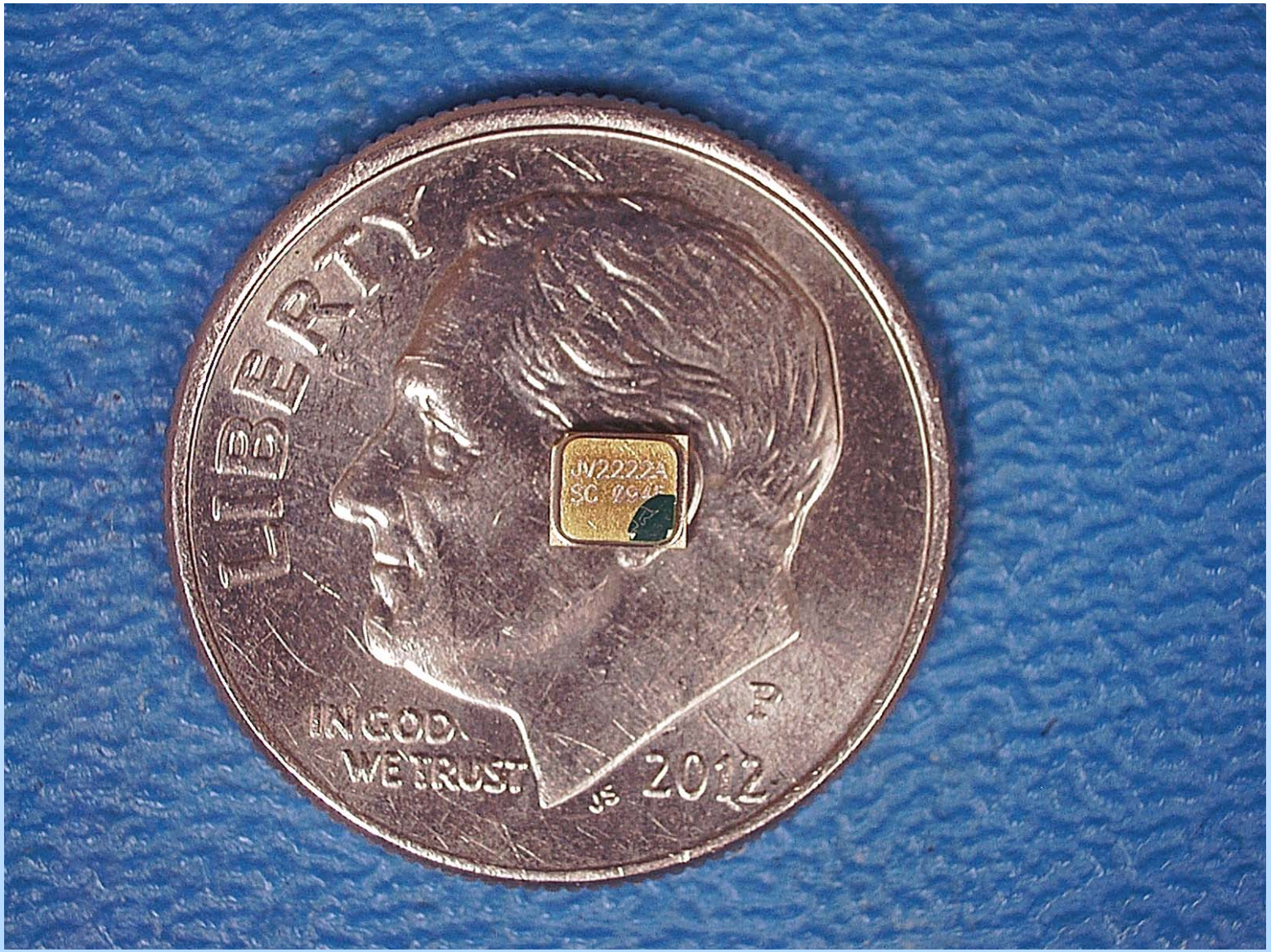
- **Everything except the die, substrate and BME capacitors**

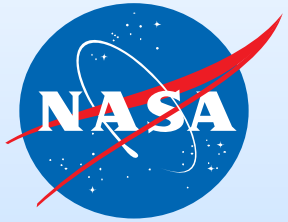
| Feature | CF Package | CN Package |
|---|---|---|
| Packaging House | IBM | Kyocera (US) |
| Bumping House | SPIL then Amkor | SPIL |
| Bumps | Hi Temp | **Eutectic Sn/Pb** |
| Lid | SiC | AlN |
| Lid Shape | Flat | Corner posts - thinner |
| Lid adhesive | IBM | Kyocera |
| Underfill | IBM | Kyocera |
| Package Style | CCGA | **CLGA**! |
| Country of Origin | Canada | United States of America |

# A 1752 I/O Column Grid Array

***From: Reliability of CGA/LGA/HDI Package Board/Assembly***
***by***
***Reza Ghaffarian Ph.D, JPL***
***Available at http://nepp.nasa.gov***

# And There is Always the Size Challenge!



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