

## Advanced Electronics Technologies: Challenges for Radiation Effects Testing, Modeling, and Mitigation

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Presented by Kenneth LaBel at Space Environment Effects Working Group, El Segundo, CA – Nov. 1-3, 2005



## Outline


- **Emerging Electronics Technologies**
  - Changes in the commercial semiconductor world
- **Radiation Effects Sources**
  - A sample test constraint
- **Challenges to Radiation Testing and Modeling**
  - IC Attributes – Radiation Effects Implications
  - Fault Isolation
  - Scaled Geometry
  - Speed
  - Modeling Shortfalls
  - Knowledge Status
- **Summary**
- **Recommendations**

### **Notes:**


- 1. The emphasis of this presentation is digital technologies and SEE.*
- 2. A discussion of mitigation implications is included in the notes.*

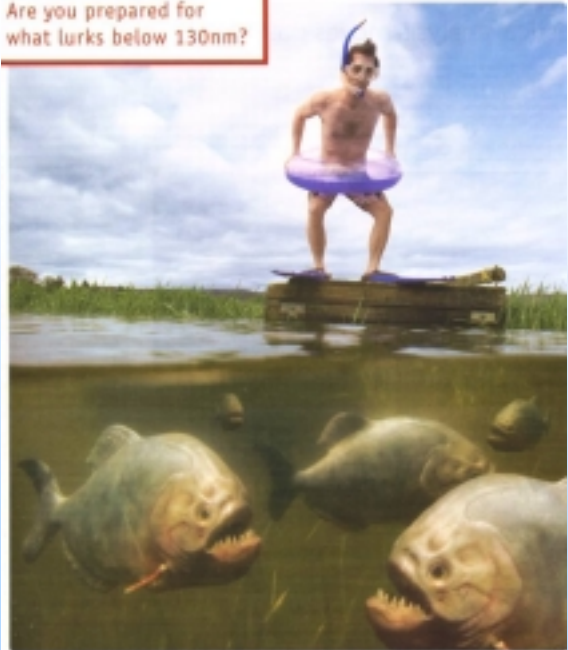
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Are you prepared for  
what lurks below 130nm?






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## Changes in the Electronics World



- Over the past decade plus, much has changed in the semiconductor world. Among the rapid changes are:
  - **Scaling of technology**
    - Increased gate/cell density per unit area (as well as power and thermal densities)
    - Changes in power supply and logic voltages (<1V)
      - Reduced electrical margins within a single IC
    - Increased device complexity, # of gates, and hidden features
    - Speeds to >> GHz (CMOS, SiGe, InP...)
  - **Changes in materials**
    - Use of antifuse structures, phase-change materials, alternative K dielectrics, Cu interconnects (previous – Al), insulating substrates, ultra-thin oxides, etc...
  - **Increased input/output (I/O) in packaging**
    - Use of flip-chip, area array packages, etc
  - **Increased importance of application specific usage to reliability/radiation performance**

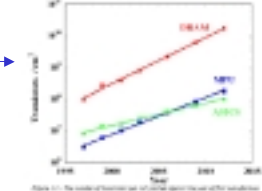
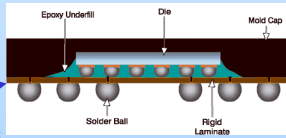


Figure 1-1: The number of transistors per unit area grows faster than Moore's Law.

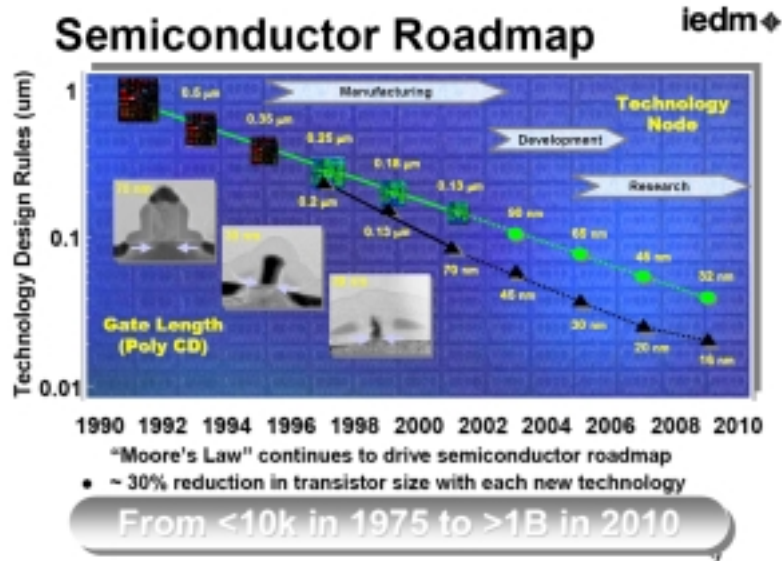


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## Mainstream digital – CMOS scaling

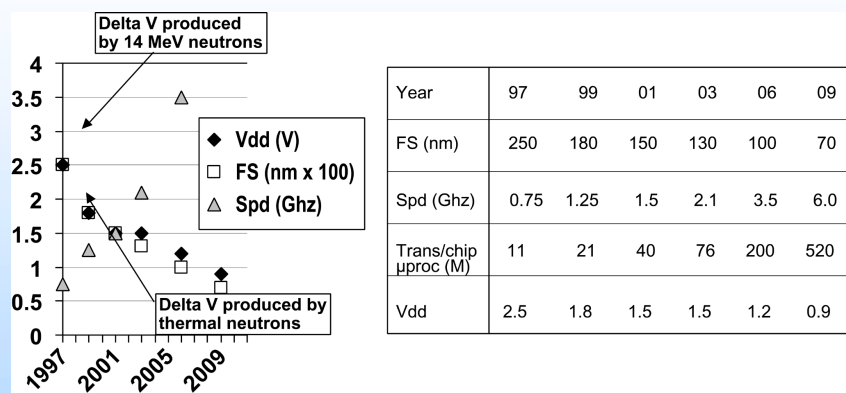


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## Neutron-Induced Transients vs. Feature Size (FS), Vdd, and Speed



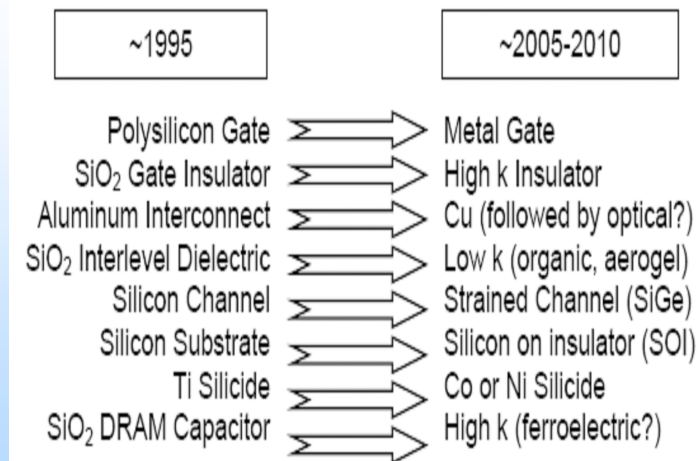
Note the magnitude of the voltage transient equals or exceeds the operating voltage for circuits fabricated using 180nm technology [Mass01-van]

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## Changing Materials for Mainstream CMOS



*Virtually all of the Materials used to fabricate IC's in 1995 will be different in 2010*  
*A&T Dellin, 2005, 21st Century Semiconductor Technology*

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## Changes in IC Attributes vs. Radiation Effects



Attributes	SEU	MBU	SET	SEFI	SEGR	TID
Intelligence	++	++	+	++	-	-
Flexibility	++	++	-	+++	-	+
Complexity	+++	-	+	-	+	++
Integration Density	+	+++	-	-	-	-
Hidden Circuit Features	+	-	-	+++	-	-
Construction	++	++	++	++	++	++
Power	+	+	++	-	-	-
Speed	-	-	+++	-	-	-

+ = worse  
++ = much worse  
+++ = very significant impact  
- = no effect

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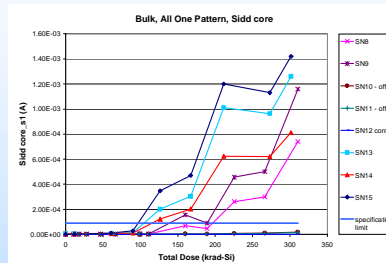
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## Total Ionizing Dose – Summary trends



- Deep sub-micron ( $<0.25\mu\text{m}$ ) CMOS basic structures have shown increasing tolerance to TID (thinner oxides)
  - $>100\text{ krad(Si)}$
- However,
  - Complex structures and those that require higher voltage fields such as charge pumps in flash memories or FPGAs may be MUCH more TID sensitive
  - Bipolar devices do not scale as easily and are susceptible to enhanced low dose rate sensitivity (ELDRS)
    - Failure at  $\ll 100\text{ krad(Si)}$  at low space dose rates
    - Scaled CMOS devices observing ELDRS-like effect (Wiczak, 2005)



Sample Bulk CMOS 0.18 $\mu\text{m}$  Technology  
Demonstrating  $\sim 100\text{ krad(Si)}$  Tolerance  
Poivey 2005

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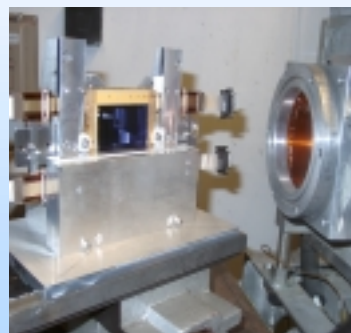


## Typical Ground Sources for Space Radiation Effects Testing



- Issue: TID
  - Co-60 (gamma), X-rays, Proton
- Issue: Displacement Damage
  - Proton, neutron, electron (solar cells)
- SEE (GCR)
  - Heavy ions, Cf
- SEE (Protons)
  - Protons ( $E > 10\text{ MeV}$ )
- SEE (atmospheric)
  - Neutrons, protons

TID is typically a local source with nearby ATE. All others require travel and shipping  
– A constraint for how testing is done.



Wide Field Camera 3 E2V  
2k x 4k n-CCD in front of Proton Beam at UCDavis

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<div style="display: flex; justify-content: space-between; align-items: center;"> <h2 style="margin: 0;">Potential SEU Sites in a SRAM-based FPGA</h2> </div>		
Chip Area	SEE Issue	Possible SEU Mitigation
Config. Memory	Single and multiple bit errors corrupting circuit operation, causing bus conflicts (current creep), etc...	<ul style="list-style-type: none"> <li>Scrubbing</li> <li>Partial reconfiguration</li> </ul>
Config. Controller	Improper device configuration can occur if hit during configuration/reconfiguration	<ul style="list-style-type: none"> <li>Partitioned design</li> <li>Multiple chip voting (Redundancy by using multiple devices)</li> </ul>
CLB	Logic hits and propagated upsets caused by transients	<ul style="list-style-type: none"> <li>Triple modular redundancy (TMR)</li> <li>Acceptable error rates</li> </ul>
BRAM	Memory upsets in user area	<ul style="list-style-type: none"> <li>TMR</li> <li>Error Detection and Correction (EDAC) scrubbing</li> </ul>
Half-latches	Sensitive structure used in configuration/routing	<ul style="list-style-type: none"> <li>Removal of half-latches from design</li> </ul>
POR	SEUs on POR can cause inadvertent reboot of device	<ul style="list-style-type: none"> <li>Multiple chip voting (Redundancy by using multiple devices)</li> </ul>
IOB	SEUs can cause false outputs to other devices or inputs to logic	<ul style="list-style-type: none"> <li>Leverage Immune Config. Memory cell</li> <li>Evaluate input SET propagation</li> </ul>
DCM	Can cause clock errors that spread across clock cycles	<ul style="list-style-type: none"> <li>TMR</li> <li>Temporal TMR</li> </ul>
DSP	Hard IP that is unhardened that can cause single event functional interrupts (SEFIs) or data errors	<ul style="list-style-type: none"> <li>TMR</li> <li>Temporal TMR</li> </ul>
MGT	Gigabit transceivers. Hits in logic can cause bursts or SEFIs. O/w bit errors in data stream	<ul style="list-style-type: none"> <li>TMR</li> <li>Protocol re-writes</li> </ul>
PPC	Hard IP that is unhardened. SEFIs are prime concern	<ul style="list-style-type: none"> <li>TMR or software task redundancy</li> </ul>
SEL	Higher current condition that is potentially damaging	<ul style="list-style-type: none"> <li>No mitigation other than substrate addition (epi).</li> <li>Circumvention techniques possible</li> </ul>

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## Fault Isolation –(3)

- **Macrobeam structure: implies probabilistic chance of hitting a single node that may be sensitive**
  - If test is run for SEE, typical heavy ion test run is to  $1 \times 10^7$  particles/cm<sup>2</sup>.
    - Ex., SDRAM – 512 Mb (5x10<sup>8</sup> bits plus control areas)
      - If all memory cells are the same, no issue. BUT if there are weak cells how do you ensure identifying them?
      - Control logic may be a very small area of the chip. If you fly 1000 devices, area is no longer “small”
  - Difficult to evaluate clock edge sensitivity of a node
- **Die access (required for most single event testing)**
  - Typical heavy ion single event macrobeam simulators have limited energy range
    - Implies limited penetration through packaged device
    - Access to die typically required
      - Overlayers, metalization, etc must be taken into account

**Device Under Test (DUT)  
Package Material**

Facility	Ion (Energy)	LET (Si)	Range in Si (μm)	Peak LET
NSCL	Xe (3.2 GeV)	40	272	69
TAMU	Ar (2 GeV)	5.9	390	18

Table assumes ion traverses 1.5 mm plastic; LET given in MeV-cm<sup>2</sup>/mg

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- Typical Chip Cross Section**
- The diagram illustrates a cross-section of a chip with three main vertical regions: Global, Intermediate, and Local. The Global region at the top contains Nitride, Via, and Dielectric layers. The Intermediate region in the middle contains Die chiplets, Dielectric diffusion barrier, and Copper conductor on metal barrier layer. The Local region at the bottom contains Pre-metal dielectric and Tungsten contact plug. The chip is mounted on a substrate.

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- DRAM Cell Area History / 2001 ITRS Model**
- This graph illustrates the historical trend and projected future trend of DRAM cell area. The Y-axis represents the DRAM Cell Area in  $\mu\text{m}^2$  on a logarithmic scale from 0.001 to 100. The X-axis represents the Year from 1980 to 2020.
- Historical Trend (1980-2000):**
- Historical trend line:  $0.35\text{e}^{-1/3 \text{ Years}}$
  - Historical trend slope:  $-29\%/yr$
- Projected Future Trend (2001 ITRS Model):**
- Projected trend line:  $0.35\text{e}^{-1/3 \text{ Years}}$
  - Projected trend slope:  $-29\%/yr$
- Key Milestones and Annotations:**
- 1980:** 1K1 (1.5  $\mu\text{m}^2$ )
  - 1985:** 1M1 (1.5  $\mu\text{m}^2$ )
  - 1990:** 16M1 (1.5  $\mu\text{m}^2$ )
  - 1995:** 1G1 (1.5  $\mu\text{m}^2$ )
  - 2000:** 1T1 (1.5  $\mu\text{m}^2$ )
  - 2005:** 1T2 (1.5  $\mu\text{m}^2$ )
  - 2010:** 1T3 (1.5  $\mu\text{m}^2$ )
  - 2015:** 1T4 (1.5  $\mu\text{m}^2$ )
  - 2020:** 1T5 (1.5  $\mu\text{m}^2$ )
- Additional Notes:**
- Actual Scaling Acceleration, or Equivalent Scaling, necessary to maintain historical trend.
  - DRAM Cell Size Historical Trend:  $0.35\text{e}^{-1/3 \text{ Years}}$
  - Full Design/Manufacture contributed additional  $-2\%/yr$
- Source:** International Technology Roadmap for Semiconductors

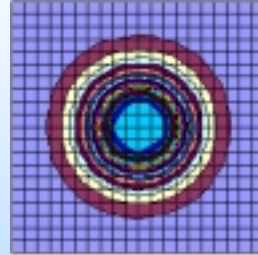
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## Geometry Implications (2)

- **Multiple node hits (cont'd)**
  - Ex., memory array
    - A single particle strike can spread charge to multiple cells. If the cells are logically as well as physically located
      - Standard memory scrub techniques such as Hamming Code can be defeated
    - This is not new, simply exacerbated by scaling. Traditional SEU modeling considers particle strikes directly on a transistor
  - Charge spreading for strikes near but not on the transistor can generate errors
    - Measured error cross-sections may exceed physical cross-sections
  - Albeit actual individual targets are smaller for a single particle
    - More targets and the spread of non-target hits implied potentially increased error rates per device
  - The role of particle directionality and of secondaries requires future use of physics-based particle interaction codes coupled with circuit tools.
    - GEANT4, MCNPX, etc. are the type of codes required
      - Efforts begun to turn these into tools and not just science codes



Charge spreading from a single particle in an active pixel sensor (APS) array impacts multiple pixels

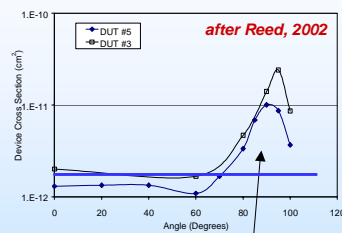
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## Geometry Implications (3)

- **High-aspect ratio electronics**
  - For “standard” devices, the direction of the secondary particles produced from a proton (or neutron) are considered omnidirectional
  - However, for electronics where there is a high-aspect ratio (very thin with long structure), this is not the case
    - The forward spallation of particles when the proton enters the device along the long structure increases the potential error measurement cross-section
    - Test methods and error rate predictions need to consider this



Effects of protons in SOI with varied angular direction of the particle;  
Blue line represents expected response with “standard” CMOS devices.

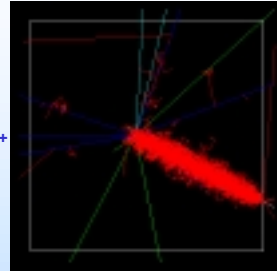
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## Geometry Implications (4)

- Ultra-thin oxides provide two concerns
  - Single particles rupturing the gate
    - This is a function of the thinness and the current across a gate oxide
  - The impact of oxide defects
    - Role for TID
- Secondaries from packaging material
  - Even on the ground, particle interaction with packaging materials can cause upsets to a sensitive device
    - Ex., Recent FPGA warning of expectation of up to 1 upset/spontaneous reconfiguration a day!
- Small probability events have increased likelihood of occurring
  - If 1 in a  $10^9$  particles causes a “larger” LET event or 1 in  $10^6$  transistors can cause a more complex error
    - With billion plus transistor devices and potential use of >1000 of the same device (re: solid state recorders), small probabilities become finite



Sample 100 MeV proton reaction in a 5  $\mu$ m Si block.  
Reactions have a range of types of secondaries and LETs.  
(after Weller, 2004)

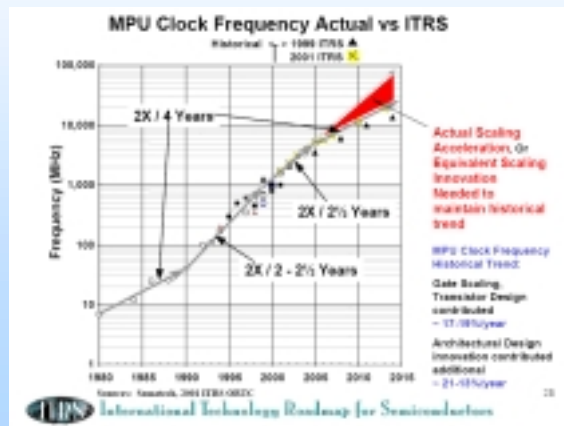
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## Radiation Test Challenge – Speed Implications

- Issue: the increasing device speeds (>> GHz) impact testing, test capability requirements, and complicate effects modeling.



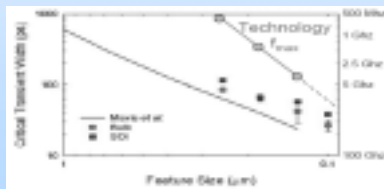
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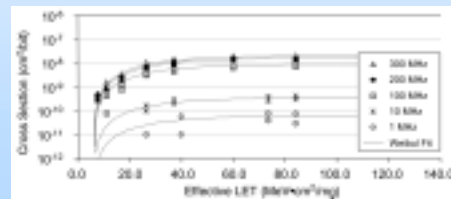


## Speed (2)

- Technology Complications
  - Propagation of single event transients (SETs)
    - As opposed to a direct upset by a particle strike on a latch-structure, the particle hit causes a transient (think hit on a combinatorial logic or such) that can propagate to change the state of a memory structure down the chain.
      - The transient pulse width can be on the order of picoseconds to nanoseconds (or longer depending on circuit response)
        - » Older, slower devices didn't recognize the transient (i.e., minimum pulse width required for circuit response was greater than that generated by a single particle)
        - » Newer devices can now respond to these hits increasing circuit error rates
      - Transient size in analog devices has been seen to be a partial function of the range of the particle entering the device
        - » Impacts facility usage choices

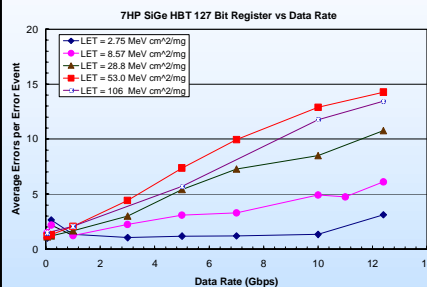


Critical width for unattenuated propagation of SETs decreases with feature size, Dodd-04



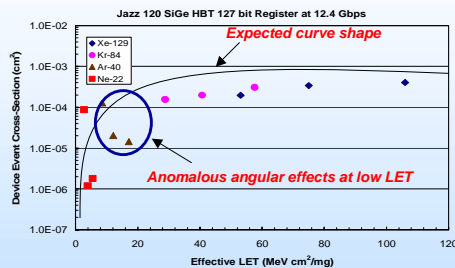


## Speed (4)



Average number of errors noted by a single particle event increases with speed and LET

Marshall-04



Effects of heavy ions on SiGe devices at 12 GHz speeds notes anomalous charge collection of this high-speed technology; Drawn line represents expected response with "standard" models.

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## Speed (5)

Testing at a remote facility requires highly portable test equipment capable of high-speed measurements

- Tester needs to be near the device or utilize high-speed drivers
  - Cable runs between the device under test (DUT) and the tester can be up to 75 feet
- Simple devices like a shift register chain can be tested using bit error rate testers (BERTs)
  - BERTs can run to ~\$1M and tend to be very sensitive to problems from shipping
    - At proton test facilities secondaries are generated (neutrons) that can cause failures in the expensive test equipment if they are located near the DUT
- Self-test techniques for testing devices being developed for shift-registers
  - Modern reconfigurable FPGA-based test boards being developed to test more generic devices



Beware of stray neutrons impinging on your test equipment.

Here, Borax is shown on top of a power supply to absorb neutrons.

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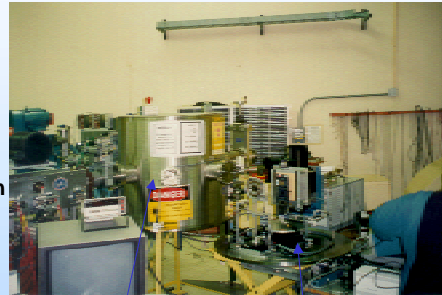
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## Speed (6)

- Testing in a vacuum chamber implies mechanical, power/thermal, and hardware mounting constraints
  - High-speed devices often mean high power consumption
    - Issue is mounting of DUT in vacuum chamber and removal of thermal heat
      - Can also be a challenge NOT in a vacuum
      - DUT may need to be custom packaged to allow for thermal issues
  - Active system required for removal of heat

Brookhaven National Laboratories' Single Event Upset Test Facility (SEUTF)



Vacuum Chamber

User equipment area

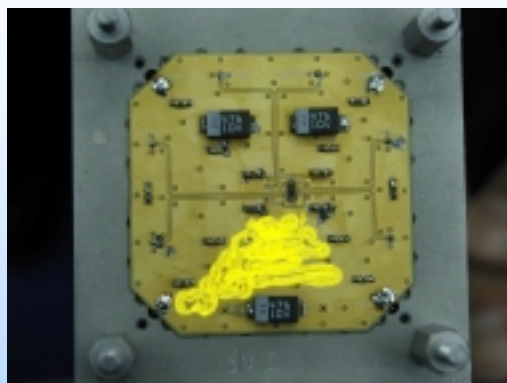
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## Specialty Packaging for Radiation Test

- Thermal, Speed, Power



Front

Back

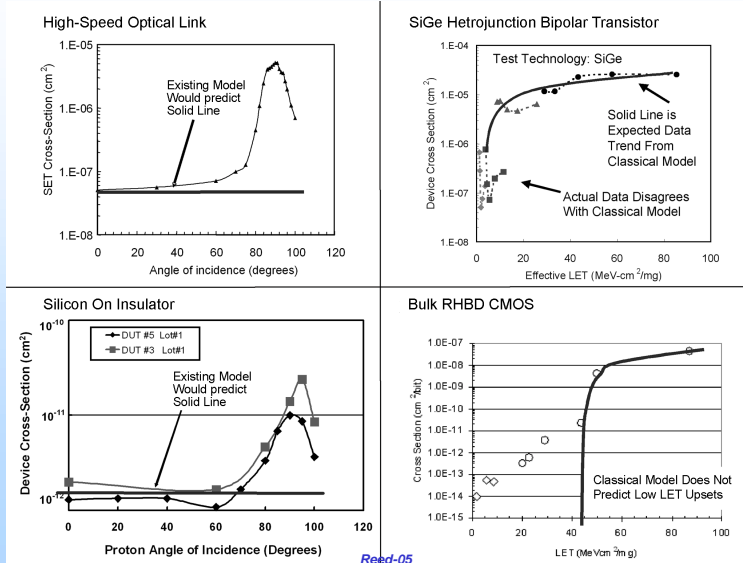


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## Sample Modeling Shortfalls



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## Radiation Status for Advanced Electronics



Radiation Response	Guideline Document	Test Method	Data Base	Modeling & Simulation
SEU/MBU	Yes	Yes	Yes	~ mature
SET	No	No	No	No
SEL	Yes	Yes	Yes	No
SEGR	No	No	No	No
SEFI	No	No	No	No
TID	Yes	Yes	Yes	Yes
Displacement Damage	Yes	Yes	No	No

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