



Current Problems in Radiation Effects in Microelectronics

Timothy R. Oldham
Perot Systems Government Services, Inc.
Greenbelt, MD 20771
15 Dec 08

DTRA



DTRA

Acknowledgements

- Sponsors
 - NASA NEPP Program (Ken LaBel)
 - DTRA (Lew Cohn)
- Collaborators—too many to name



IEEE Nuclear and Space Radiation Effects Conference (NSREC)

- Held each year in July since 1964
- Accepted papers published in Dec issue of IEEE Transactions on Nuclear Science (TNS)
- IEEE Radiation Effects Data Workshop Record (REDW)
- Typically about 100 regular papers, 30 Workshop submissions, tutorial short course
- 2009 NSREC July 20-24 in Quebec, Canada

5



References

- T.P. Ma and P.V. Dressendorfer, *Ionizing Radiation Effects in MOS Devices and Circuits*, Wiley Interscience, New York, 1989.
- T.R. Oldham, *Ionizing Radiation Effects in MOS Oxides*, World Scientific Publishing, Singapore, 1999.
- IEEE Trans. Nucl. Sci, June 2003 special issue.
- IEEE NSREC Archive of Radiation Effects Short Course Notebooks, 1980-2006

6



Outline

- Introduction
- Total Ionizing Dose (TID) Effects
- Single Event Effects (SEE)
- Conclusions

5



TID Effects

- Charge Generation/recombination
- Charge Transport
- Oxide Charge Trapping/annealing
- Interface Traps
- Testing Issues (Rebound, Dose Rate, Dose Enhancement)
- Isolation Structures
- ELDRS

6

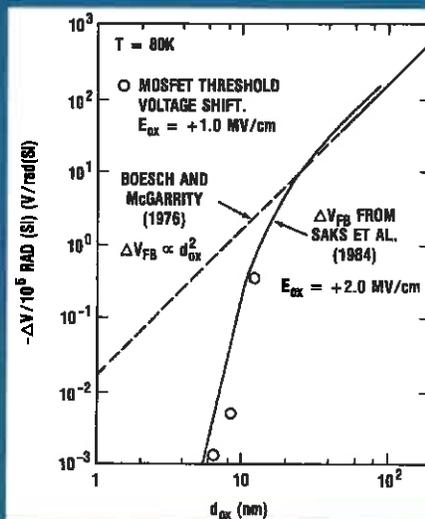


TID Effects

- Trap-assisted tunneling
- STI
- Micro-dose
- ELDRS



Oxide Thinning



J.M. Benedetto et al., IEEE TNS, Dec 1985.



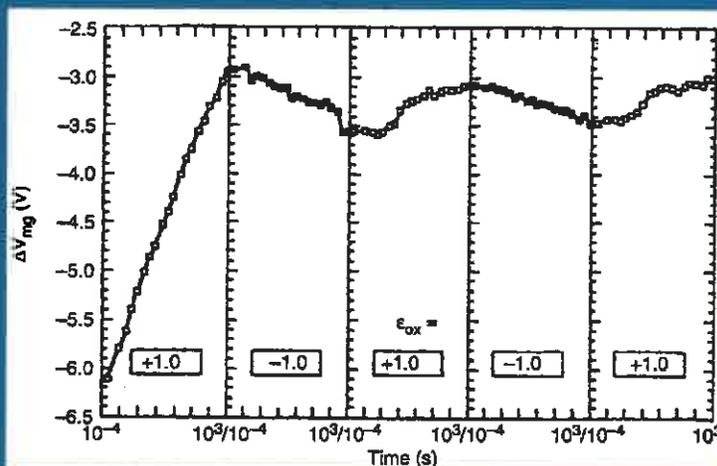
Oxide Thinning

- Very thin modern oxides are resistant to TID damage
- Remaining TID issues with isolation structures
- RILC/SILC (Radiation or Stress Induced Leakage Current)—new concern because oxides are thin
- RILC/SILC appear to be due to same underlying mechanism (A. Paccagnella et al., IEEE TNS, Dec 1997)—tunneling, in particular, trap assisted tunneling

9



Bias Switching Experiment



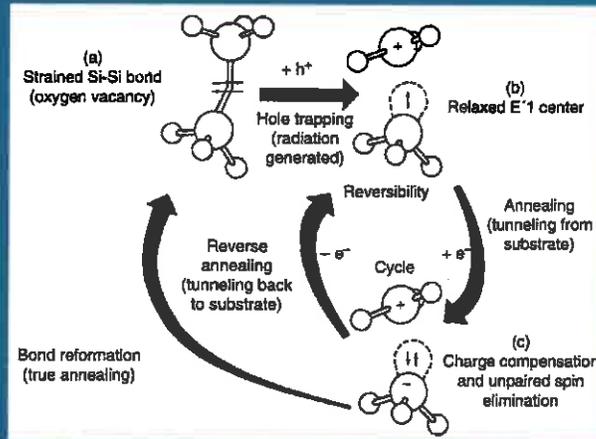
A.J. Lellis et al., IEEE TNS, Dec 1988

10



DTRA

Switching Oxide Trap



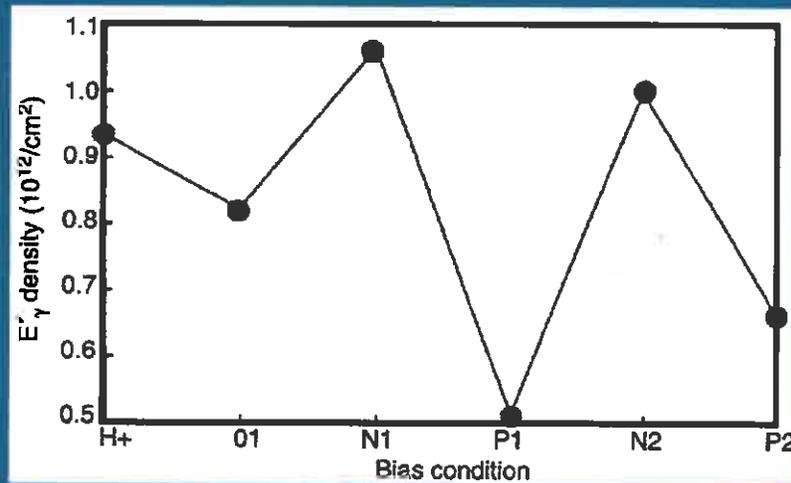
A.J. Leelis et al., IEEE TNS Dec 1989.

11



DTRA

ESR Result



J.F. Conley et al., IEEE TNS, Dec 1995.

12



STI Effects

- Trench oxide charging concentrated near the top of the oxide (M. Turowski et al., IEEE Trans. Nucl. Sci, 51, 3166 (2004)).
- Parasitic leakage paths near the surface of the chip

13



Stuck Bits

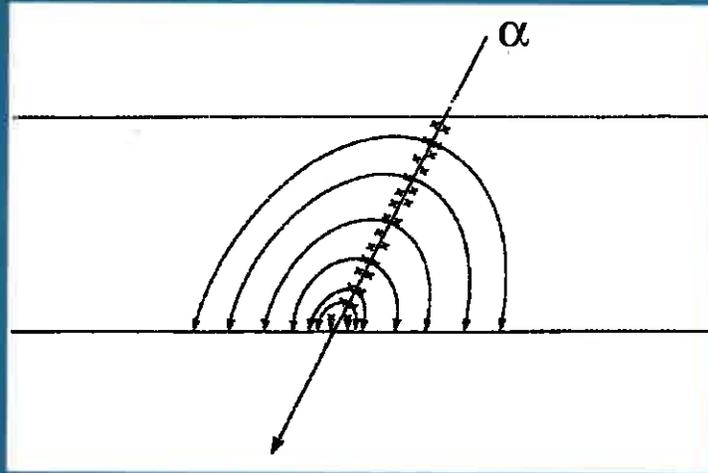
- Reported by Koga (IEEE TNS, Dec 1991), attributed to total dose from single ion by Dufour et al. (IEEE TNS, Dec 1992), analysis by Oldham et al. (IEEE TNS, Dec 1993) and Poivey et al. (IEEE TNS, Dec 1994)—micro-dose.
- Second mechanism, related to SEGR, reported by Swift et al. (IEEE TNS, Dec 1994)
- Loquet et al. modeling implicating isolation oxides (IEEE TNS, Dec 2001)
- First reported in 1M SRAMs with 4T cell

14



Charge Transport in SiO₂

DTRA



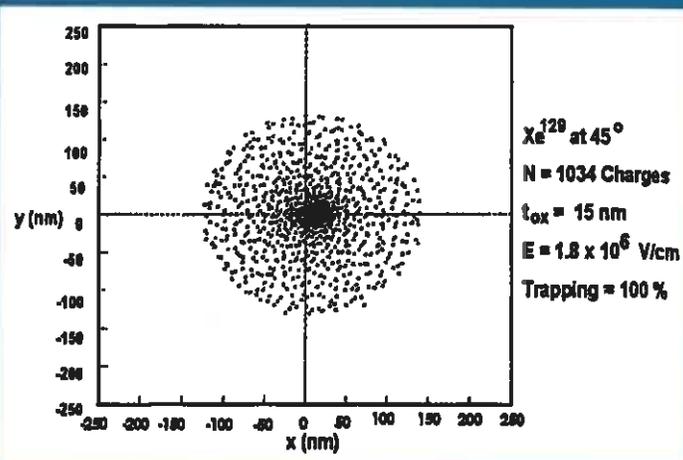
T.R. Oldham, IEEE TNS, 40,1820 (1993).

15



Charge Trapping in SiO₂

DTRA



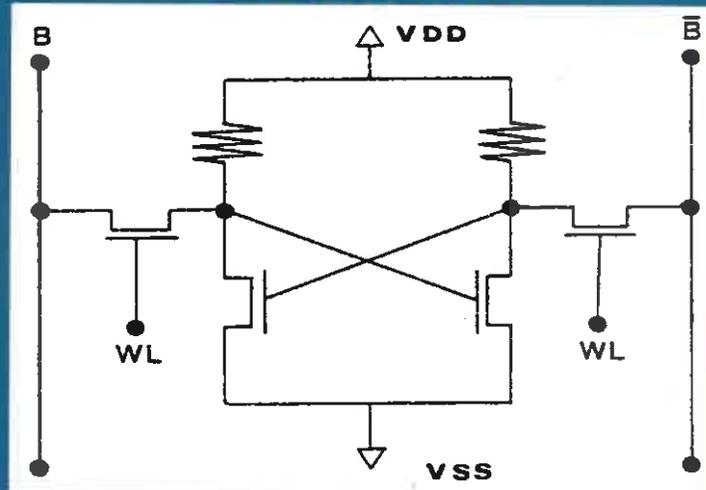
T.R. Oldham et al., IEEE TNS, 40, 1820 (1993).

16



4T SRAM Cell

DTRA



S. E. Diehl-Nagle, IEEE TNS, NS-31, 1145 (1984)

17



Micro-dose Conclusions

DTRA

- First observed in 1M SRAMs
- Predicted in DRAMs, and observed later
- At 2008 NSREC, several papers where failures were observed in other circuits, attributed to micro-dose
- With continued scaling, more devices seem to be becoming sensitive

18

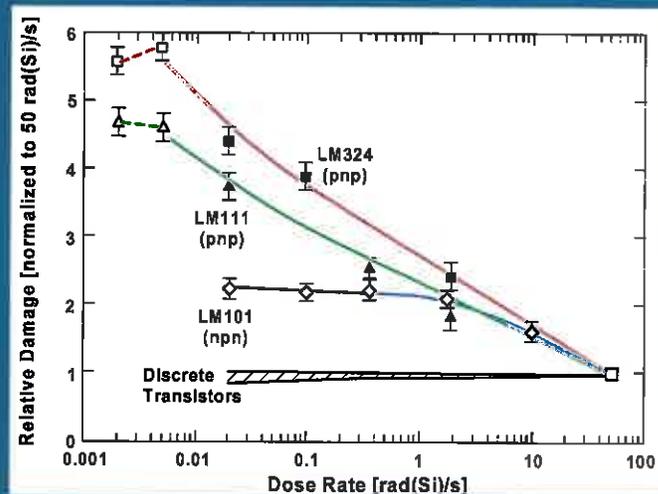


ELDRS

- Enhanced Low Dose Rate Sensitivity discovered by E.W. Enlow et al. (IEEE TNS, 38, 1342 (1991).
- Attributed to radiation damage in bipolar isolation oxides—underlying mechanisms still not fully understood
- Standard test method established



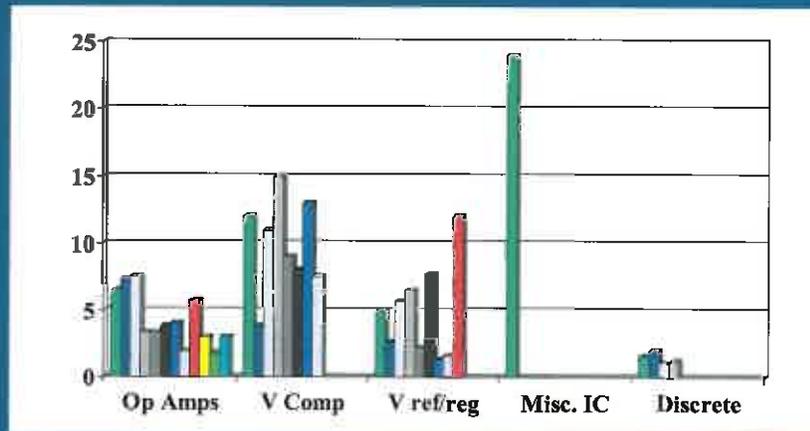
ELDRS



A.H. Johnston et al., IEEE TNS, 41,2427 (1994).



Damage Enhancement Factors



After R.L. Pease et al., NSREC REDW, 2001.

21



SEE Background

- Remember when there were no SEE—result of scaling
- New SEE problems discovered almost every year
 - Ion induced breakdown
 - SET, starting around $0.25\mu\text{m}$ technology
 - multiple bit upsets increasingly significant
 - upsets from direct ionization of protons
 - SEFIs from processor errors in advanced memories

22



Single Event Effects (SEE)

- SEU—Single Event Upset
- SEL—Single Event Latchup
- SES—Single Event Snapback
- SEB—Single Event Burnout
- SEGR—Single Event Gate Rupture
- SET—Single Event Transient
- SHE—Single Event Hard Error (Micro-dose)
- SEFI—Single Event Functional Interrupt

23



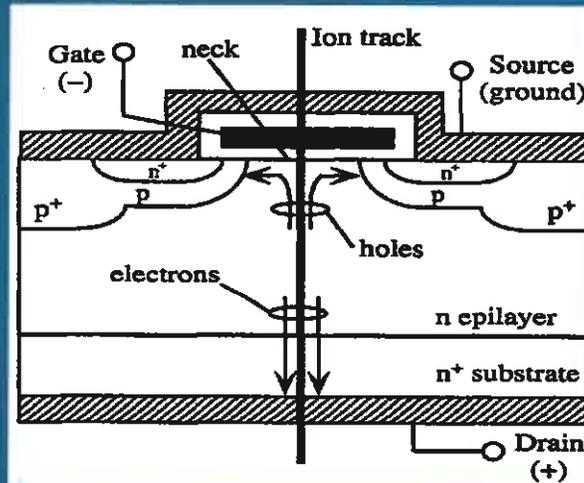
Hard Breakdown

- Ion-induced hard breakdown is SEGR
- SEGR proposed as second mechanism for stuck bits (G.M. Swift et al., IEEE TNS, Dec 1994)
- Sexton (IEEE TNS, June 2003) concluded thinner oxides have higher intrinsic breakdown fields, SEGR in digital circuits not expected below 5 MV/cm.

24



Gate Rupture Conceptual Model



After J.R. Brews et al., IEEE TNS, NS-40, 1929 (1993).



Soft Breakdown (SBD)

- Slight increase in leakage current, attributed to oxide damage
- Shown by J.F. Conley, et al. (IEEE TNS, Dec 2001) to start with the first ion strike in oxides 3 nm or less
- Massengill et al., (IEEE TNS, Dec 2001) argued that SBD-induced leakage current too small to matter in most applications, which is true, BUT...
- ...Suehle et al., (APL, 80, 1282 (2002)) showed reliability is significantly degraded in life tests after SBD observed



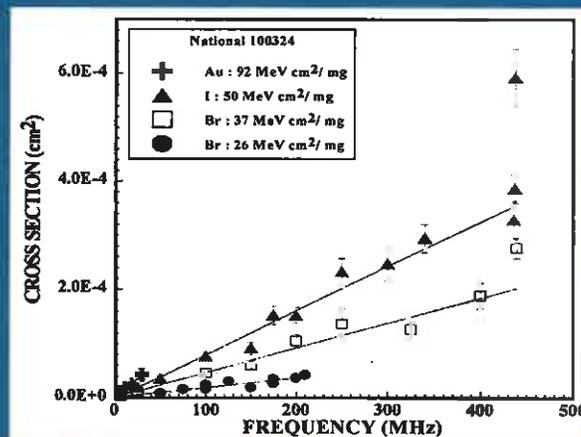
Track Formation (after Fleischer et al.)

- Fleischer et al. (*Nuclear Tracks in Solids*, 1975) find that cosmic rays form etch pits in insulators (glass or plastic), but not in semiconductors or metals
- Consider seven different models
- Conclude damage is due to free carrier interactions, rather than direct atomic scattering
- Ion explosion spike—coulomb repulsive forces between atoms along the track so high that atoms are displaced and bonds broken
- Normal displacement damage and delta rays among other models, that they dismiss

27



SET Frequency Dependence



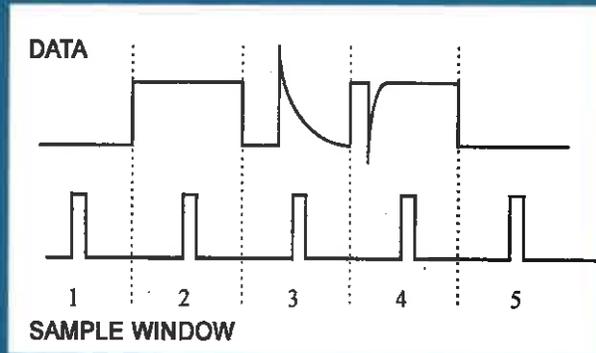
R.A. Reed, et al., IEEE TNS, NS-43, 2862 (1996).

28



DTRA

SET Sample Data



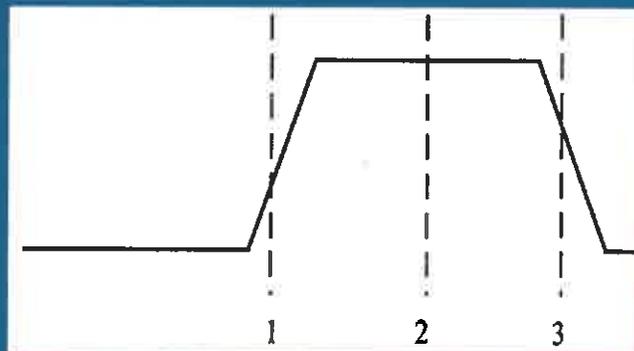
R.A. Reed, et al., IEEE TNS, NS-43, 2862 (1996).

29



DTRA

Data Pulse with Rising and Falling Edges

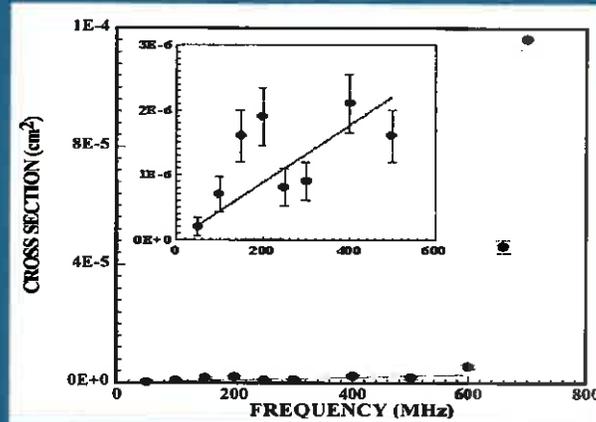


R.A. Reed et al., IEEE TNS, NS-43, 2862 (1996).

30



SET Results—Maximum Operating Frequency



R.A. Reed, et al., IEEE TNS, NS-43, 2862 (1996).



Effect of Scaling on SET

- SET identified as a problem in logic circuits because of scaling
- Frequency dependent—operating at higher frequencies is a main goal of scaling
- Transients are more likely to cause circuit effects at low voltage
- Obvious mitigating strategies (higher voltage, lower frequency) will never be attractive



Error Correction

- All major companies have their own proprietary error correction systems, and have for decades
- Error correction has usually been implemented at the system level, not on-chip
- Simplest and most widely used is Hamming code (Hamming, 1950)
- For a word with 2^n bits, $n+1$ parity bits necessary for single error detection and correction
- To also detect (but not correct) double errors requires $n+2$ parity bits

33



EDAC Case Studies (1)

- NASA Toms/Meteor3—about 350 errors/day for 2 years, with no uncorrected errors
- NASA SAMPEX—about 100 errors/day for one year, with no uncorrected errors
- Both used Hamming code for single bit error detection/correction, plus BIT (Built in Test) for hard errors, for SSR
- K.A. LaBel et al., IEEE REDW, p. 77 (1993).

34



EDAC Case Studies (2)

- T. Sasada et al., IEEE TNS, 53, 1806 (2006).
- SSR containing 768 NEC 16M DRAMS, 1.3×10^{-7} e/bit-day w/o EDAC (i.e., 1600 errors/day)
- With Hamming SEC, 81 of 86 errors corrected in one test
- Reed-Solomon double error correction would have corrected 85 of 86 in the same test

35



EDAC Case Study (3)

- G.M. Swift et al., IEEE TNS, 47,2386 (2000).
- Cassini—SSRs with 640 Oki 4M DRAMs, EDAC at system level, but not on-chip
- SEE testing of single die, but not system
- Launched based on calculated EDAC rate—assuming adjacent bits in different words
- After launch—interleaving not turned on, adjacent bits actually in same word
- 37% of SBU not corrected

36



MBU

- Koga et al., (IEEE REDW, p. 45, 2000) report more than 100 bits upset by single ion
- Recommend that bits in same word be physically separated by $>100\mu\text{m}$ to insure that single bit error correction will work
- Commercial EDAC systems, designed to work at sea level, do not provide this separation

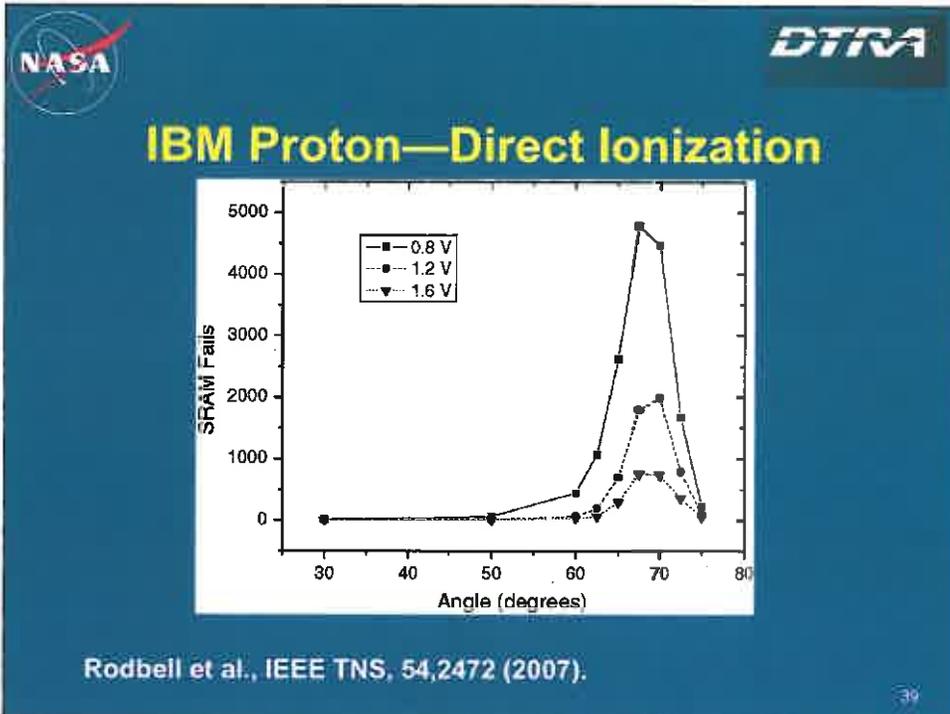
37



EDAC Conclusions

- Properly implemented, EDAC can be very effective--baseline requirement on all NASA systems
- Many practical problems in designing and implementing EDAC systems for space applications
- Difficult to test on the ground prior to launch—simply installing EDAC does not guarantee success

38



-
- Low Energy Proton Upsets**
- Bragg peak falls at surface of Si (70 KeV protons)
 - Residual range is about $0.7 \mu\text{m}$, so proton almost comes to rest in sensitive volume
 - In space, very few protons will come to rest in just the right place, so error rate is expected to be small, compared to other mechanisms.
 - Results at 65 nm—expect higher error rate with each additional shrink



SEFIs

- SDRAMs and NAND flash are both controlled by on-chip processors
- Error modes of processors are far more significant than errors in memory array (J.M. Benedetto et al., IEEE TNS, Dec 2008)
- Similar results in NAND flash (T.R. Oldham et al., NSREC REDW, 2008)
- Lose millions (or billions!) of bits from one error in control logic

41



Conclusions

- Thinning oxides has reduced TID concerns, in general, but some problems because the oxide is thin.
- SEE originally emerged as a problem because of scaling.
- Continued scaling will cause different problems to emerge.

42