

Radiation Testing on State-of-the-Art CMOS: Challenges, Plans, and Preliminary Results

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Abstract: *At GOMAC 2007 and 2008, we discussed a variety of challenges for radiation testing of modern semiconductor devices and technologies [1, 2].*

In this presentation, we provide more specific details in this on-going investigation focusing on out-of-the-box lessons observed for providing radiation effects assurances as well as preliminary test results.

Keywords: CMOS; radiation effects; digital electronics.

Introduction

Radiation effects testing of electronics has become more challenging [3]. In particular, testability of devices for both total ionizing dose (TID) and single event effects (SEE) is continuing to provide major challenges.

In this talk, we shall consider these challenges as they pertain to radiation effects testing of modern commercial CMOS devices in the natural space environment. Both SEE and TID issues will be discussed focusing on specific examples and current plans. The approach will focus on radiation testing of both commercial devices as well as CMOS process test structures.

We will again ask and attempt to answer the following question: Based on increasing device complexity, can adequate parametric and functional measurements be made to support the use of a technology for operation in a critical space system application?

Manufacturers of complex devices such as processors invest tens of millions of dollars into creating test programs for multi-million dollar automated test equipment (ATE) to collect parametric measurements on such a device. For TID testing, functional and parametric measurements are the norm for monitoring device performance. Without vendor collaboration, this full TID characterization would be impossible on devices such as processors and FPGAs.

Discussion

The specific topics to be addressed in this paper will include SEE and TID radiation test results from a number of advanced technologies to include IBM 65nm technologies [4], TI 65nm technologies [5], and Intel 45nm Hi-K dielectric technology. A discussion of current advanced CMOS radiation testing plans and efforts will be included. In addition, radiation test data from selected other

advanced commercial microelectronics will be provided. Prior work (4) indicated an anomalous low energy proton SEE response on the 65nm technology node. This will be discussed including the issues involved with performing very low energy proton testing. Recommendations concerning the need for low energy proton testing will be provided.

Radiation Test Results: 65nm CMOS

NASA and DTRA have been working with two different commercial vendors (IBM and TI) to evaluate the inherent radiation tolerance of highly scaled CMOS devices. By determining the radiation-induced failure mechanisms, two key technology needs are met. They are:

- Develop a knowledge-base for future test guidance of commercial highly scaled devices, and
- Determine appropriate Rad Hard by Design (RHBD) techniques for new device development.

The IBM 65nm CMOS technology evaluated is a silicon-on-insulator (SOI) technology. Figure 1 is a photo of the test sample used. This particular package is designed so that irradiation may take place using the front (rather than the back) side of the packaged die.

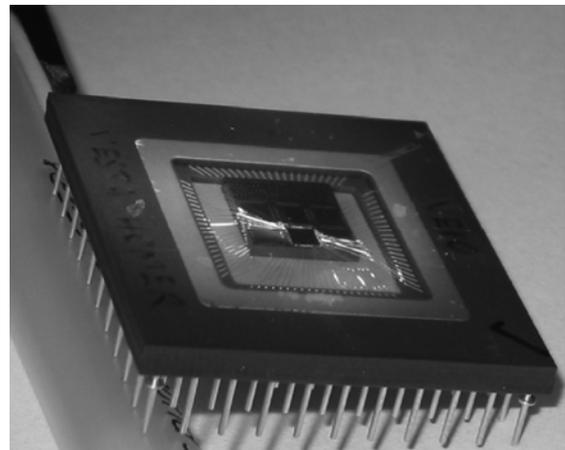


Figure 1. Photo of 1Mbit 65nm SOI SRAM used for "front-side" testing.

Whereas there are numerous radiation related conditions to consider such as particle arrival angle, energy deposition,

and single particles inducing multiple bit flips (MBU), the issues related to proton SEE testing is key. In particular, the low proton energy regime response has implications for both test and design that require consideration. Figure 2 illustrates the response of this test sample to a range of proton energies.

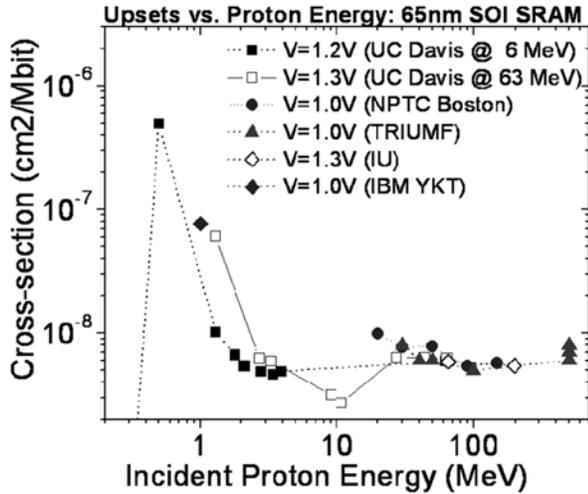


Figure 2. Data from 1-500 MeV at normal incidence.

In previous generations of CMOS technology, it has been noted that the response is relatively flat with energy for energies greater than ~25MeV. This dataset is consistent with the flatness for these higher energies, however, for energies <25MeV, the result is inconsistent. First, one would expect a drop in measured sensitivity below 25MeV based on previous technology generations. This is roughly observed between the 25 and 10MeV points, however, a rise in sensitivity is observed at energies below 10MeV.

One may wonder if this is an artifact of SOI technology, however as shown in Figure 3, bulk CMOS 65nm technology from TI shows a similar shape to its sensitivity.

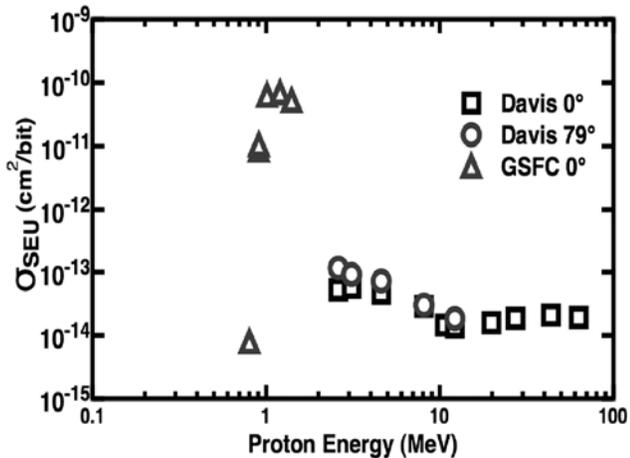


Figure 3. Proton test of bulk CMOS 65nm technology from TI.

There are several takeaway points to consider based on the low energy proton sensitivity. They are:

- Do we understand the mechanisms causing this increased sensitivity? Direct ionization (which is new for proton sensitivity) has been proposed.
- Even though shielding may reduce the number of protons impinging on the device in a space mission, higher energy protons are degraded in energy when passing through this material and create low energy particles that may increase the overall device SEU rate in space. And,
- Given that these are test structures where many details of the technology are available, how do we handle testing of commercial devices (like a FPGA, for example) that may have these same low energy issues? Efforts are underway to develop techniques to do just this using a qualitative if not quantitative approach to sensitivity estimation. Results of this work are expected later this year.

Radiation Test Results: 45nm CMOS

Preliminary TID data has been collected on the first commercially available Hi-K dielectric CMOS device, an Intel 45nm Wolfdale processor as seen in Figure 4. This is a dual-core processor with a 3 GHz clock frequency. In essence, two test campaigns are underway: a functional TID test where the device is irradiated then tested for power supply consumption and general functionality only and a full TID campaign where parametric measurements are taken. The functional TID testing was performed independent of Intel using strictly commercial motherboards and software to check performance. Tolerance to the 1 Mrad(Si) level was observed. Please note that the results can NOT be inferred as exceeding ITAR levels without parametric tests.



Figure 4. Intel 45nm Hi-K Wolfdale processor.

Given the complexity of the commercial, it is simply not feasible for an independent test organization to re-create the infrastructure (ATE and test vector coverage that cost many millions of dollars and time) that a complex device manufacturer owns. Hence, the only way to perform a

proper TID test would be to utilize this existing infrastructure to provide the measurements. However, this does provide some data sensitivity for the manufacturer and may limit how the data is shared. The full TID testing on the Wolfdale is underway now and results are anticipated this fiscal year.

Radiation Test Plans for FY09

Table 1 illustrates the general radiation testing plans and status for CMOS test efforts in FY09. The 45nm structures from IBM and TI are a high priority to gather data.

Table 1. General radiation testing plans and status for CMOS test efforts in FY09.

	90 nm	65 nm	45 nm	Notes
IBM		SOI and bulk SRAMs evaluated for SEE (proton and heavy ion)	SOI SRAMs received with preliminary data gathered	Collaboration with IBM and Sandia; Seeking structures for temporal SEE testing
Texas Instruments	TID on transistors completed (90 and 130 nm)	SEU/SEL on SRAMs completed; Awaiting transistors for TID	SRAM test structures received; Vanderbilt designing new test structures	Collaboration with TI and Vanderbilt; Experiments also performed at temperature
SIRF Program	TID on transistors completed	TID on transistors completed		Courtesy of Xilinx and AFRL; Experiments also performed with temperature
Intel		TID and dose rate completed	TID and dose rate planned on 1 st commercially available Hi-K device (Preliminary TID completed – functional only)	Collaboration with Intel and NSWC

Additional tasks related to scale CMOS include:

- Development of hardness assurance guideline for low proton energy testing,
- MBU analysis of 45 and 65nm CMOS,
- Commercial FPGA evaluation (65nm and below),
- Commercial Flash memory testing (including combined radiation and reliability implications),
- Commercial SDRAM radiation characterizations (including DDR3 and use of laser SEE test techniques),
- Support for DoD technology development programs, and,
- Tasks related to device preparation for radiation testing, combined radiation (TID impact on SEE) effects, and elevated temperature consequence on radiation response.

Summary

We have presented an overview of on-going investigations into the radiation sensitivity of emerging CMOS technologies. General trends indicate improving tolerance to TID, but new and increased sensitivities to SEE. By continuing to evaluate the state-of-the-art, we can provide a significant risk reduction for the development of new RHBD products as well guidance for testing new commercial electronics.

References

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