To be published in IEEE Transactions on Nuclear Science (TNS), December 2009.

TPA Laser and Heavy-ion SEE Testing: Complementary Techniques for SDRAM Single-Event Evaluation

R. Ladbury, J. Benedetto, D. McMorrow, S. Buchner, K. A. Label, M. D. Berg, H. Kim, A. Sanders, M. Friendlich, A. Phan

Abstract— We report on complementary use of two-photon absorption laser and heavy-ion SEE testing to evaluate the single-event response of SDRAMs. The tandem testing technique helps disentangle the response of devices exhibiting multiple SEE modes.

Index Terms— single-event effects, SDRAMs, reliability estimation, quality assurance

I. Introduction

Increasing use of complicated microcircuits in critical spacecraft applications has increased the need for economical methods for single-event effects (SEE) characterization. SEE testing of such devices is challenging for several reasons:

1) **Cross Contamination**: Vulnerability to multiple SEE modes (e.g. single-event upset (SEU), multi-bit upset (MBU), single-event functional interrupt (SEFI) and single-event latchup (SEL)) makes it difficult to disentangle the effects and accumulate sufficient statistics for confident rate calculation, especially for rare modes.
2) **Testability**: Microcircuit packaging, metallization and design limit the ability of test beams to reach SEE sensitive volumes, while multiple operating modes often make full characterization impractical.
3) **Error Latency**: The large sizes and complex operations of these devices can give rise to a significant time between an error's occurrence and its discovery. This latency can lead to overestimation of the ion fluence needed to produce the error, especially when the device is operating at slow speed.
4) **Repeatability**: Long error latency coupled with high vulnerability to control logic errors means the state of the device when a given error occurred is uncertain.

Although, Synchronous Dynamic Random Access Memories (SDRAMs) pose all of these challenges, they are indispensible in applications requiring large amounts of dense, low-power memory. However, because of their susceptibility to SEE induced data loss, SDRAMs are not usually used to store mission critical information. As such, the decision to use SDRAM to store critical spacecraft health and housekeeping data in the Magnetospheric Multiscale (MMS) mission[1] Control and Data Handling (C & DH) system provided a particularly demanding SDRAM application.

The candidate memory for this application is the Elpida 512 Mbit EDS5108ABTA-75 (Lot Date Code=0805) SDRAM. Previous testing showed this device to be SEL immune up to LET~65 MeVcm2/mg.[2] However, the SEFI rate was higher than previous generations, and different studies gave slightly different pictures of SEU and SEFI susceptibilities.[3],[4] Reference 3 reported a higher SEFI cross section and a much lower SEU cross section than references 4 or 2. While these differences likely arise from the difficulty of analyzing complicated SEE data and different test methods, the differences had important implications for the mitigation the MMS application would need. Both references 3 and 4 agreed that onset LET for unrecoverable SEFI exceeded 20 MeVcm^2/mg—implying that protons could not induce these errors. However, the cross section at the lowest LET where these errors were measured is only a factor of 2-3 below the saturated cross section, and the disruptive nature of SEFIs means that these conclusions are based on limited statistics.

To understand the implications of the SDRAM's SEE response for the MMS application, the Goddard Space Flight Center (GSFC) Radiation Effects and Analysis Group (REAG) performed a laser test of the part to complement heavy-ion testing. Although previous studies had carried out topside irradiation of SDRAMs,[5] the dense metallization covering much of the memory array and the thick lead frame covering the die's center meant that this option would require expensive repackaging of the die. We opted to irradiate the memory from the backside using two-photon absorption (TPA) laser testing.[6],[7],[8] Because the greater penetrating

Manuscript received July 17, 2009. The authors thank NASA's Electronic Parts and Packaging (NEPP) program and the Defense Threat Reduction Agency, IACRO-

Ray Ladbury is with NASA Goddard Space Flight Center, Greenbelt, MD 20771, USA (phone: 301-286-1030; fax: 301-286-4699; e-mail: raymond.L.Ladbury.1@gsfc.nasa.gov).
J. Benedetto is with Radiation Assured Devices, 5017 N. 30th St., Colorado Springs, CO 80919 (USA), phone : 719-531-0800, email : jbenedetto@radiationassureddevices.com
D. McMorrow, Naval Research Laboratory, Code 6816, Washington, DC 20375 (USA)
S. Buchner, Global Strategies Group, 2200 Defense Highway Crofton, MD 21114 (USA)
Kenneth A. Label, and Anthony Sanders are with NASA Goddard Space Flight Center (/GSFC), Code 561.4, Greenbelt, MD 20771 (USA)
Melanie D. Berg, Hak S. Kim, Mark, R. Friendlich and Anthony Phan are with MEI Technologies, Inc., c/o NASA Goddard Space Flight Center (GSFC), Code 561.4, Bldg. 22, Rm. 052, Greenbelt, MD 20771 (USA), phone: 301-286-2153, email: Melanie.D.Berg@nasa.gov

power of TPA testing makes it better suited to testing double-data-rate (DDR) SDRAMs mounted in flip-chip packages, the Elpida SDRAM also offered a chance to develop a test technique to complement heavy-ion irradiation of future complex devices.

In this work, we discuss development of this test strategy. We first discuss the MMS mission and the C&DH SDRAM application. Next, we consider how laser testing complements heavy ion testing and part procurement and preparation. We next discuss the laser test procedure and how the test results influenced the subsequent heavy-ion testing. We then discuss the results of all tests and evaluate implications for MMS. Finally, we discuss challenges of TPA laser testing, along with strategies for maximizing the value of the technique as a complement to heavy-ion SEE testing of complicated devices.

II. MMS AND SDRAM APPLICATION

MMS's mission is to study magnetic reconnection events, particle acceleration and other phenomena in boundary regions in Earth's magnetosphere. The two-phase mission will fly a constellation of 4 satellites first exploring the sunward side in an orbit out to 12 earth radii (R_E), and in the second-phase looking at the magneto-tail in an orbit with apogee $25R_E$. (See figure 1.) The highly elliptical orbits mean that the satellites will not always be able to relay data to ground stations, so they will need enough memory in the C&DH to hold health and housekeeping data for up to 2 orbits (6 days). These orbits will expose the satellites to a variety of radiation hazards including trapped protons near perigee and unattenuated solar and galactic cosmic ray (GCR) particle fluxes for much of the orbit. Moreover, much of the most interesting science for MMS will take place during times of high solar activity. The high proton flux in critical phases of the mission makes it important to verify the onset LET for unrecoverable SEFI and ensure protons cannot cause these errors.

The C&DH application calls for two stacks of six 512 Mbit die for each satellite to store data for up to 2 orbits (6 days). The C&DH will use Reed-Solomon Error Detection and Correction (EDAC), regular error scrubbing and interleaving of words across multiple SDRAM die to ensure that any error confined to a single die is correctable. However, mitigating SEFIs that require a power cycle or chip reset would require additional expensive measures, since all die in a stack share common power and clock, and resets or power cycles would result in the loss of all data on a stack. It is important to assess whether the frequency of such errors would justify the cost of mitigating them.

In addition, the rate for block errors and SEU has important operational implications, since it determines the required memory scrub rate. Since the C&DH is responsible for the satellite health and safety, it is important that scrubbing and other maintenance tasks not interfere with normal operations.

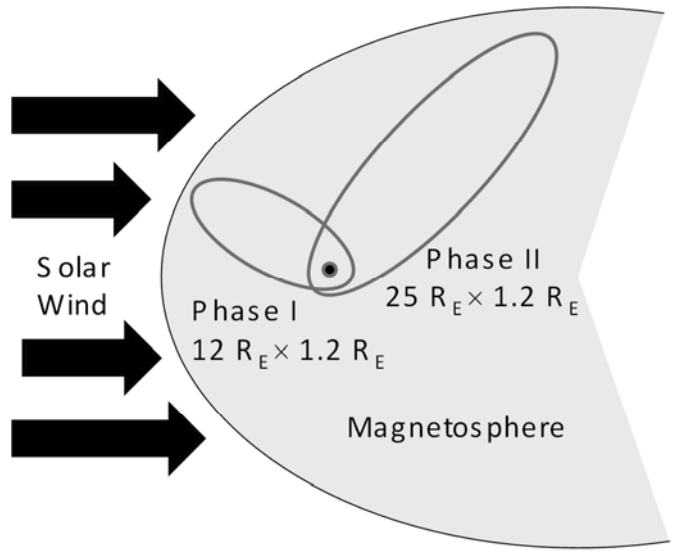

Fig.1 The MMS Mission will explore magnetic reconnection events in two phases. Phase 1 will explore the events on the daytime or sunward side in highly elliptical orbit 12 by 1.2 Earth radii (R_E). In phase II, the orbit apogee will be raised to 25 R_E and the satellites will explore recombination events on the night-time side. In both phases, the satellites pass through the protons belts and are exposed to the full solar particle flux on every orbit.

III. TPA LASER TESTING COMPLEMENTS HEAVY-ION TESTING

In broad-beam heavy-ion testing we have no control over where we induce an error, and long memory read times limit our ability to determine when the error occurred or the state of the memory when the error occurred. In contrast, laser SEE testing stimulates a single known node (control logic or memory) and we then observe the effects. Unfortunately, light from conventional laser testing cannot reliably penetrate to device sensitive volumes when the device is mounted in a flip-chip package or when metal lead frames and/or metallization obscure significant portions of the die. TPA laser testing eases the difficulties of stimulating device sensitive volume, because it uses infrared (IR) light (wavelength=1.26 microns), with photon energy below the electron-hole pair production threshold in silicon, so the die is transparent to the beam. The laser beam produces charge only at the focus where the laser pulse irradiance is sufficiently high to produce charge via two-photon absorption. (See figure 2.) As with conventional laser testing, the micron-sized laser spot probes individual features of the device under test (DUT), eliminating the risk of multi-mode data contamination.

Unfortunately, because the TPA cross section depends on the square of the laser pulse irradiance, I, small changes in pulse irradiance or inhomogeneities on the backside DUT surface significantly change the charge delivered to the sensitive volume. This makes it very difficult to evaluate the equivalent LET for the laser beam. Thus, while TPA laser testing is invaluable for elucidating the types of errors the memory can exhibit, heavy-ion testing is still needed to provide cross section vs. LET curves for rate calculations and to validate TPA test results for an environment with greater fidelity to the space radiation environment. TPA laser testing complements rather than replaces broad-beam heavy-ion

testing. TPA laser testing is also an invaluable tool for validating SEE test procedures, hardware and software prior to the heavy-ion test.

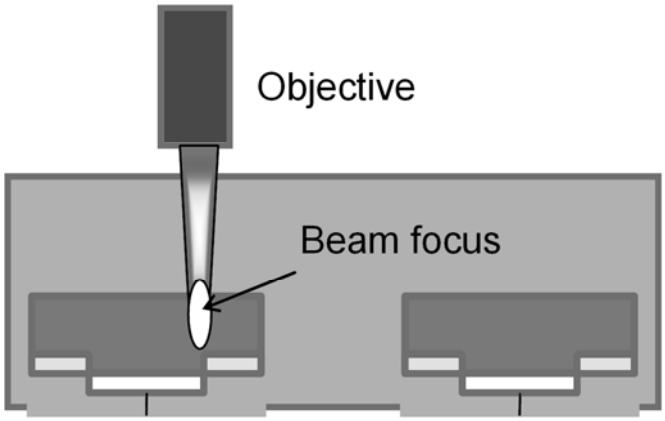

Fig. 2 Two-photon absorption laser SEE testing uses an infrared laser beam with wavelength below the electron-hole pair production threshold. Charge generation occurs only at the beam focus where the probability of absorbing two photons is significant.

IV. Part Procurement and Processing

3D Plus, the manufacturer of the stacked package, made available several individual parts from the flight lot for testing and evaluation by GSFC. Five of these SDRAMs were thinned to about 50 microns by Radiation Assured Devices (RAD). Prior to thinning, the parts were mounted on daughter boards that interfaced to the GSFC Xilinx Spartan II-based Low-Cost Digital Tester (LCDT).[9] The daughter boards added structural integrity to the parts and improved yield during the thinning process. At RAD, the parts were lapped to the desired thickness and then sent back to GSFC so the rest of the parts on the daughter board could be populated.

In addition to the thinning, the backsides of the parts were polished to a near-specular finish to minimize loss of laser light at the die's back surface. (See figure 3.) This is important not just so that the laser can focus on the sensitive volumes of the device, but also so that the test system's IR camera can image device features. In fact, the ability to image device features with the IR micrograph is a good practical criterion by which to judge the adequacy of backside polish. At the test site, when we found that the initial polish of the thinned parts was too rough, we polished the parts by hand using laps impregnated with diamond grit until we could image device features and induce upsets with the laser. This hand polishing took about 20 minutes per device and could be done despite the fact that the daughter boards were fully populated. Despite the thinness of the die, none was damaged by gentle polishing. Other parts—especially those mounted in flip-chip ball grid array (FBGA) packages have exhibited greater fragility.[10]

V. TPA Laser Test Procedure

The goals of the laser test were:

1) Determine susceptibility to unrecoverable SEFI—that is SEFI requiring a power cycle or chip reset for recovery
2) Determine the distribution of the numbers of bits upset by control-logic and address errors.
3) Determine the relative susceptibility (e.g. onset energy) of control-logic and memory-cell upsets
4) Enumerate the SEFI, block error and other control logic upsets to which the memory is susceptible
5) Determine whether memory-cell upsets could involve multiple bits in the same logical word.

At the test site, we mounted the GSFC LCDT board on the TPA translation stage with the DUT under the laser system's 100× objective lens. (See figure 4.) DUT Power was supplied and controlled by National Instruments' Labview®-based software running on a laptop. During irradiation, this system monitors for sudden, large current increases that might indicate a SEL. The LCDT controlled all other DUT functions (operating mode, test pattern, test type, clock speed, etc.).

The DUT was then positioned under the objective in line with the camera system and laser beam, and both the IR lamp and the laser were focused on the sensitive volume. As the translation stage was moved under the laser beam, we navigated using the DUT image from the system's IR camera.

Most of the control logic for the Elpida SDRAM was located in a strip running down the center of the part, while the memory array was located on either side of this strip. The control-logic features were easily discernible (figure 5), while those of individual memory cells (figure 6) could not be resolved with the resolution of the microscope (~1 micron).

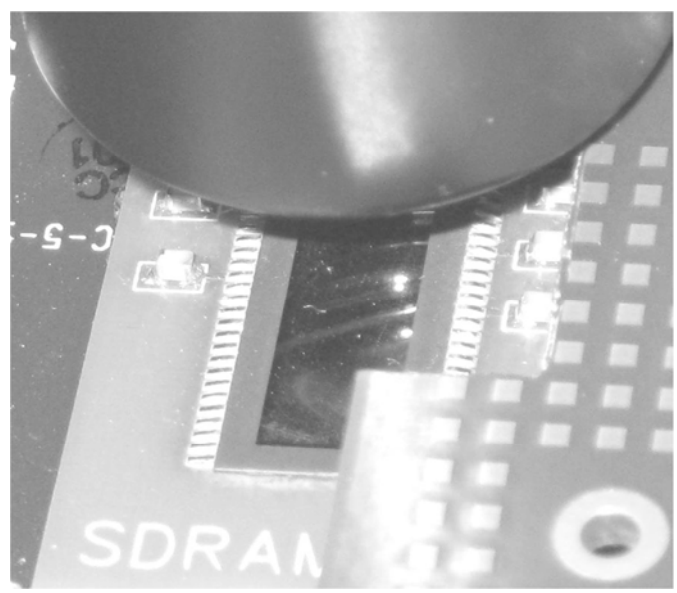

Fig. 3 For TPA laser testing, the backside of the device must be polished to a near specular finish, as is evident from the reflection of the objective lens.

To determine the relative sensitivities of control logic and memory cells, we first focused the laser pulse on a control logic cell in the center of the memory and varied the laser pulse irradiance, beam position and focus until we determined the laser energy that just barely produced upsets. We repeated this with the beam spot illuminating a block in the memory array, again varying beam position, focus and irradiance to find the minimum irradiance that could cause upsets. We then repeated this procedure for several control-logic and memory locations to compensate for any lack of uniformity in surface finish or other factors affecting laser pulse irradiance in the sensitive volume. The ratio of the lowest energy that caused upsets in logic cells to that causing upsets in memory cells is a measure of the relative susceptibilities of the two cell types.

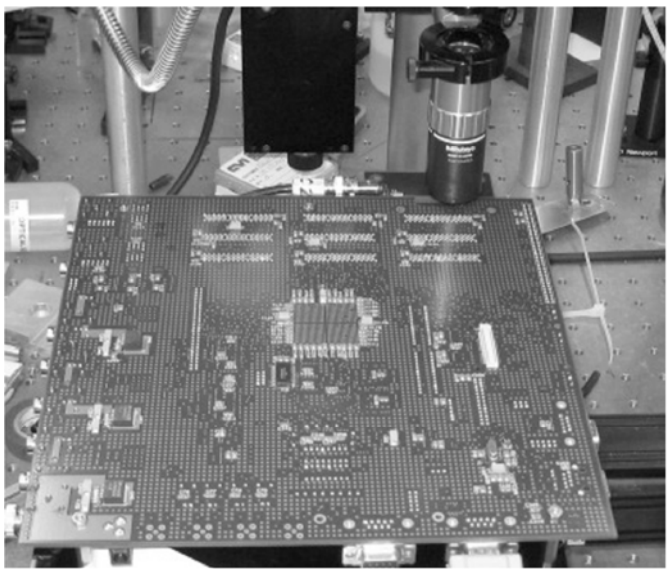

Fig. 4 TPA laser SEE test, showing the GSFC Low-Cost Digital test board, SDRAM daughter board, (partially obscured by the objective lens. The LCDT is mounted to a translation stage that moves the part in the plane perpendicular to the laser beam. Focus is controlled by changing the vertical position of the objective

The test procedure consisted of exploring the SEE behavior of the DUT: Picking a region, we scanned over it with the laser at moderately high pulse irradiance until we saw errors. Although most of the testing was done at high speed, a dwell time of several seconds was often required before the tester registered errors. Once we had isolated a sensitive region, we could change DUT speed, test pattern and other test conditions and look at how the device responded. While this was time consuming at first, efficiency improved over time. Precise positioning had little effect for the memory blocks, where feature sizes were much smaller than the beam focus. For control logic, it became clear quickly which features caused errors. Testing focused on these features, but we also sampled other structures to ensure they did not cause errors.

If we saw a burst of errors, we stopped the laser beam and verified that the device was still functional and that the tester was able to correct the errors in the memory. To ensure full functionality, we also verified not only that all the errors were correctable, but that the tester could write and verify a different arbitrary test pattern in memory. If a SEFI occurred, we would stop the beam and wait a few seconds to see if it would clear itself. We would then try to refresh DUT mode registers, and if this did not work, try a soft reset and then a power cycle as a last resort. Both the power cycle and the soft reset result in loss of data for MMS.

We verified the lack of SEL susceptibility seen in previous testing, both at room temperature and at 80 °C.

Once the laser testing had been completed, the data were analyzed and the errors were classified based on the number of upsets caused, the addresses of the errors, upset type (SEU or MBU) and any patterns in the bits that upset. Errors with common characteristics were grouped together. SEUs involved a single incorrect bit in a word with the error persisting until it was rewritten. Logic errors involved small clusters of upsets. Block errors consisted of bursts of errors, often with common row or column numbers. SEFI were those errors where a chip reset or power cycle was required to restore functionality.

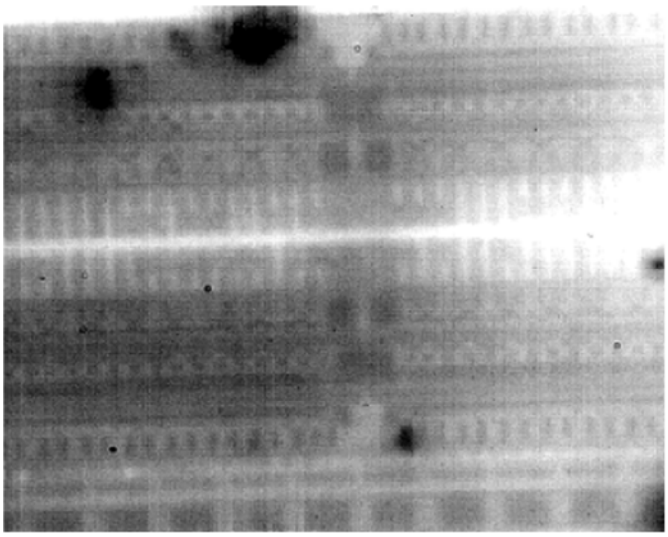

Fig. 5 Comb-like structures like those seen in the control logic running down the center of the SDRAM were responsible for most of the block errors and other logic errors seen in the test.

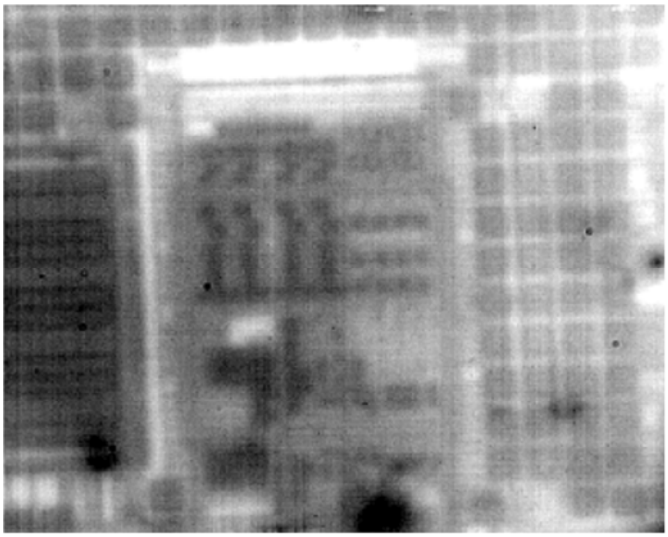

Fig. 6 Control Logic (center) is found even in the memory array of the SDRAM. Upsets of this logic produce from one to dozens of upsets at a time.

VI. TPA Laser Test Results

Given the complexity of SDRAMs and the variety of errors that can occur, error classification is somewhat subjective, and it is usually driven by system requirements and mitigation rather than any intrinsic quality to the errors. Reference 3 classified errors into five categories, while reference 4 chose four categories. The main difference is that Reference 3 recognizes a category in which an error looks like an SEU, but the memory contents are still correct when the mode register is reset and it is read again (Category 1). We also saw such "false SEUs," and they were associated with upsets in control logic rather than memory cells. However, we chose to group them with SEUs, because they would likely have the same system consequences and be dealt with in the same way for MMS. We chose the following error categories:

1. SEU—including the "false SEU" events reported by reference 3 and also seen in our testing.
2. Small logic errors—giving rise to fewer than 20 upsets (this level was chosen because such errors account for more than half of all logic errors and because they do not require increased scrubbing rates to keep error from accumulating.
3. Block errors—giving rise to 20-4096 upsets.
4. SEFI—requiring a power cycle or chip reset for recovery.

One surprising result was that the control logic upset threshold was ~18 mJoules, while the memory cells required 25 mJ. Since charge generation is proportional to the square of the laser pulse irradiance, this implies the onset LET for control logic upsets is about half that for memory-cell upsets.

Memory-cell errors upset only a single bit in a given word (no MBU), while control-logic errors produced as few as one error or bursts of as many as 4096 errors (see figure 7). Most of these errors could be corrected merely by writing the correct pattern over the affected word, although some errors required a reset of mode registers before a rewrite could be successful.

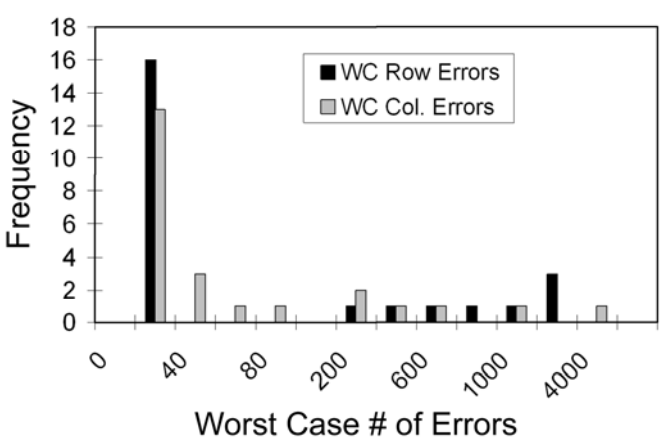

Fig. 7 The largest block errors are Row and Column errors. Most control logic locations give relatively few errors. Some features produce streams of several thousand contiguous words in error. Note the logarithmic scale on the x-axis.

We did observe one SEFI that required a power cycle for recovery. Although we searched the area that gave rise to this error repeatedly, both by hand and with an automated scan, no similar errors were observed. This suggests either that the vulnerable area for such errors is very small or that vulnerability only occurs when the memory is in a particular operating state. This error only occurred when the part was operated at our highest test speed of 100 MHz. Determining whether such errors could be induced under heavy-ion irradiation thus became a high priority for heavy-ion testing.

VII. TPA Influence on Heavy-Ion Test Plan

The main heavy-ion test goals were evaluation of SEFI vulnerability, comparison of the heavy-ion and laser-induced error modes and determination of cross section vs. LET curves for SEU, control-logic, block error and SEFI modes. The SEFI rate was important for determining whether proposed mitigation would be adequate for the C&DH application, while the other error rates would determine memory-scrubbing rates.

An important criterion for achieving the second goal was to limit the number of modes excited in each read cycle. This was especially important because the large cross section and low onset LET for control-logic upsets meant these would occur nearly as often as SEUs. One proposed strategy was to mask the control logic and memory array on different parts and test each separately. Unfortunately, laser testing revealed (see figure 6) that there is also control logic interspersed in the memory array, so the masking approach was not feasible. Upsets in this logic give rise to short bursts of errors, ranging in length from one to a few dozen errors, and some of the short bursts are indistinguishable from SEUs or MBUs.

Instead of masking the die, we used short runs with very low flux (<100 $cm^{-2}s^{-1}$) and fluence (<100 cm^{-2}) to increase the probability that subsets of the data would have only SEU or only control logic errors. To limit fluence inhomogeneities and improve statistics, we averaged cross sections over several runs. The short runs also reduced errors on fluence estimates. This last factor was particularly important for tests with slow clock speed, since the long latency for slow-speed runs can give rise to significant fluence errors.

We also carried out a few runs to high fluence with high LET ions to look for rare SEFI, SEL or other error modes. While we did not use these runs for error cross section estimates, they were important for establishing that TPA laser testing had not missed any important error modes. Heavy-ion testing was conducted at the Texas A&M University Cyclotron Facility. Heavy-ion testing was performed on the same devices used for laser testing, from the backside using the 25 MeV per amu accelerator tune. Table I lists ions used in the test. The memory was tested at 2 different angles for each ion, at 2 frequencies (10 MHz and 100 MHz) and with several different test patterns (all 0's, all 1's, AA, 55, checkerboard, etc.).

TABLE I: ESTIMATED MINIMUM RDM α

Ion-Energy (MeV)	Incident LET (MeV•cm²/mg)	Range in Si (μm)
Ne-545	1.7	799
Ar-991	5.4	493
Kr-2081	19.3	311
Xe-3197	37.9	286

The test setup and procedure were very similar to that used for TPA laser testing, using the same test modes and recovery procedures after a burst of errors was seen.

VIII. HEAVY-ION TEST RESULTS

During the TAMU heavy-ion testing, we observed only a single SEFI that required a power cycle for recovery. This error occurred under irradiation with Kr ions with LET ~22 MeVcm^2/mg. No similar errors occurred even at higher LET. The symptoms of this error mode were similar to that seen during laser testing. Both the heavy-ion and laser results support an interpretation of these errors being time/state dependent and occurring with low probability. This interpretation is also consistent with the sporadic occurrence of this error type reported in reference 4. Based on these factors, it is likely that the SDRAM is only vulnerable to this SEFI mode during a small portion of its normal operation, and the actual rates will be lower than those predicted in column 2 of Table II.

For the other error modes, our cross sections are higher than those reported in reference 3 and, except for SEU, in references 4. (See figure 8.) This is probably in part because of the low-fluence test methodology we used, which showed both SEUs and block errors occurred even with fluences less than 100 ions/cm^2. The result is that rates for block errors could be significantly higher than would be predicted by methods testing with higher flux and fluence. Fortunately, all of these errors are recoverable with at most a reset of the mode registers and rewriting the memory.

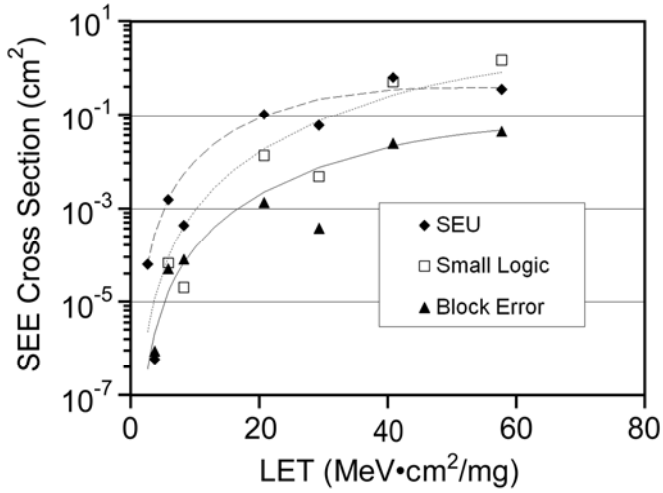

Fig. 8 Device cross Section vs. LET for SEU, Small Logic (<20 associated upsets) and Block Errors (>20 associated errors) based on current work.

IX. ON-ORBIT COMPARISON

The launch of the Lunar Reconnaissance Orbiter LRO in June 2009 provided an opportunity to benchmark the rates calculated using our test data. LRO's Control and Data Handling unit includes 4 data storage banks, each with 288 die of the same SDRAM selected for MMS. The LRO project provided data on upsets corrected by the Reed-Solomon EDAC during the first 19 days of the mission. SEUs, logic errors and block errors are all evident in the data. Table II compares the rates observed by LRO with those calculated using the heavy-ion data in figure 8 for the Solar Minimum Galactic Cosmic Ray environment. Agreement for SEUs, where statistics are fairly good is excellent, while the other modes give reasonable agreement given the limited statistics available. By comparison, the data used by LRO to estimate rates gave underestimated rates by over an order of magnitude, probably due to error latency effects and mode contamination.

TABLE II: CALCULATED VS. ON-ORBIT SEE RATES

GCR Rates	Predicted	Observed (LRO)*
SEU (bit^{-1}*day^{-1})	2×10^{-11}	9×10^{-12}
Logic Error (dev^{-1}*day^{-1})	1×10^{-2}	1×10^{-3}
Block Error (dev^{-1}*day^{-1})	3.5×10^{-3}	2×10^{-4}
SEFI (dev^{-1}*day^{-1})	$\sim8\times10^{-6}$	$<10^{-5}$

* based on data through 7 July 2009.

X. TPA Laser Testing: Lessons Learned

Although TPA laser testing was an excellent complement to broad-beam heavy-ion SEE testing, it poses challenges. Many of these challenges arise because of the I^2 dependence of charge production via TPA. Because of this, light reaching the sensitive region can be significantly diminished by backside surface imperfections or inhomogeneities or heavily doped substrates (in which light is lost by free-carrier scattering). Also, TPA laser testing has limited resolution—both spatially and temporally (due to error latency). This can limit the technique's utility for resolving low-probability error modes.

The following "lessons learned" were developed to mitigate some of these challenges.

1) Since our technique uses TPA laser testing in conjunction with heavy-ion testing, most parts will require thinning so that ions will reach the sensitive volume. We opted to use thinned parts for TPA laser testing as well, because it reduced concern about possible attenuation of the laser beam by heavy doping in the substrate and obviated the need to conduct substrate resistivity measurements.
2) Mounting the SDRAM to a daughter board prior to thinning and polishing increases yield and decreases the probability of subsequent failure in transit or handling. This is even more important for fragile parts, especially those mounted in FBGA packages.
3) Even if the die are polished after thinning, it is prudent to be able to do additional polishing at the test site. Surface imperfections left over from thinning or polishing or subsequent handling may not become evident until they are imaged as high magnification. Such imperfections may adversely and unpredictably affect the TPA process.
4) Although surface imperfections can affect the laser pulse irradiance reaching sensitive volumes, their influence is local. As such, one can take advantage of the repetitive structure of the memory array and control logic by irradiating several similar structures while looking for upset thresholds. As long as the individual structures do not vary too much in sensitivity, the minimum energy that generates an SEE can be looked upon as the threshold. If significant variability is expected, the mode of the distribution of energies is a better choice.
5) Rare error modes are problematic whether the rarity derives from a small cross section or from a short vulnerability window. Because laser testing localizes the effect, it makes it possible to scan over the same vulnerable region repeatedly. Automatic scanning is advantageous for such repetitions. In addition, because of the potential for error latency, these automated scans should be carried out initially at the highest operating speed to minimize uncertainty about the location of the vulnerable feature.

All of these lessons were very helpful for extracting information to supplement our understanding of heavy-ion test results. In particular, without 5), we would have had a very difficult time interpreting the single SEFI we observed during heavy-ion testing. The fact that repeated laser scans over the SEFI vulnerable area did not reproduce the error strongly suggests that the SDRAM is only vulnerable to this error mode at certain times during its normal operation.

XI. Conclusions

TPA laser testing is a unique tool for evaluating SEE response of complicated microcircuits. It presents an opportunity to explore the different SEE modes a part can exhibit prior to heavy-ion testing, so that test methods, hardware, software and analyses can be optimized to understand the error modes of greatest concern for the system.

In the case of the 512 Mbit Elpida SDRAM, the combination of TPA and heavy-ion SEE testing resulted in an efficient qualification of the memory for MMS. The qualification concluded with high confidence that the SDRAM would fulfill its requirements. The technique was particularly valuable for elucidating the nature of SEFI modes seen in heavy-ion as well as laser testing. Laser testing also helped to elucidate the distribution of upset number for various error modes, and this determines the on-orbit scrub-rate needed for the application. Moreover, the laser test helped to elucidate the signatures of the various SEE modes likely to be seen during heavy-ion testing so that the heavy-ion test method could be optimized to extract as much information as possible about the modes of interest and rates could be estimated accurately.

Because of the low onset energy and high cross section for SEFI and SEU, and because control logic was interspersed among the memory cells, our heavy-ion test called for runs with low flux and fluence to minimize cross contamination of SEE. Although we saw logic errors and/or SEUs on every run, this strategy yielded relatively clean data for cross section calculation. In part because our method is less susceptible to overestimating the fluence that caused the error, our calculated cross sections are up to an order of magnitude higher.

The knowledge gained from TPA laser testing complements the knowledge that we gain from heavy-ion testing. Laser testing does an excellent job of sampling the types of error modes. Because we can identify the features causing the errors, we can repeatedly stimulate them while varying test conditions (e.g. test pattern, frequency, device mode, etc.). Because of this control, we also have high confidence that we know the mode the device is in when it exhibits the error.

On the other hand, broad-beam heavy-ion testing is essential for rate calculation and for ensuring all modes are stimulated (high-fluence runs, albeit with device state highly uncertain). Heavy-ion testing also provides greater fidelity to SEE generation in the space environment.

The Elpida 512 Mbit part also proved to be an excellent candidate for developing and demonstrating the power of such complementary test techniques. This part has provided us with an opportunity to develop strategies that compensate for the weaknesses in both test methods and to maximize the synergy between them. We are confident of further improvements as we apply the technique to other parts in the future.

XII. Acknowledgements

The authors thank the NASA Electronic Parts and Packaging program, the Defense Threat Reduction Agency (IACRO-09-4987I) and the Magnetospheric Multi-Scale mission for support. We also thank the Lunar Reconnaissance Orbiter mission for the use of their DSB error data, and J. Pellish for technical support of these efforts.

References

[1] S. Curtis, The Magnetospheric Multiscale Mission... Resolving Fundamental Processes in Space Plasmas – Report of the NASA Science and Technology Definition Team for the Magnetospheric Multiscale (MMS) Mission – December 1999

[2] T. Langley, R. Koga and T. Morris, “Single-event Effects Test Results of 512MB SDRAMs,” IEEE Radiation Effects Data Workshop, pp. 98-101, 2003.

[3] J. Benedetto, “Examination of Single Event Functional Interrupts (SEFIs) in COTS SDRAMS,” 2006 Single-Event Effects Symposium, Long Beach, CA, April 10-12, 2006.

[4] Lawrence, R.K., “Radiation Characterization of 512Mb SDRAMs," IEEE Radiation Effects Data Workshop, pp. 204 – 207, 2007.

[5] A. Bougerol, F. Miller, and N. Buard, “SDRAM Architecture & Single Event Effects Revealed with Laser,” IEEE International On-line Testing Symposium, pp. 283-288, 2008.

[6] D. McMorrow, et. al., “Subbandgap laser-induced single event effects: Carrier generation via two-photon absorption,” IEEE Trans. Nucl. Sci., vol. 49, no. 6, pp. 3002–3008, Dec. 2002.

[7] D. McMorrow, et al., “Demonstration of Through-Wafer Two-Photon Absorption Induced Single-Event Effects,” IEEE Trans. Nucl. Sci., vol. 51, no. 6, pp. 3553–3557, Dec. 2004.

[8] D. McMorrow, et al., “Single-Event Upset in Flip-Chip SRAM Induced by Through-Wafer Two-Photon-Absorption,” IEEE Trans. Nucl. Sci., vol. 52, no. 6, pp. 2421-2425, Dec. 2005.

[9] J.W. Howard, et al., "Development of a Low-Cost and High-Speed Single Event Effects Testers based on Reconfigurable Field Programmable Gate Arrays (FPGA)," SEESYM06, April 2006.

[10] Ladbury, R. et al.., “Radiation Performance of 1 Gbit DDR2 SDRAMs Fabricated with 80-90 nm CMOS,” IEEE Radiation Effects Data Workshop, pp. 42 – 46, 2008.