Effect of Radiation Exposure on the Endurance of Commercial NAND Flash Memory

T. R. Oldham, M. Friendlich, M. A. Carts, C.M. Seidleck, and K. A. LaBel

***Abstract*—We have compared the endurance of irradiated commercial NAND flash memories with that of unirradiated controls. Radiation exposure has little or no effect on the endurance of flash memories. Results are discussed in light of the relevant models for electron and hole trapping.**

***Index Terms*—text**

I. Introduction

In this study, we have subjected unirradiated control devices to repeated Program/Erase (P/E) cycles to determine the endurance properties of the memories. Then we repeated this procedure on other parts irradiated to different doses, below the total ionizing dose (TID) failure levels for the parts, which had been determined previously. Normally, in floating gate (FG) flash memories, electrons are injected through a thin tunnel oxide into the floating gate to program (write) the zero state. Conversely, electrons can be removed from the floating gate by applying a large negative field, so that electrons are emptied out of the floating gate to erase the cell to the one state. It is well known that high field electrical stresses from programming and erasing cause oxide damage, which limits the endurance of the memory [1, 2]. Endurance failures occur primarily because of electron trapping in the tunnel oxide, which eventually causes cells empty of electrons (ones) to be read incorrectly as full of electrons (zeroes).

II. Description of Samples

The samples used in this study are 4Gb NAND flash memories from Micron Semiconductor (part number MT29F4G08AAAWP, LDC 744), and 8Gb NAND flash memories from Samsung (part number K9F8G08U0A, lot date code (LDC) 807), shown in Fig. 1. Both have 4K blocks, with 64 pages per block. The Micron parts have 2Kx8 page organization, plus 64 redundant columns, while the Samsung parts have 4Kx8 pages, plus 128 redundant columns. Both use nominal 3.3 V power supplies (2.7-3.6 V, full range), and they have the same 0-70º C commercial temperature range. All NAND flash products typically have a few bad blocks, which have to be screened out. For both manufacturers, the specification is <80 of the 4096 blocks will be bad, but in our experience, a number in the neighborhood of ten is more typical. Both the write (Programming) and Erase operations proceed by Fowler-Nordheim tunneling of electrons through the tunnel oxide. Fowler-Nordheim (F-N) injection requires very high fields, and the operation of a charge pump circuit to step up the power supply voltage. F-N injection also introduces damage into the tunnel oxide, contributing to wear-out. It is for this reason, that manufacturers typically guarantee flash memory only for 10^5 (P/E) cycles.

III. Experimental Procedure

Characterization of the test devices was performed using the NASA LCDT (Low Cost Digital Tester) system, shown in Fig. 2. Basically, five parts are tested in each test group—that is, five are cycled with no dose, for each manufacturer. Then five more parts are irradiated to the first dose increment, and cycled. Then five more are exposed at the next dose increment, and so on. Only 1% of each memory, 41 blocks, is actually cycled.

TID testing was done using a Co-60 source. This is a room air source, where the pencils are raised up out of the floor, during exposures. Active dosimetry was performed, using air ionization probes. Testing was done in a step/stress manner, using a standard Pb/Al filter box. The initial test was done in accordance with MIL-STD-TM 1019. Parts were under DC bias during exposures, but not actively exercised. Each test group of five devices were programmed with an all zero pattern during exposures, and biased at 3.6 V (nominal voltage, plus 10%).

IV. Results

The principal results are shown in Fig. 3 (Samsung) and Fig. 4 (Micron), for different doses after the parts have been exposed to 106 P/E cycles. We note that the endurance specification for both manufacturers is 105 P/E cycles, and that there were no errors on any part from either manufacturer at that level, at any dose level. We had to stress the samples about an order of magnitude beyond the manufacturers specification to get a measurable error rate. In Fig. 3, we show the results of stressing the Samsung 8G after radiation

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exposures of 0, 25, 50, and 100 krads (SiO2). For each group of five test samples, we plot the best response (fewest errors), the worst response (most errors), and the median response (third best or third worst of five). There is virtually no difference in the endurance response at any of the radiation levels. The variation within the five samples at each dose is much greater than the variation with dose. In Fig. 4, we show results of stressing samples of the Micron 4G through 106 cycles, for unirradiated controls, and after 20, 30, 50, and 100 krads (SiO2). There is more variation within the test group at each dose, and also between doses, than for the Samsung parts. Although there are more endurance errors after 20 and 30 krads (SiO2) than for the unirradiated controls, there is virtually no difference between the controls and the higher doses, which indicates the differences are not due to dose. Even when there is a variation with dose, the difference is less than that observed within the test group at each dose. The spread in the results for five devices tested under identical conditions typically shows a variation of two orders of magnitude, or more, which is larger than the difference between groups of samples tested under different conditions. Therefore, the differences observed from, say 0 to 20 krads (SiO2), are probably not statistically significant. Other results, in Figs 5 and 6, for higher cycle counts also show only minimal differences, well within the spread in the data for devices tested identically. Points for 20 and 30 krads (SiO2) shown in Fig. 4, are omitted in Fig 6 because the endurance test was stopped after 10^6 cycles. We note that many of the errors are intermittent at first. For this reason, we have plotted the average error count over an interval of 1000 cycles in Figs. 3-6. Therefore, error counts less than one are real average numbers--.001 means one error in a thousand cycles.

V. Discussion

There is an extensive literature on the reliability, including endurance characteristics, of flash memory (see, for example, [1] and its bibliography). Generally, the physical mechanism that causes endurance failure is electron trapping in the tunnel oxide. Chen et al. [2] showed that the programming window, the VT difference between programmed and erased cells, diminishes with cycling. They also showed that electron trapping in erased cells is the largest contributing factor. In the results presented below, the errors are primarily one-to-zero errors, which is consistent with electron trapping. Although one might think that radiation-induced positive trapped charge would offset the effects of trapped electrons, there is strong evidence that both positive and negative charge traps in SiO2 are due to the same oxygen vacancy defect center (OVDC). This idea is illustrated in Fig. 7 [3]. The first report indicating this conclusion was by Aitken [4], who was studying process-induced radiation damage. He concluded that a dipolar defect accounted for both positive and negative charge trapping. The negative end of the dipole could capture a positive charge, and the positive end could capture an electron. At the time, however, there was no known defect in SiO2 with a dipolar structure. Aslam [5] also supported the idea of a common origin for electron and hole traps, in a series of processing studies. Basically, he found that some oxide growth processes introduced more hole trapping than others, in hole injection experiments. In electron injection experiments, the oxides with high levels of hole trapping also had high levels of electron trapping. The structure of the radiation-induced trapped hole was identified by Lenahan and Dressendorfer [6], as the E□□□center. The defect, itself, had been known for many years, but they showed, through a series of annealing experiments that it correlated with radiation-induced trapped holes. The annealing of radiation-induced trapped holes had been well-known for many years. Then Lelis et al. [7, 8] proposed that some features of the annealing process could best be accounted for if an electron tunneled to the hole trap, but did not necessarily recombine with the trapped hole. Instead, it was trapped on another nearby Si atom, compensating the hole to restore net electrical neutrality, and forming a dipole structure, as originally proposed by Aitken. The dipole structure is metastable, in general, but the electron and hole can recombine under some circumstances, which reforms the strained Si-Si bond in the OVDC. Then, Walters et al. [9] proposed that the dipole structure suggested by Lelis et al. was the neutral electron trap sought by Aitken and others, which is neutral, but capable of trapping electrons, if they are injected. They conducted a series of electron injection experiments to test this idea. The results were a very strong confirmation of both the Lelis dipole structure, and also of the idea that it could capture a second electron to become a net negatively charged center, under appropriate conditions.

The large variability observed in the amount of electron trapping, within the groups of samples tested identically, is qualitatively consistent, both with the model and with other experimental results reported in studies of electron trapping. The dipole structure forms when a strained Si-Si bond is broken, and the Si atoms move apart as the lattice relaxes. In an amorphous material, there is expected to be a wide distribution of separation distances between the two Si atoms, which are the ends of the dipole [3]. The electron trapping cross section is a very strong function of this separation distance. For this reason, reported electron trap cross sections can vary by many orders of magnitude, even when measured by the same investigators [10, 11].

The threshold voltage shift from electron trapping necessary to cause a cycling error is on the order of 1V [1, 12]. But the maximum possible VT shift at the highest dose used in these tests can be calculated, using the expression

$$\Delta V_T = 1.9 \times 10^{-8}\, t_{ox}^2\, f(E)\, f_t\, D \qquad (1)$$

where tox is in nm, f(E) is the yield of charge (fraction of charge escaping recombination, which is on the order of 0.9 here), ft is the fraction of charge generated in the oxide that is eventually trapped there (typically 0.3-0.5 for unhardened commercial oxides), and D is the dose in rads (SiO2). If we evaluate this expression, assuming tox nm and the maximum

dose (105 rads (SiO2) in these experiments) we get a result of about 50-100 mV, or 5-10% of the total electron trapping necessary to cause a cycling failure.

On one group of samples, the Micron unirradiated controls, we stopped cycling at about $3.5x10^6$, and set the parts aside. A few months later, we resumed cycling, to check for annealing effects. Recovery of electron traps has been reported in the literature [13, 14], so we expected to see some effect. The results are shown in Fig. 8. All but about 1% of the errors had apparently recovered. But when cycling was resumed, the recovered bits all failed again within about $2x10^5$ P/E cycles. Apparently, the threshold voltage shift had partially recovered, but not all the way back to the pre-stress distribution. We do not have enough data to make a strong quantitative statement, but the endurance will apparently be better than our results indicate if the stressing duty cycle is not continuous, as in our tests, because the parts would have more time to recover during the P/E cycling.

VI. Conclusions

We point out that the manufacturer's specifications for these flash memories is endurance up to 10^5 cycles, and that no DUT had a cycling error until several times the specification in any of our tests. Many of them had no errors even an order of magnitude past the specification. The purpose of this study was to determine if the endurance of these memories would be degraded by radiation exposure. The most widely accepted model for electron trapping predicts leads to a prediction that radiation exposure should degrade the endurance, somewhat, but the effect is expected to be small. The experimental results tend to confirm this prediction—changes observed so far are within the scatter of the data, and are not thought to be statistically significant.

Fig. 1. Micron 4Gb NAND flash memory.

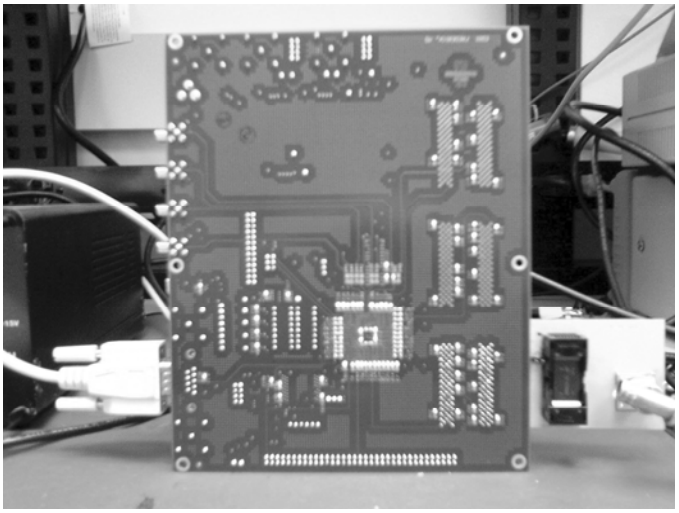

Fig. 2. LCDT mother and daughter boards.

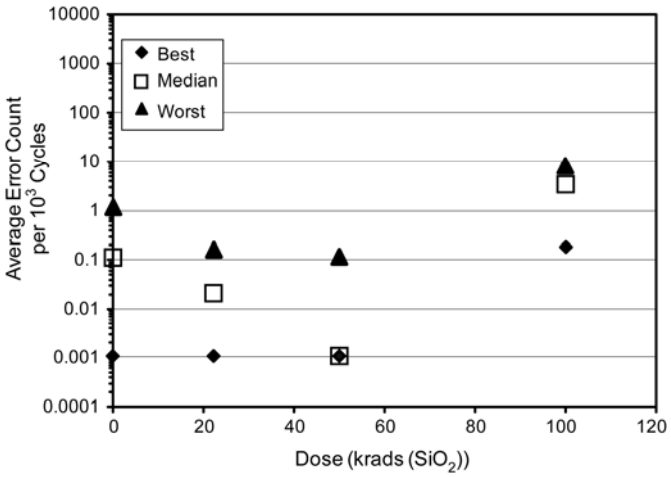

Fig. 3. Averge error count after 106 P/E cycles for Samsung 8Gb NAND flash as a function of radiation dose.

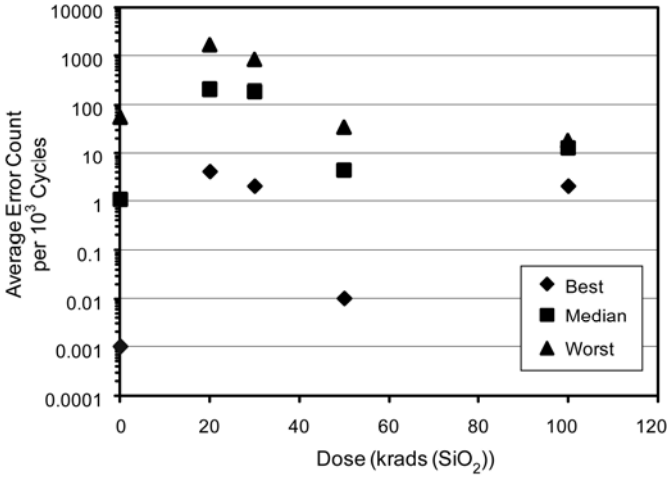

Fig. 4. Average error count after 106 P/E cycles for 4Gb Micron NAND flash as a function of radiation dose.

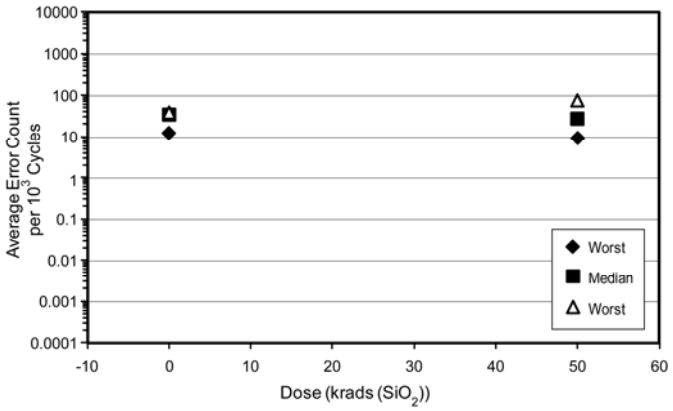

Fig 5. Average error rate for Samsung 8Gb after 4x106 P/E cycles.

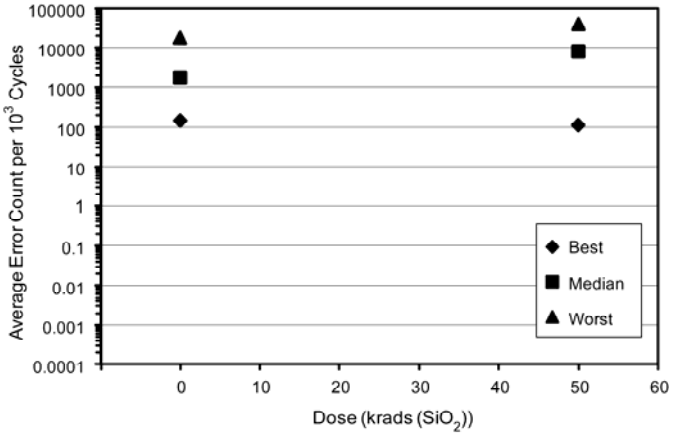

Fig 6. Average error rate for Micron 4Gb after 3x106 cycles.

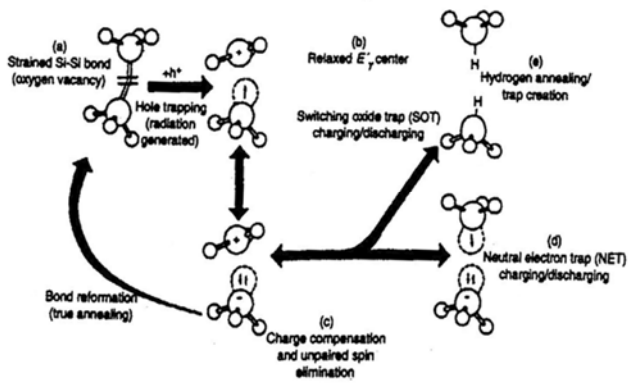

Fig. 7. Model for oxygen vacancy defect center, acting as both hole and electron trap [12].

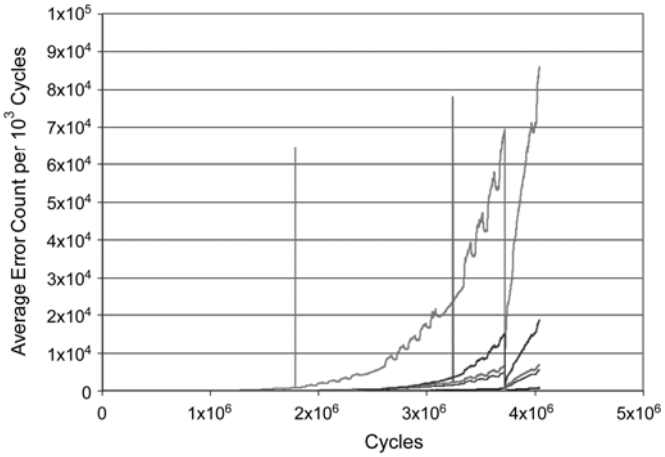

Fig. 8. Recovery of Micron parts when P/E cycling is interrupted, and subsequent failure when cycling is resumed.

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