SEU Analysis of Complex Circuits Implemented in Actel RTAX-S FPGA Devices

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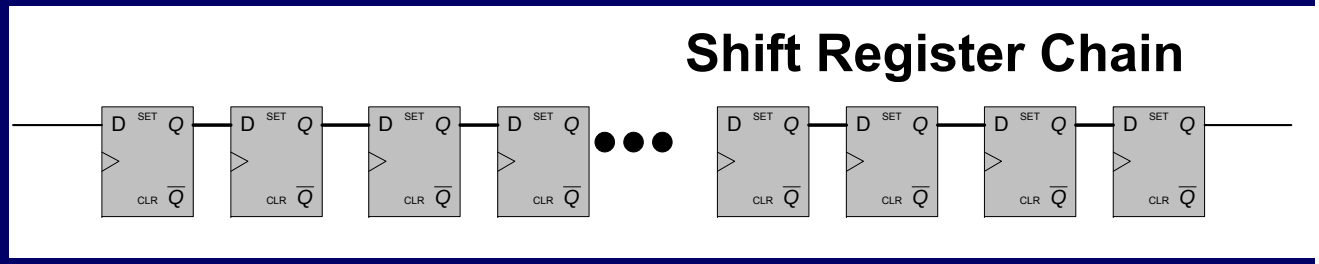
NASA/GSFC Radiation Effects and Analysis Group

Sponsors:

NASA Electronic Parts and Packaging (NEPP) Program

Motivation

- Single Event Effects (SEE) FPGA characterization is utilized to predict design error rates
- Conventional SEE test methodology is shift register (SR) based

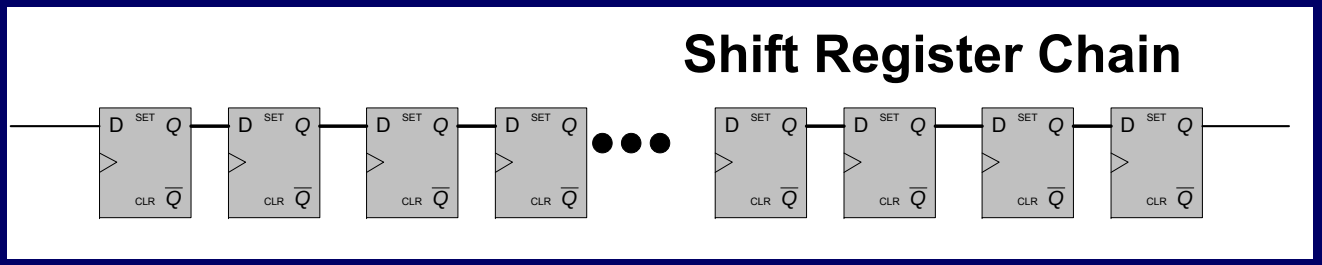


- Traditionally, System Error rate (dE/dt) is calculated using the SR bit error rate (dE_{bit}/dt) and the number of used DFFs

$$\frac{dE}{dt} < \frac{dE_{bit}}{dt} * (\#UsedDFFs)$$

Where Does dE_{bit}/dt Come From?

- SR logic is linear $$SR_{\text{fanout}} = SR_{\text{fanin}} = 1$$



- Most designs are complex and have

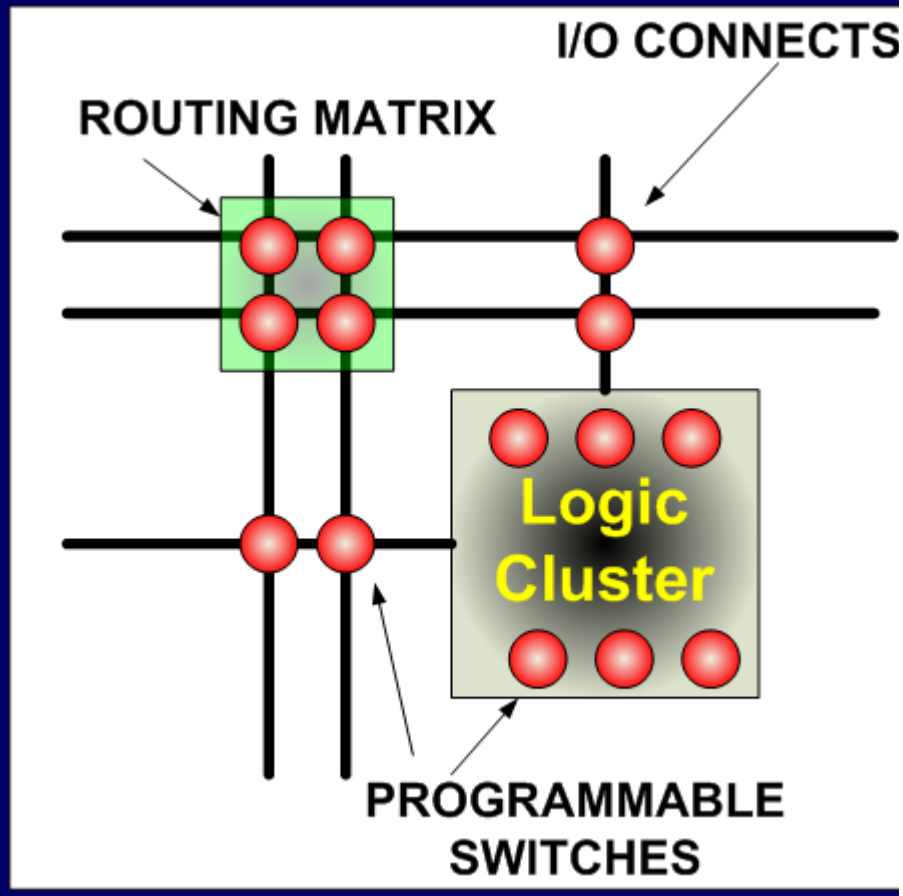
$$SR_{\text{fanout}} > 1 \quad and \quad SR_{\text{fanin}} > 1$$

- Should SR SEE data be applied to Error Rate Prediction of complex circuits

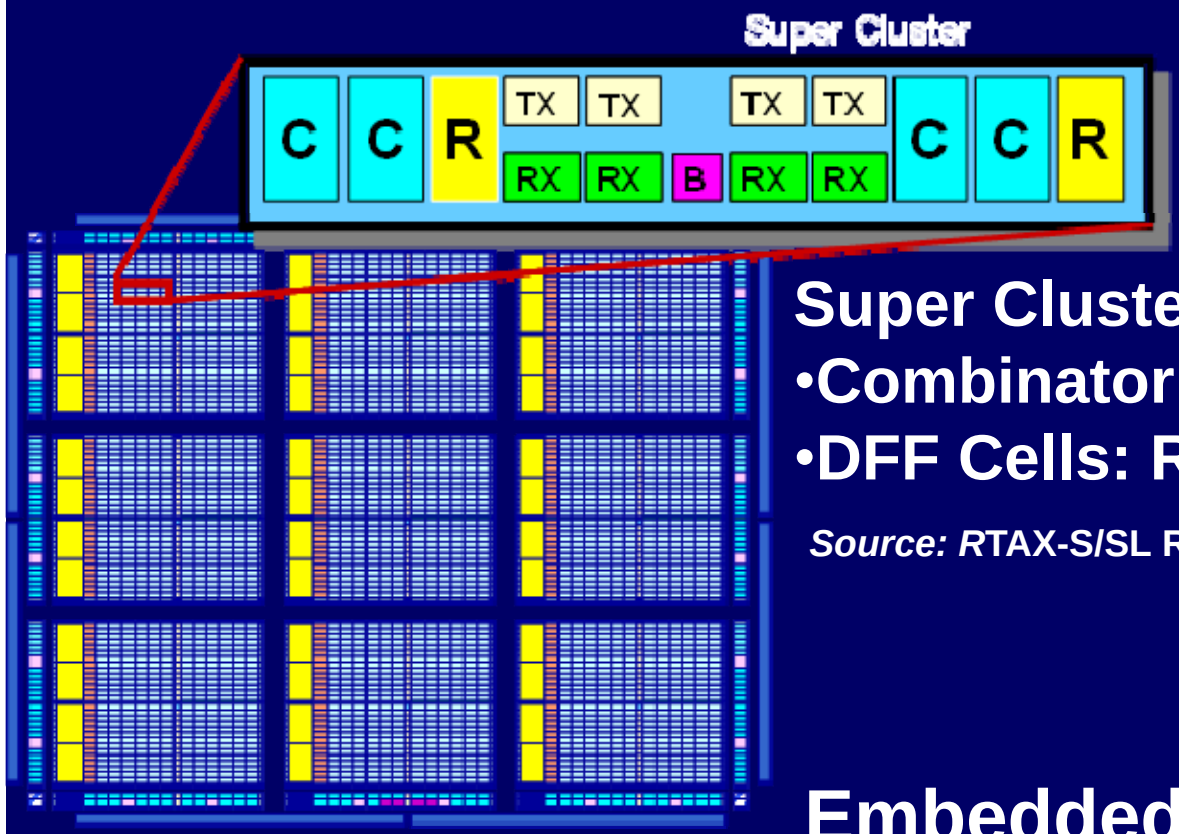
FPGA Basics

Configuration… Defines Connectivity and Functionality through Switches

- **Programming Switch Types:**
  - **Antifuse:** One time Programmable (OTP)
  - **SRAM:** Reprogrammable (RP)
  - **Flash:** Reprogrammable (RP)



ACTEL RTAX-S Architecture Basics



Super Cluster:

- **Combinatorial Cells: C CELLS**
- **DFF Cells: R Cells**

Source:* RTAX-S/SL RadTolerant FPGAs *2009 Actel.com

Embedded RHBD:

- Hardened Global Clocks and Resets
- Antifuse Configuration is SEU immune
- Embedded Localized TMR (LTMR) at each DFF (RCELL)

Actel RTAX-s SEE Susceptibility

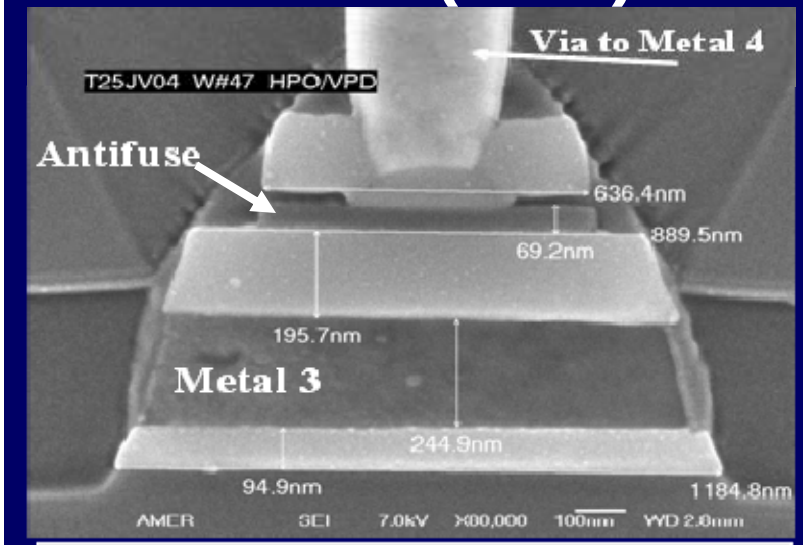
Contributing Factors Regarding FPGA Probability of Single Event Errors

- Pconfiguration: Configuration Upset rate
- P_{DFFSEU}: DFF upset rate
- $P_{SET \rightarrow SEU}$: SET capture rate
- P_{SEFI}: Error rate pertaining to Single Event Functional Interrupt (SEFI)

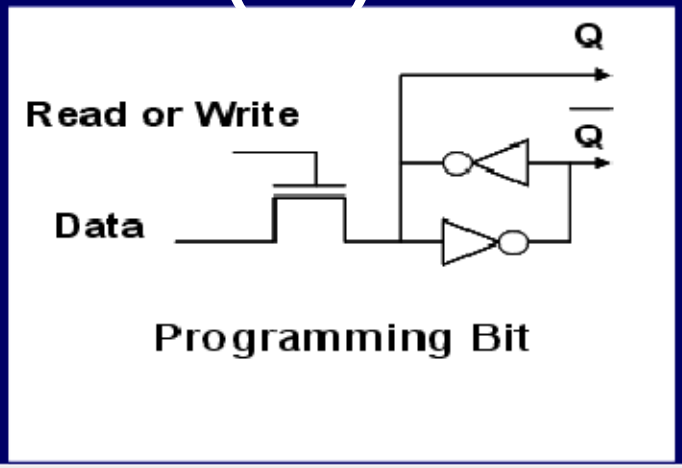
$$P(fs)_{error} \propto P_{Configuration} + P_{DFFSEU} + P(fs)_{SET \rightarrow SEU} + P_{SEFI}$$

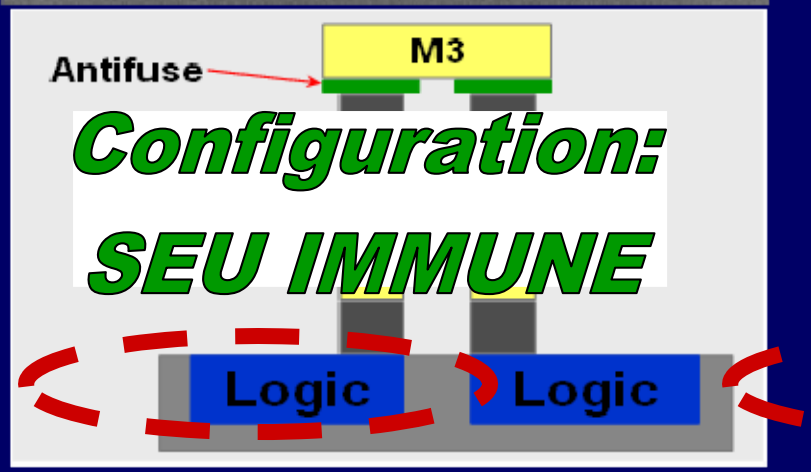
Programmable Switch Implementation and Single Event Upset (SEU) Susceptibility

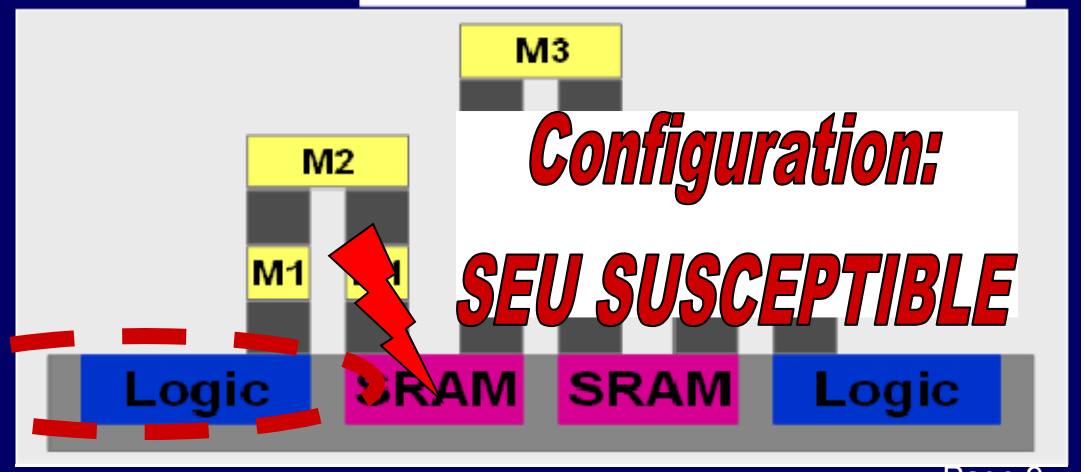
ANTIFUSE (OTP)



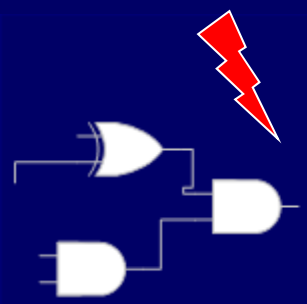
SRAM (RP)

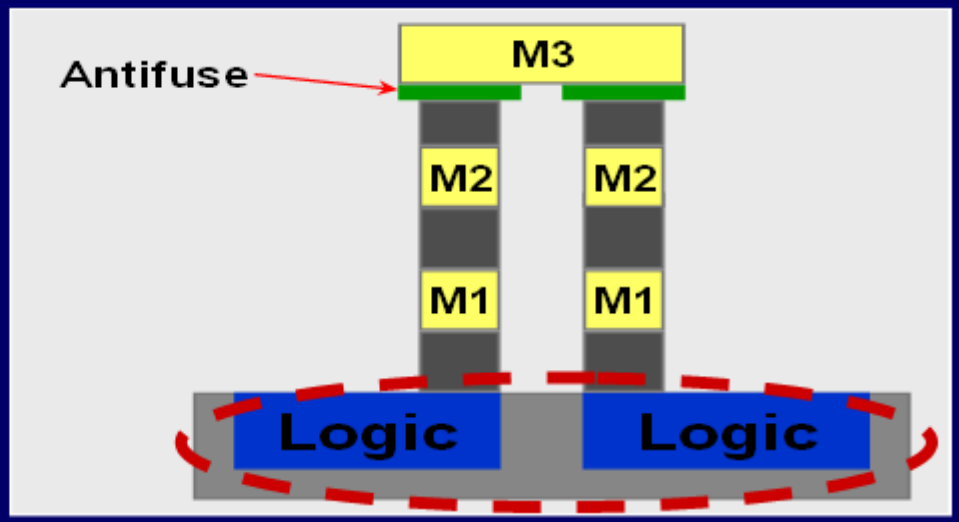


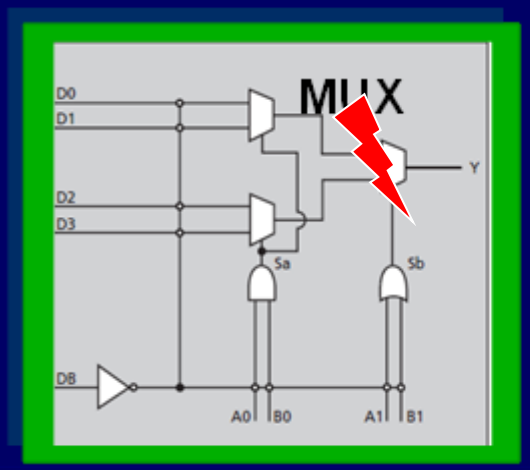




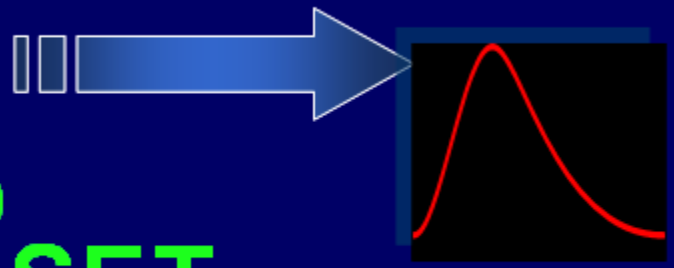
Combinatorial Logic Blocks (CCELLS) and Potential Upsets







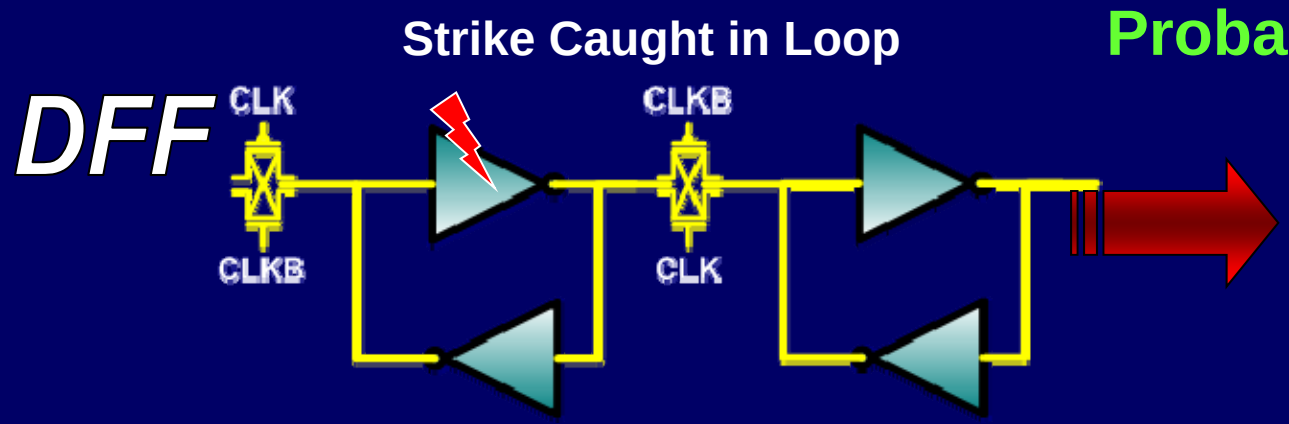
Glitch = Transient



P_{SET}

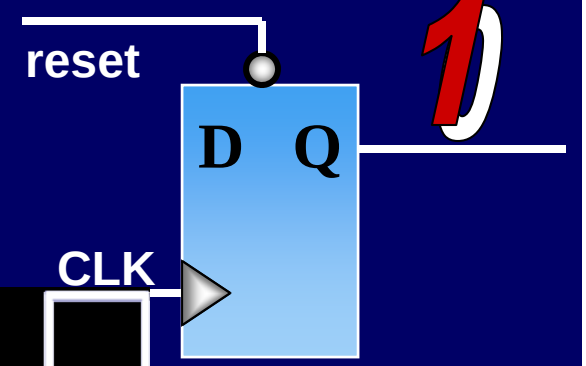
Probability of SET

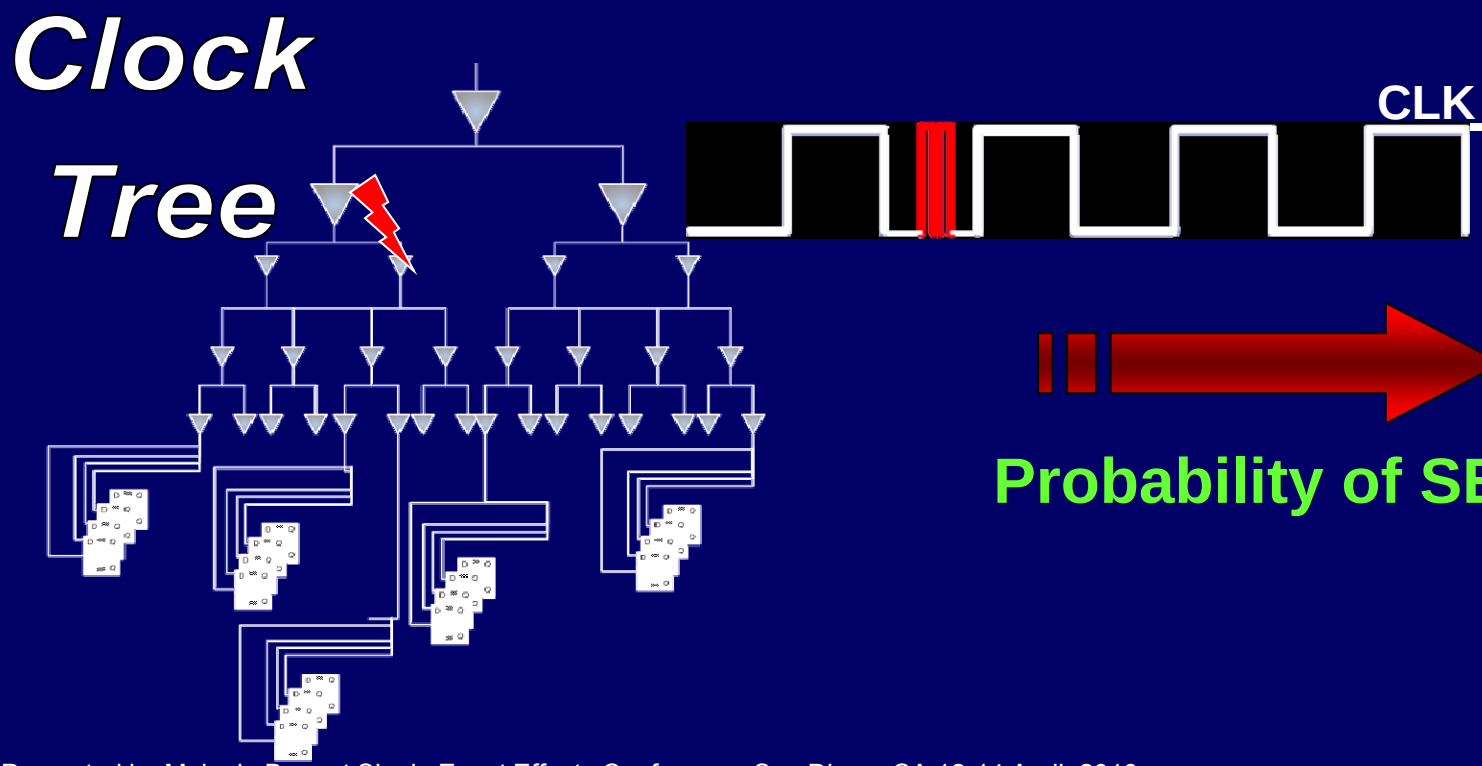
DFF's: SEUs and SEFIs



Probability of SEU

P_{DFFSEU}

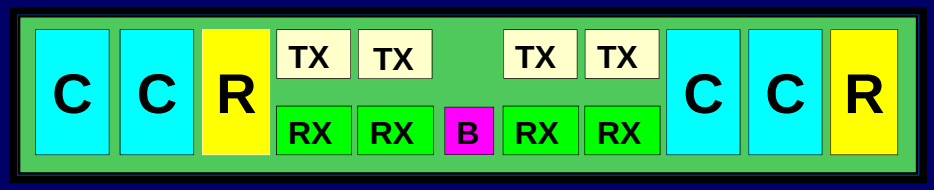




P_{SEFI}

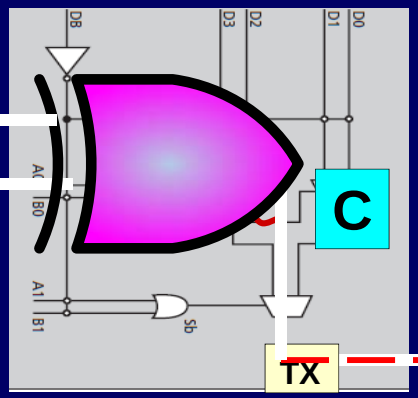
Probability of SEFI

ACTEL RTAX-S Embedded Mitigation… LTMR and SETs

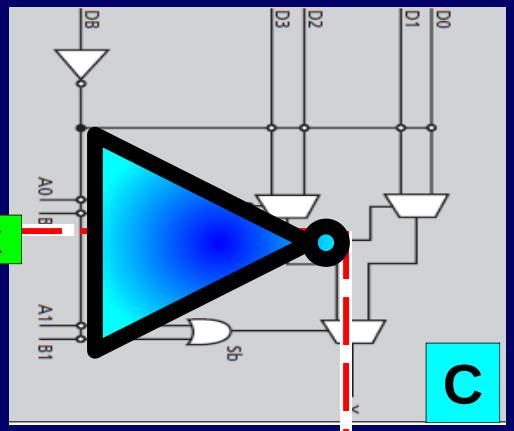


Super Cluster

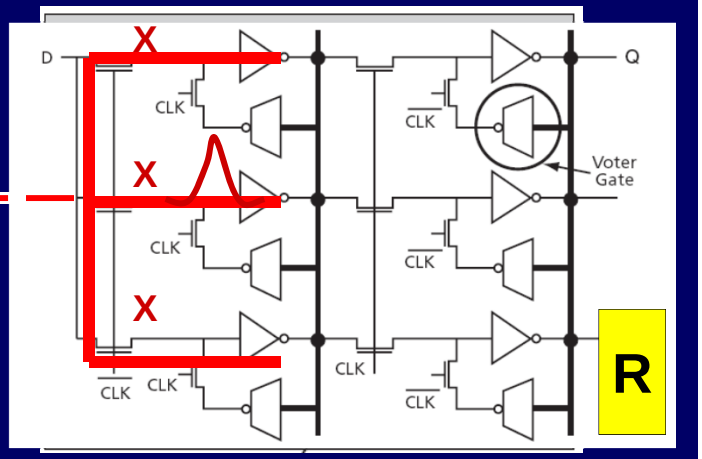
Combinatorial logic: C-CELL



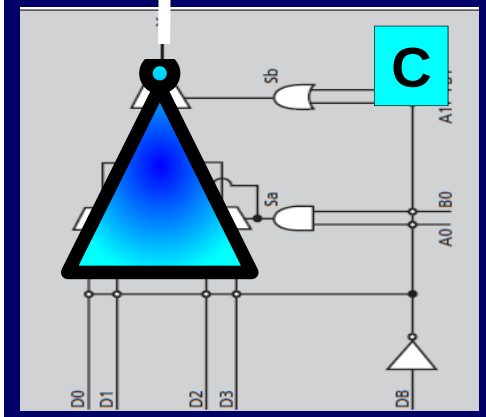
Combinatorial logic C-CELL



Sequential logic R-CELL



Combinatorial logic C-CELL

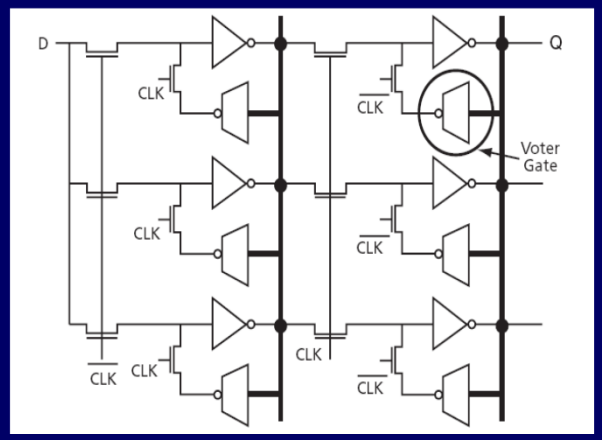


Embedded LTMR ERROR it caught In Library Cell

Presented by Melanie Berg at Single Event Effects Conference, San Diego, CA 12-14 April, 2010.

RTAX Example: Probability of Error Reduction

Antifuse Configuration + ***LTMR*** + ***Hardened Clocks***



$$P(fs)_{error} \propto P_{Configuration} + P_{DFFSEU} + P(fs)_{SET \rightarrow SEU} + P_{SEFI}$$

0 Low ~0

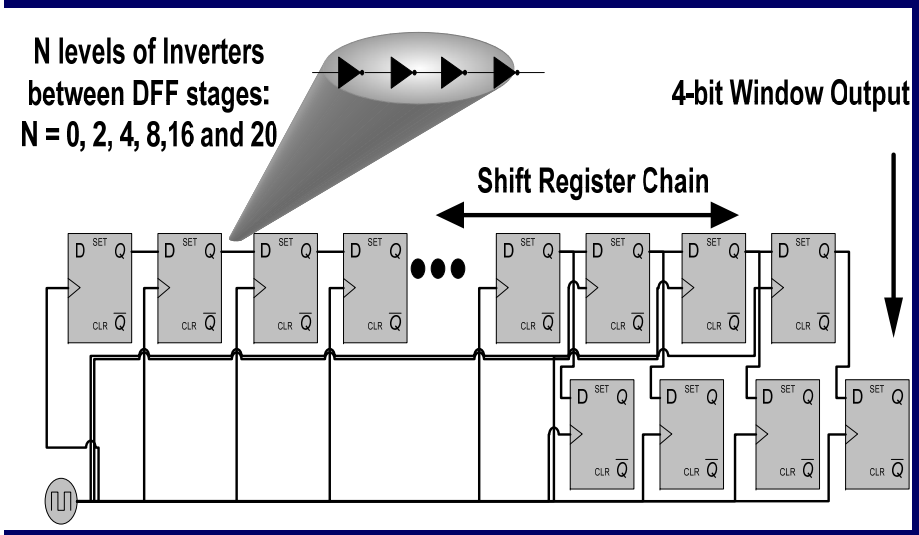
Error Rate must reflect frequency of operation

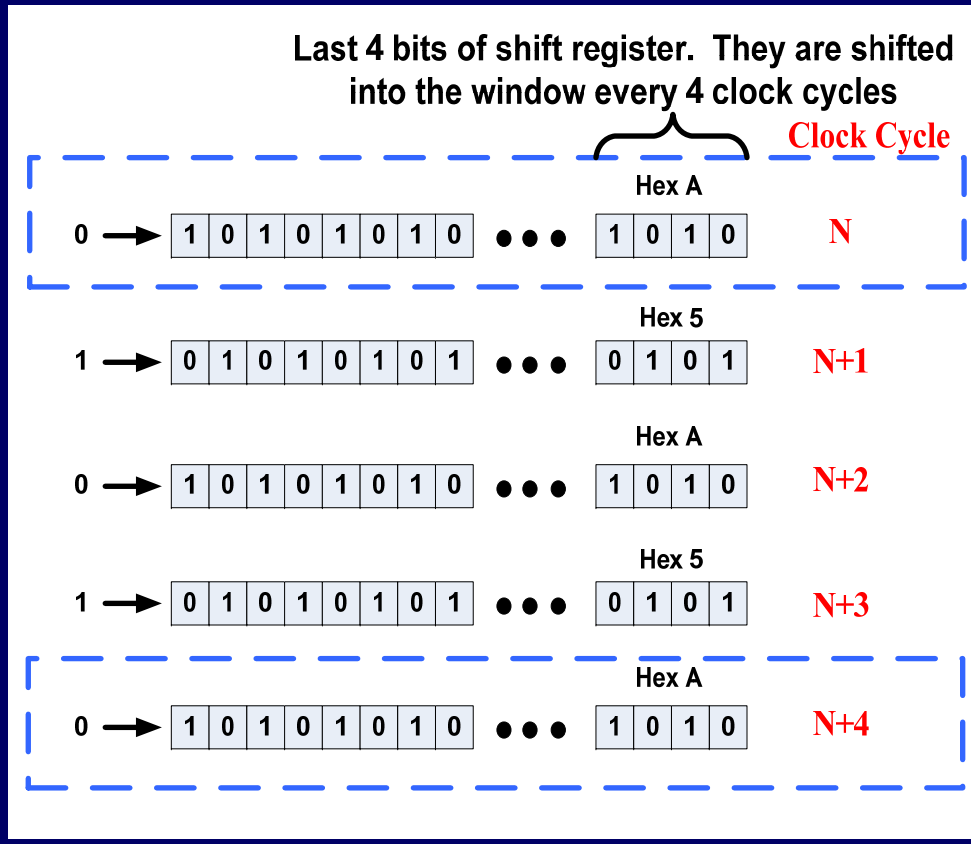
$$\frac{dE(fs)}{dt} < \frac{dE_{bit}(fs)}{dt} * (\#UsedDFFs)$$

SEE Test Methodology Development

Prior SR Testing

- Development of Windowed Shift Registers (WSRs)
- High Speed Internal Shift Register Operation
- Static output enhances signal integrity





REAG Windowed Shift Register String

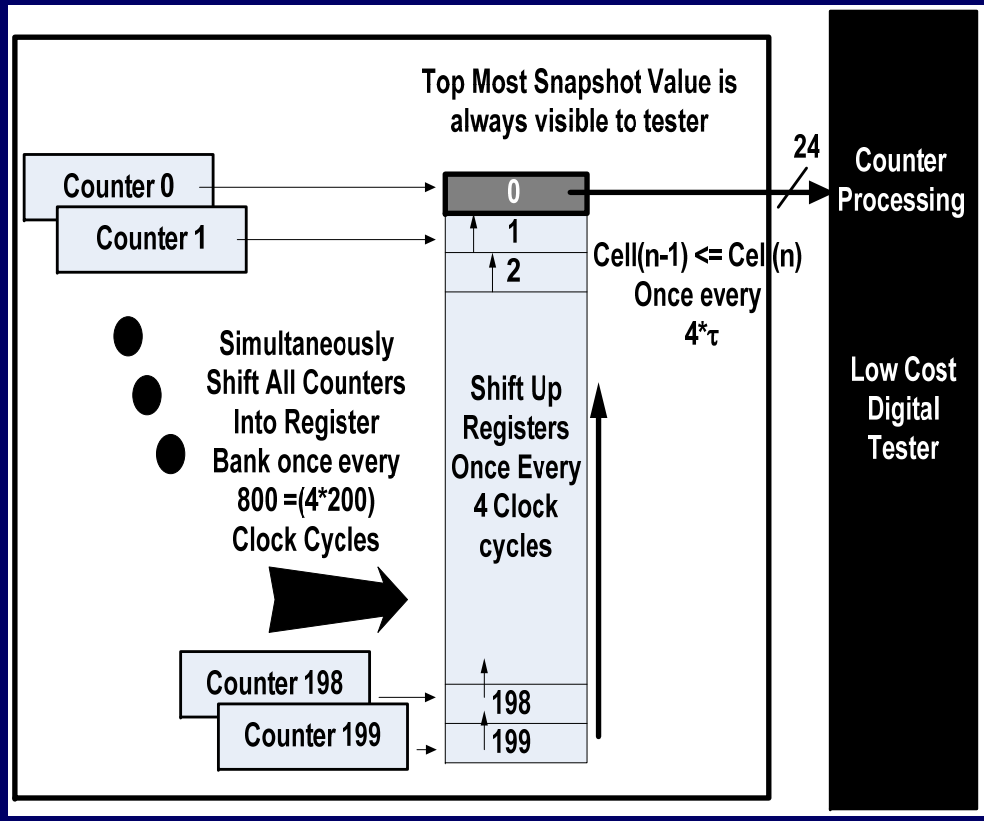
Prior WSR SEE Results

- Error rates are significantly dependent on Threshold LET(LET_{th})
- Choice of design impacted LET_{th}

	Low Frequency	Increased Frequency
LET_{th} MeV*cm^2/mg	LET_{th} >37	8< LET_{th} <30
Bit Error Rate (errors/bit-day)	$dE_{bit}/dt \approx 1x10^{-10}$	$1x10^{-10} < dE_{bit}/dt < 5x10^{-8}$

Development of Complex Architecture

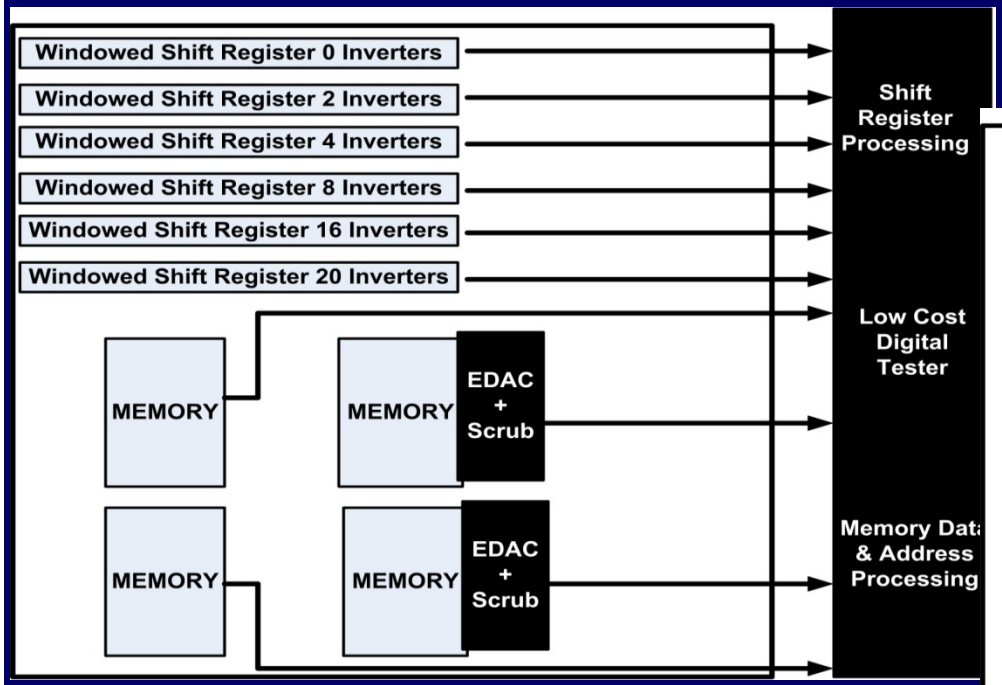
- It has the characteristics of a complex design with:
  - fan-out and fan-in > 1
  - contains a mixture of sequential and combinatorial logic.
- The circuit can be replicated to increase statistics.



- Its state space can be traversed within relatively short time periods such that all states are equally likely to be subject to particle strikes during radiation testing.

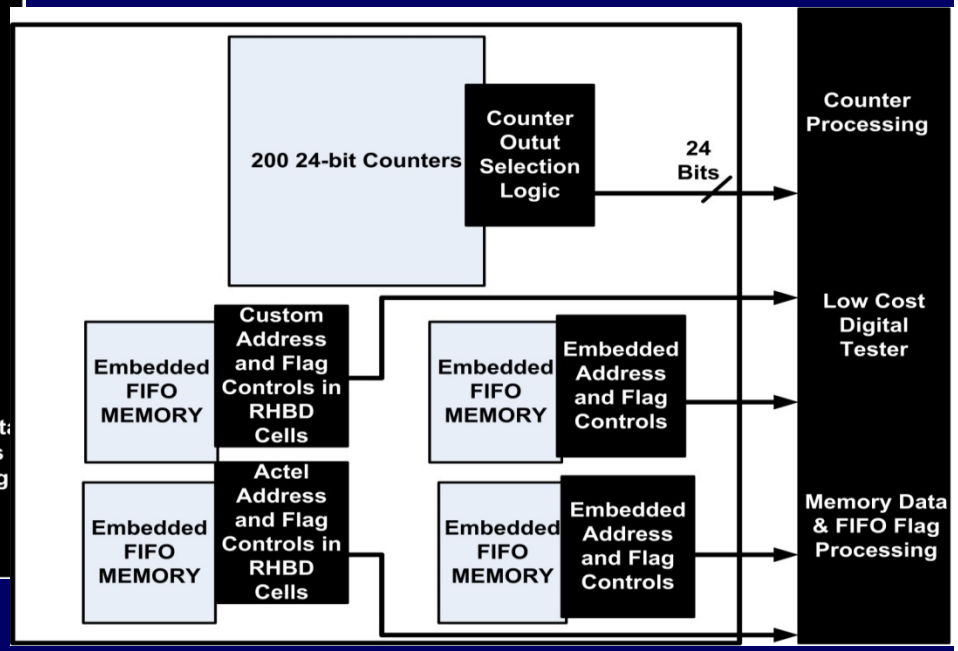
STATUS:
Actel RTAX-s

- RTAX-s Heavy Ion Testing December 2009
- RTAX-s preliminary test report delivered 02/2010



DUT1 : 4 memory structures and 6 various WSR strings

DUT2 : 4 FIFO memory structure and 200 counters in counter array



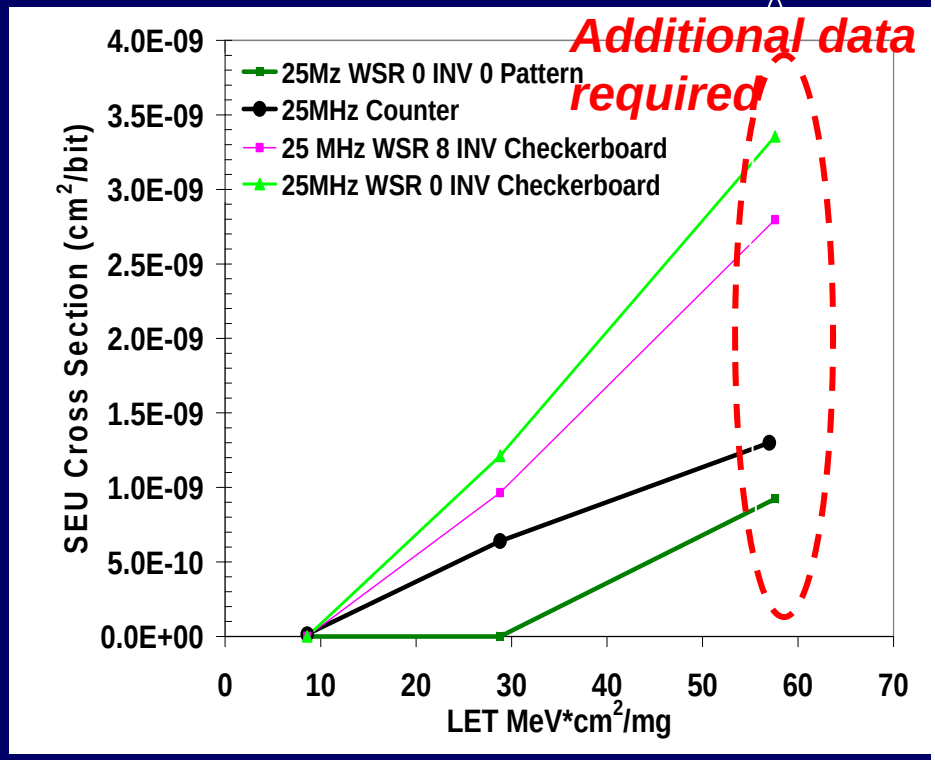
RTAX-s Design and Tester were successfully completed within 2 months

Highlights

Actel RTAXs : Counters versus WSRs

- 8 inverter (Inv) chains and 0 Inv chains are statistically equivalent at 25 MHz.
- However, as demonstrated 2004 data, there is a significant difference in cross sections at higher frequencies.
- 23 bit counter cross section is similar to checkerboard WSR:

  1<= #CCells between DFFs <8



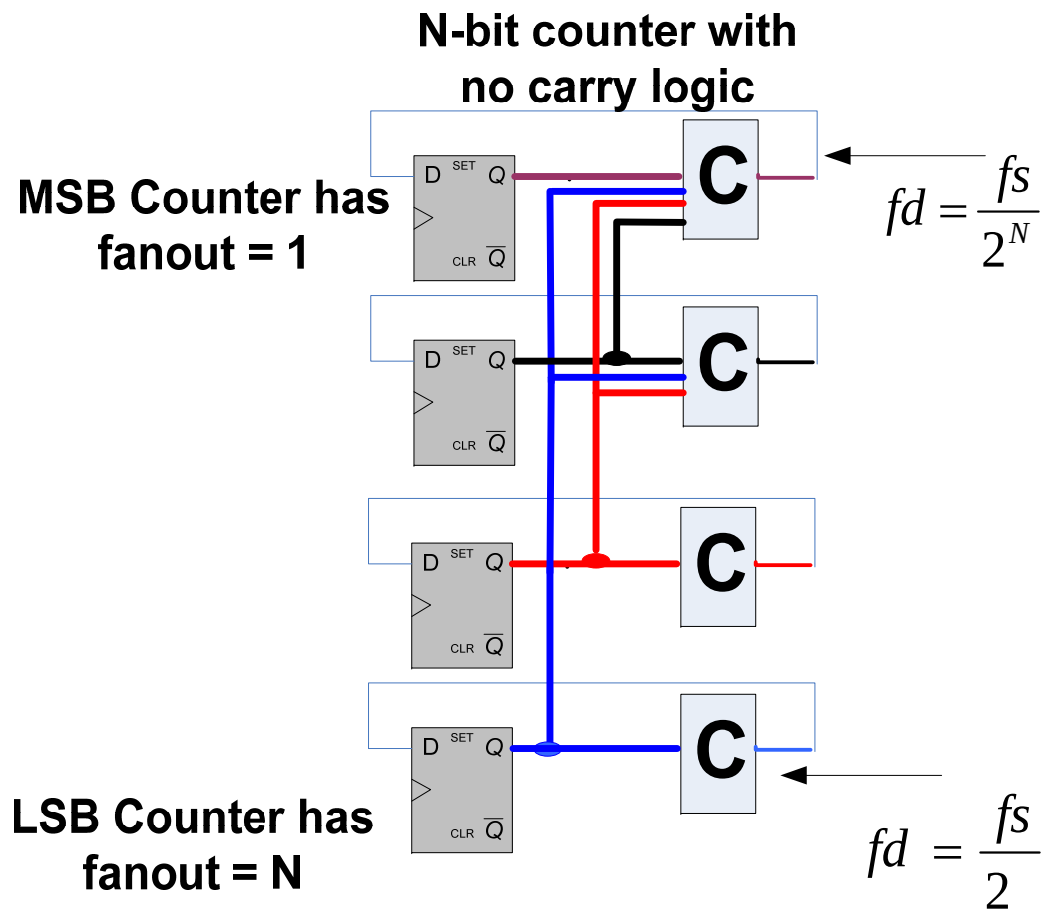
Data Pattern significantly affects threshold LET

Design/Data Pattern	8 Inv/ Checker	0 Inv/ Checker	0 Inv/ 0 pattern	Counter
LET_{th} MeV*cm²/mg	>8	>8	>30	>8

Presented by Melanie Berg at Single Event Effects Conference, San Diego, CA 12-14 April, 2010.

Highlights
Actel RTAXs: Counters and Capacitive Loading

- Each bit of the counter has different fanout
- Based off of WSR and Data pattern analysis, counter LSB should have the highest cross section
- It doesn't have the highest cross section … capacitive loading
- Data still under analysis



***fd*: data pattern frequency**
***fs* = system frequency**

Error Prediction of Complex Test Structures

- Must take into account:
  - System Frequency
  - Data Pattern
  - Levels of logic between DFFs
- Complex testing demonstrated that checkerboard WSR SEE data can provide a sufficient upper bound for complex circuits

Summary

- Error prediction for complex circuits must use SEE data that is applicable to the target design
  - Error rates have shown to differ by > 2 orders of magnitude
  - Designer will need to select SEE rates that apply
- SEE testing has evolved from simple SR testing to high-speed WSRs, and now counters
- It is best to use both WSR and counter architectures for SEE testing
- The advantage of testing counter circuits is the ability to reveal electrical effects:
  - Capacitive loading
  - SET propagation