Heavy Ion Testing with Iron at 1 GeV/amu

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Abstract—**A 1 GeV/amu ^{56}Fe ion beam allows for true 90° tilt irradiations of various microelectronic components and reveals relevant upset trends at the GCR flux energy peak. Three SRAMs and an SRAM-based FPGA evaluated at the NASA Space Radiation Effects Laboratory demonstrate that a 90° tilt irradiation yields a unique device response. These tilt angle effects need to be screened for, and if found, pursued with radiation transport simulations to quantify their impact on event rate calculations.**

***Index Terms*—SRAM, FPGA, galactic cosmic ray, heavy ion testing**

I. INTRODUCTION

ACCELERATED ground testing using heavy ions to study single-event effects (SEEs) in microelectronic components differs from the actual space environment in two critical ways: one, ground-based accelerator heavy ion fluxes are much larger, and two, ground-based accelerators cannot produce ions that cover the high-energy regime in space [2]. While these two issues do not prevent effective ground-based characterization of SEEs, they tend to limit experimental conditions, some of which are important for hardness assurance. This paper describes recent heavy ion single-event upset (SEU) experiments at the NASA Space Radiation Effects Laboratory (NSRL) at Brookhaven National Laboratory (BNL) using a 1 GeV/amu ^{56}Fe beam. This energy corresponds to silicon linear energy transfer (LET) of 1.2 (MeV·cm^2)/mg. The devices under consideration include static random access memories (SRAM) and a SRAM-based field programmable gate array (FPGA), all of which are sensitive to low LET upsets.

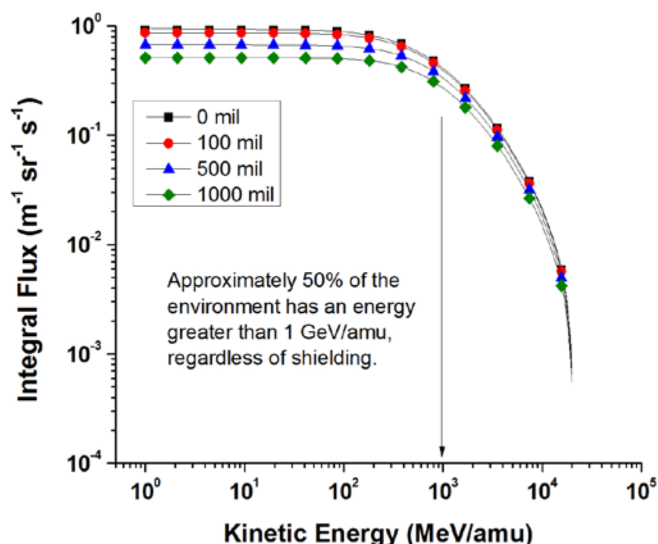

Fig. 1: Integral ^{56}Fe galactic cosmic ray fluxes behind different levels of solid spherical shielding. The levels are representative of a geostationary orbit at solar minimum. Note that half of the iron in the GCR environment has energies greater than 1 GeV/amu. These fluxes represent the model developed by R. A. Nymmik et al. [1].

Spacecraft must be designed to handle a number of different radiation environment hazards, including, but not limited to

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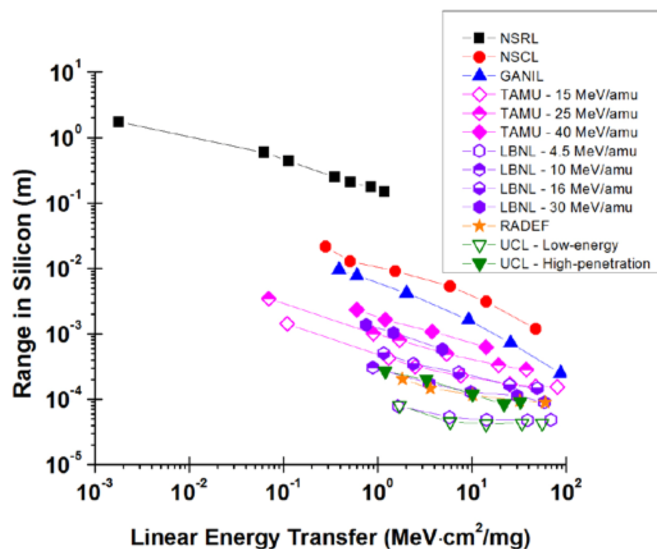

Fig. 2: Range *vs*. LET comparison for different heavy ion facilities commonly used for radiation testing. All of the NSRL beams are at 1 GeV/amu, NSCL ranges in energy from 0.15 to 0.08 GeV/amu, GANIL ranges in energy from 0.095 to 0.024 GeV/amu, and RADEF is at 0.0093 GeV/amu. Other energy tunes are given in the legend. Based on the space environment, the NSRL beams are most representative. ^{56}Fe is the rightmost data point on the NSRL series. Note that the beams shown are representative samples and not necessarily a complete list of the beams available at the facility.

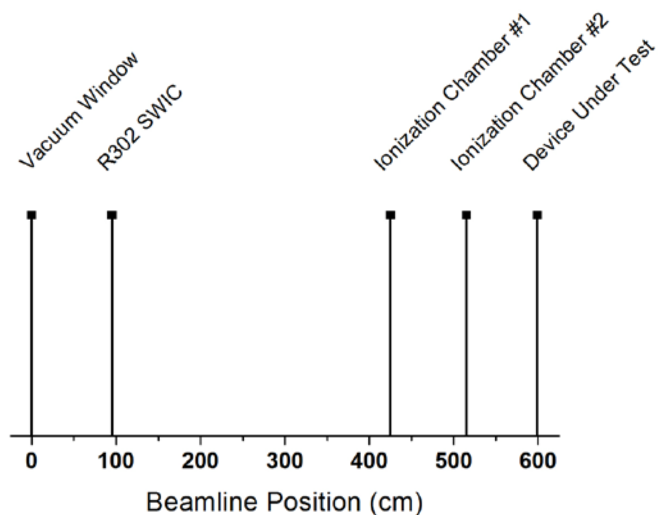

Fig. 3: This NSRL beamline diagram shows components' location upstream from the device under test. While more components can be in the beamline during setup, tuning, and initial characterization, we ran experiments with only two ionization chambers and one segmented wire ionization chamber (SWIC). Details of the material thicknesses and compositions are given in the text.

particle radiation, electromagnetic radiation, and orbital debris [3]. This work considers SEU hardness assurance for microelectronic components and thus focuses on the three categories of high-energy particle radiation in space. There are particles trapped in planetary magnetic fields, high fluxes of protons and heavy ions emitted from the sun during coronal mass ejections and solar flares, and a low flux, isotropic background of protons and heavy ions originating outside of the solar system called galactic cosmic rays (GCR); the GCR iron flux is shown in Fig. 1. It is the third category, GCR, which is relevant here.

GCR include all naturally occurring elements and have a flux energy peak of approximately 1.0 GeV/amu [1, 3-7]. GCR abundance is inversely proportional to the atomic number, Z, with the exception of iron, which accounts for a large amount of the total GCR flux beyond oxygen [3, 6]. These high-energy cosmic rays are very penetrating and have low LET values. However, as shown in Fig. 2, most ground-based facilities focus on lower energy, shorter range particles than those found in space. The larger range of LET values at ground-based facilities permits complete part characterization, but that does not necessarily correspond to abundance-based threats for highly-scaled microelectronics in space. Updates to the cyclotron cocktails at Texas A&M University (TAMU) and Lawrence Berkeley National Laboratory (LBNL) have extended the low-LET selection to provide more overlap with the higher energy facilities at the NSRL, the National Superconducting Cyclotron Laboratory (NSCL), and the Grand Accélérateur National d'Ions Lourds (GANIL). Université catholique de Louvain (UCL) and the RADiation Effects Facility (RADEF) at the University of Jyväskylä offer standard heavy ion cocktails.

$$\Omega = 2\pi(1 - \cos(\text{tilt angle})) \quad (1)$$

The maximum angle of irradiation in typical ground-based accelerator testing is governed by the device under test's (DUT) packaging and the range of the ion. While accelerated testing is often conducted at tilt angles between normal incidence and a maximum of perhaps 60-70°, half of the GCR flux is incident at angles greater than 60°. The solid angle of a cone, shown in Eq. 1, can be used to approximate a plane of sensitive devices. When the tilt angle is equal to 60°, $\Omega = \pi$, which is half the solid angle subtended by the surface of a hemisphere. This means that half of the particles in an isotropic environment are incident at angles less than 60° and the other half at angles greater than 60°.

Since a large number of heavy ions in the GCR spectrum are incident at grazing angles relative to the surface normal of the part, multiple-bit/cell upset (MBU/MCU) is a significant concern [8-10]. We define MBU as more than one upset bit in the same data word and MCU as physically-adjacent upset bits – clusters of size two or greater – that may or may not be in the same data word. If there is no knowledge of the physical chip layout, including intentional bit scrambling, observed multiple-bit errors must therefore be classified as MBUs. MBUs can be problematic because they could reduce or negate the effectiveness of error detection and correction codes (EDAC) [11] depending on the size of the event and capability of the EDAC implementation. If bit interleaving is used, MCUs are typically manifest as single-bit upsets (SBUs) in different data words since the interleaving would likely prevent errors within the same word assuming the interleaving

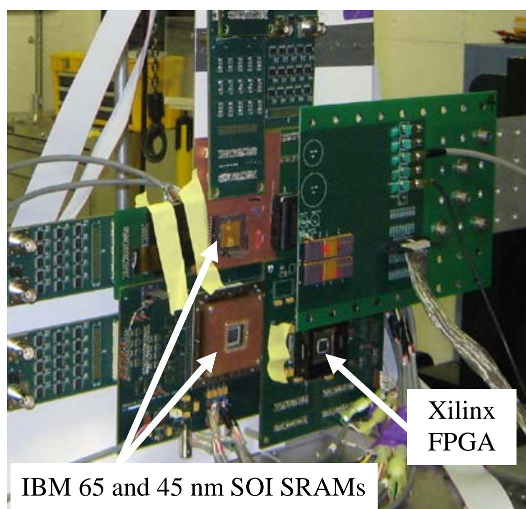

Fig. 4(a): Normal incidence test setup for the IBM and Xilinx parts. DUTs are clustered in center of 20 cm × 20 cm beam spot. Individual parts are marked. The beam vector is into the page.

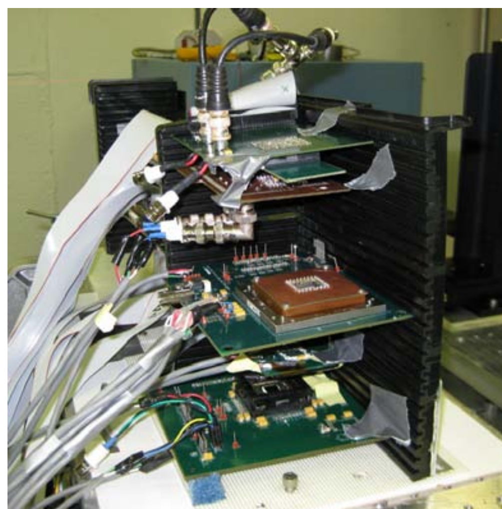

Fig. 4(b): 90° tilt, 0° roll test setup for the IBM, TI, and Xilinx parts. The 90° tilt, 90° roll setup is the same as this, but rotated counterclockwise around the vertical axis. The DUTs are, in order from top to bottom: IBM 65 nm SOI, IBM 45 nm SOI, TI 65 nm bulk CMOS, and Xilinx XC4VLX25. The beam vector is right-to-left.

spans a sufficient physical distance. With no bit interleaving, every MCU would be a MBU. However, with bit interleaving and because events in space occur discretely in time, single MCUs do not often cross enough of the physical memory fabric to appear in the same data word.

MBU hardness assurance concerns are further complicated by the fact that modern, highly-scaled process technologies (≤ 100 nm) are more sensitive to MBU [12-16]. Particularly for technologies below 90 nm, this is the result of packing the sensitive nodes closer together and not necessarily an increase in the upset sensitivity [17]. In several cases demonstrated to date, the upset thresholds of these technologies are low enough to be affected by direct ionization from incident protons [17-20]. Since we have knowledge of the physical layout of the SRAMs, multiple-bit upsets are interpreted as MCUs.

II. Experimental Facility & Setup

The NSRL at BNL is a joint effort by the NASA Johnson Space Flight Center and the Department of Energy's Office of Science designed to study radiobiological effects relevant to human spaceflight. In addition to radiobiological studies, the NSRL also hosts physics experiments such as this work. Currently, heavy ions are accelerated using one of the two BNL Tandem van de Graaff accelerators and sent down a 700 m beamline to the Booster synchrotron. The beams are accelerated further in the Booster and then delivered to the NSRL. Because the Tandems serve as the ion source, the number of beams available at the NSRL is presently limited to hydrogen, carbon, oxygen, silicon, chlorine, titanium, and iron. However, with the commissioning of the electron beam ion source, predicted to be sometime in 2010, all ions from hydrogen to uranium will be available and at much higher fluxes.

The NSRL 1 GeV/amu particle beams are compared to several other common facilities' beam selections in Fig. 2. The NSRL beams favor low LETs and substantial ranges, just like the actual space environment. As mentioned earlier, TAMU and LBNL have added more high-energy, light ion beams creating more LET commonality with the NSRL. However, the substantial energy increase at the NSRL translates to a 160x difference in range for most overlapping LETs not at the high-energy facilities. It is becoming necessary to use these lower LET beams when searching for SEE onset due to increasing technology sensitivity [17] and the corresponding impact on SEE rate calculations.

The beam itself is well-controlled and focused by two sets of magnetic lenses that can produce a "square" beam spot of up to 20 cm × 20 cm with a uniformity of ±2%. The staple energy tune at the NSRL is 1 GeV/amu, though the energy can be changed quickly if the operators are given adequate notice of the required tunes. The energy range is approximately 0.1 GeV/amu to 1 GeV/amu, which is the energy at the DUT, not the extraction energy of the Booster synchrotron. At lower energies the beam is less uniform, with a small dip in intensity at the center of the beam spot. The ions are delivered to the target room in 300 ms spills approximately every 3.7 s. Real-time dosimetry is achieved with a calibration ion chamber (a.k.a. EGG counter) manufactured by Far West Technologies in conjunction with larger secondary ion chambers, shown in Fig. 3. The secondary ion chambers are used to measure integrated dose and cut the beam off when a specific dose has been reached. The dosimetry unit is rad(H_2O) and must be converted to rad(Si) and then scaled by the LET of the incident beam in order to calculate the particle fluence.

In order to take advantage of the generous beam spot, jigs were made to hold four separate, coplanar DUTs – three SRAMs and one SRAM-based FPGA. Irradiations that took place at normal incidence have the DUTs' surface normal parallel with the beam vector, making the DUTs' surface the *xy*-plane. The coordinate system for experiments at angle is

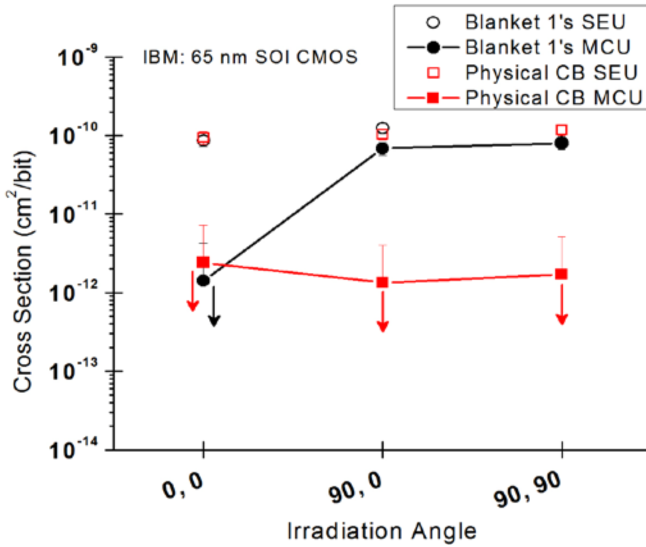

Fig. 5(a): IBM 65 nm SOI cross sections showing SEU and MCU (physically-adjacent) for both blanket 1's and physical checkerboard patterns. Two-sided error bars, shown if larger than the data point, are 1σ Poisson errors. One-sided error bars are 1σ Poisson upper limits for measured limiting cross sections – a downward arrow emphasizes this.

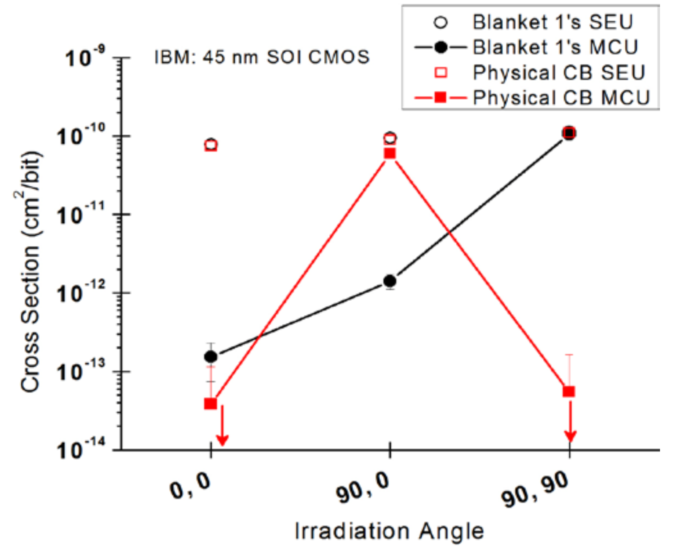

Fig. 5(b): IBM 45 nm SOI cross sections showing SEU and MCU (physically-adjacent) for both blanket 1's and physical checkerboard patterns. Two-sided error bars, shown if larger than the data point, are 1σ Poisson errors. One-sided error bars are 1σ Poisson upper limits for measured limiting cross sections – a downward arrow emphasizes this.

described by the tilt and roll angles relative to the normal incidence setup. (90° tilt, 0° roll) requires a 90° rotation about the *x*- or *y*-axis. (90° tilt, 90° roll) first requires a 90° rotation about the *z*-axis, swiveling the DUT perpendicular to the beam, followed by a 90° rotation about the *x*- or *y*-axis. The latter two tilted conditions can be viewed as irradiating the DUT through one edge and then the other. In terms of spherical coordinates, tilt is a displacement in the polar angle and roll is a displacement in the azimuthal angle θ. Sample images of some of the experimental setups are shown in Figs. 4(a) and 4(b).

While there is a lot of material in the beamline, as shown in Fig. 3, by far the biggest contributor to energy loss is the nearly 6 m of air gas. Nevertheless, these components, along with the calibrated EGG counter, enable real-time dosimetry to 10% or better. The conversion from absorbed dose to fluence relies on the accuracy of the particle LET as it transits the ionization chamber(s) as well as the assumption that it does not change by the time it impacts the sensitive volume(s) in the device under test (DUT). Since the beam is high-energy and the relevant dosimeter is close by, this assumption does not carry with it too much error. The near-perfect uniformity of the beam at 1 GeV/amu helps reduce systematic errors.

III. Experimental Results

A. *Static Random Access Memories*

Three SRAMs from two vendors, IBM and Texas Instruments (TI), were exposed to the iron beam at the NSRL. Of the three, two are 65 nm (one IBM and one TI) and one is 45 nm (IBM). The IBM 65 nm [18, 19] and 45 nm [17] SRAMs are silicon-on-insulator (SOI); the TI 65 nm [10, 20, 21] part is a bulk complementary metal oxide semiconductor (CMOS) part. The IBM 65 nm SOI SRAM is 1 Mbit and their 45 nm SOI SRAM is 36 Mbit. The TI bulk CMOS SRAM is 8 Mbit. We tested all three SRAMs under static conditions. The test software writes a specific data pattern to the DUT, the DUT is irradiated, and then the contents of the memory are read back. This is different than either continuous read (errors can accumulate) or read-modify-write (continuous scrubbing) testing, both of which are dynamic methods.

$$\sigma_{\mathrm{SEU}} = \sum_{i=1}^{\infty} \frac{i \times \mathrm{Event}_{ith\ bit}}{\Phi} \tag{2}$$

$$\sigma_{\mathrm{MCU}} = \sum_{i=2}^{\infty} \frac{\mathrm{Event}_{ith\ bit}}{\Phi} \tag{3}$$

The SEU and MCU cross sections for the IBM 65 and 45 nm SOI SRAMs are shown in Figs. 5(a) and 5(b). Two data patterns were written to the memory – blanket 1's and a physical checkerboard. The equations for the uncorrelated SEU and the correlated MCU cross sections are given by Eqs. 2 and 3 [10]. The SEU cross section is the total number of single-bit errors plus the multiplicity-corrected number of multi-bit errors divided by the uncorrected fluence. Since effective LET and effective fluence are either undefined or zero at a tilt angle of 90°, the standard right rectangular parallelepiped cosine corrections have been omitted. The MCU cross section is the number of MCU events involving two or more physically-adjacent bits divided by the uncorrected fluence. Both the 65 and 45 nm SRAMs were irradiated at normal incidence, a tilt of 90° and roll of 0°, and at a tilt of 90° and a roll of 90°. All three of these irradiations were conducted with the 1 GeV/amu ^{56}Fe beam.

The MCU pattern and orientation dependence in the IBM components is a result of the SRAM cell construction and the location of off-state transistors in proximity [14, 17]. The location of these off-state transistors can change depending on

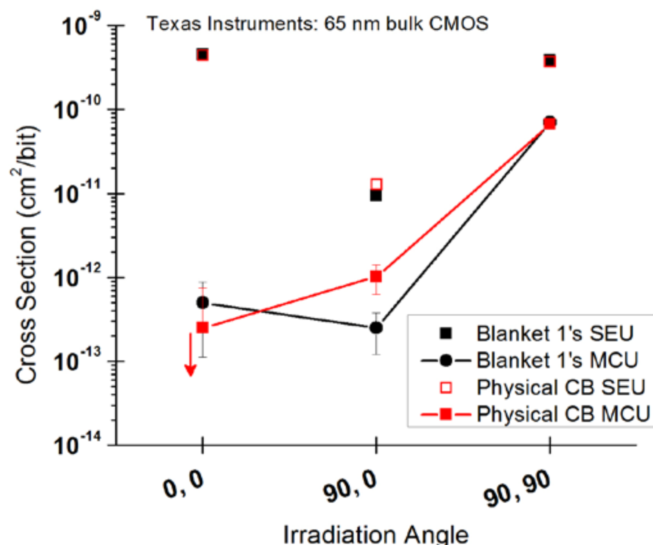

Fig. 6: TI 65 nm bulk CMOS cross sections showing SEU and MCU (physically-adjacent) for both blanket 1's and physical checkerboard patterns. Two-sided error bars, shown if larger than the data point, are 1σ Poisson errors. One-sided error bars are 1σ Poisson upper limits for measured limiting cross sections – a downward arrow emphasizes this.

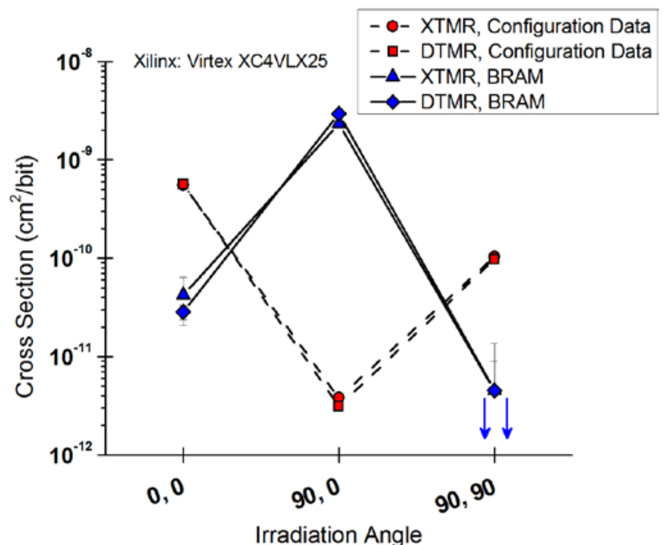

Fig. 7: Xilinx XC4VLX25 bulk CMOS SEU cross sections for two different redundancy schemes. The configuration and BRAM cross sections are shown separately. Two-sided error bars, shown if larger than the data point, are 1σ Poisson errors. One-sided error bars are 1σ Poisson upper limits for measured limiting cross sections – a downward arrow emphasizes this.

the data pattern, shown in Fig. 5(b), or stay the same, as shown in Fig. 5(a).

The TI SEU and MCU cross sections are shown in Fig. 6. We exposed the 8 Mbit bulk CMOS SRAM with the 1 GeV/amu ^{56}Fe beam at normal incidence and the other two orientations – (90° tilt, 0° roll) and (90° tilt, 90° roll). Two data patterns were written to the memory – blanket 1's and a physical checkerboard. There is no significant difference in SEU and MCU response for these two patterns unlike the IBM 65 nm SOI SRAM. The data in Fig. 6 show a definite cross section dependence on grazing orientation with (90° tilt, 90° roll) being the most sensitive for MCUs. At this orientation both the SEU and MBU cross sections are larger than at the orthogonal roll angle with the same tilt. This indicates that the physical layout is responsible for the elevation in upset cross section [10, 21]. The data and conclusions published in [10, 21] demonstrated conclusively that the n-well orientation affected the SEE cross section. The work of Tipton [10], Hutson [21], and Sierawski [20] provides insight regarding the layout of the TI 65 nm SRAM cell. Orienting the part such that the ion trajectory is parallel to the long dimension of the n-well is what causes the increase in cross section. Physically adjacent MCUs as large as ten bits were observed at this orientation, though this number is uncertain due to unavoidable false-positive MCUs. More information on MCU cluster sizes with conventional heavy ion testing with this part is available in [10].

B. *Field Programmable Gate Array*

A 90 nm bulk CMOS, SRAM-based FPGA from Xilinx (XC4VLX25) [22-24] was exposed to the same beam as the IBM and TI SRAMs – 1 GeV/amu ^{56}Fe at normal incidence as well as (90° tilt, 0° roll) and (90° tilt, 90° roll). The results are shown in Fig. 7. A biased DUT was placed in the beam and the clocks were held static. The DUT underwent read back following exposure, recording the full contents of the configuration memory, which includes the logic configuration and block RAM (BRAM). The number of bits in error were calculated and then separated into configuration data and BRAM. This process was completed for two different, redundant FPGA designs – XTMR and DTMR [23, 25]. The cross section for each of these designs' configuration data and BRAM were calculated separately and are reported in Fig. 7.

C. *False Positives in Static Upset Data*

As mentioned in Sections III.A and III.B, we conducted all tests under static conditions due to long cable runs that resulted in loss of high-speed data integrity. This was required because the FPGA motherboards could not be kept in the beam during tests. Because the runs were static, errors accumulated in the memories before being read back at the end of the run.

Assuming that a memory is not scrubbed during testing, there is a finite probability that an upset bit will have one of its nearest neighbors upset before the memory can be read back and scrubbed for the next exposure. Nearby SBUs from independent events cannot be distinguished from MCUs caused by a single impinging particle; this is a false positive MCU. Therefore, tests should be conducted such that the probability of independent SBUs happening in close proximity (*i.e.*, physically-adjacent) is low. However, when testing four components with different sensitivities at the same time, as we did at the NSRL, this condition can be hard to meet.

$$P_{\text{MBU per test}} = \frac{N_{\text{pairs}} \cdot N_{\text{errors}} \cdot (N_{\text{errors}} - 1)}{2N_{\text{A}}} \tag{4}$$

E. H. Cannon *et al.* [14] presented an approximate formula for calculating the probability of false positive MCUs given a number of neighboring pairs. Just considering the vertically and horizontally adjacent cells, there are four pairs and the

probability is given by Eq. 4. N_{pairs} is the number of pairs a specific distance from the central hit cell, N_{errors} is the number of errors in the run, and N_A is the number of cells in the whole array.

Table I: Maximum (approximate) number of errors in each SRAM array for a 0.1 probability of one false positive MCU for two different numbers of neighboring pairs

N_{pairs}	IBM 65 nm SOI	IBM 45 nm SOI	TI 65 nm bulk CMOS
4	224	1285	632
8	159	909	448

Given Eq. 4 and the size of the three SRAMs, to keep the false positive probability below 0.10, the maximum number of uncorrelated errors allowed in each array is given in Table I. These numbers hold as long as the number of errors in the memory at any one time is much less than the size of array. This information says that the number of errors we can accumulate at any one time to avoid excessive false positives is driven by the IBM 65 nm SOI SRAM since it only has a 1 Mbit array. These conditions were maintained for all SRAMs with the exception of the TI SRAM in the 90° tilt, 90° roll orientation, where the total number of errors per exposure was between 800 and 1000. Note that the IBM 45 nm SOI SRAM only had 33 of 36 Mbit active.

These calculations and numbers break down when the probability of hitting any given memory cell is not equal, which is exactly the situation that occurs when the DUTs are tilted to 90°. The cells at the edge of the chip where the beam first penetrates have a higher probability of getting struck than cells in the middle or on the backside of the chip assuming the beam is perfectly collimated and scatters after hitting the chip. However, the reality is that the beam is not perfectly collimated. Regardless, the probability of false positives increases at 90° tilt, but this increase is not considered significant enough to skew the observed results.

IV. Discussion

The SRAM results are consistent with the fundamental differences between bulk CMOS and SOI technologies. The bulk technology has a thicker sensitive volume with many devices residing in the same n- and p-wells, making a large number of bits simultaneously susceptible to upset. This feature, while increasing the probability of high-multiplicity MCUs, also removes data pattern sensitivity since charge transport within the p- and n-wells means that it is unnecessary for the incident ion to physically strike the necessary nodes to cause a cell state change; Fig. 6 shows this.

The SOI SRAM data, shown in Figs. 5(a) and 5(b), have a definite pattern dependence in addition to the orientation sensitivity observed with the bulk CMOS SRAM, which is apparent in Fig. 6. Since each SOI SRAM cell, and indeed some individual transistors within the SRAM cell, are isolated by oxide, the charge transport relevant in the bulk SRAM technology no longer applies. MCU in an SOI SRAM requires that the incident ion, or daughter particles in the case of indirect ionization, strike all the cells necessary to cause upset; charge transport plays a limited role.

In the SRAM arrays in these tests, as with most SRAMs, the off-state n-channel transistors, or NFETs, drive the cell sensitivity. The SBU and MCU sensitivity of the TI 65 nm bulk CMOS array has been described at length by A. D. Tipton *et al.* [10], so it will not be covered again in detail with the exception of what has already been mentioned. The IBM 65 and 45 nm SOI SRAMs, on the other hand, present an interesting comparison because the designs, while similar, end up with the off-state NFETs in different locations for the blanket 1's and physical checkerboard patterns [17].

In the IBM 65 nm SOI SRAM, the blanket 1's pattern is always more sensitive to MCUs than the physical checkerboard. This is because the off-state NFETs of a 2x2 cell array are all together in the center. These off-state NFETs are offset and in opposite corners for the physical checkerboard, removing the geometric alignment. Regardless of whether the ions are incident on the 2x2 array from top-to-bottom/bottom-to-top or left-to-right/right-to-left there are always two off-state NFETs in alignment for the blanket 1's pattern; this is not true for the physical checkerboard. The 90° roll, 90° tilt configuration is slightly more sensitive to blanket 1 MCUs than the 0° roll, 90° tilt configuration because in the former case both vertical pairs of NFETs share a diffusion rather than separation by oxide, similar to patterns and layouts shown in Fig. 7 of [17].

The IBM 45 nm SOI SRAM shares some of the characteristics of the 65 nm SOI SRAM, with one critical difference. At 90° tilt, 0° roll the physical checkerboard results in alignment of off-state NFETs – this same alignment is not present for the blanket 1's pattern. The diagram that shows this is in Fig. 7 of [17]. Testing at full 90° tilt confirms the conclusions drawn by D. F. Heidel *et al.* [17] based on much smaller tilt angles, which is encouraging for conventional heavy ion testing techniques.

The FPGA data shown in Fig. 7 exhibit similar behavior to the SRAM data presented in Figs. 5(a), 5(b), and 6, partly because the FPGA is SRAM-based, though the functionality of the two device types is very different. It is interesting to note that the configuration data and BRAM have opposing trends at (90° tilt, 0° roll) and (90° tilt, 90° roll), yielding information about the orientation of internal data storage. For further information on this FPGA, see [23].

While we focused this work on experimental results, these data provide a strong argument for the use of radiation transport simulations to extend standard heavy ion testing and evaluation to more realistic on-orbit environments. Simulations not only provide suitable space environments, they also yield far more granularity in their solutions. These details are useful for uncovering SEE mechanisms and making design decisions that impact system-level hardness assurance. For instance, a radiation transport and upset model could be calibrated at modest angles and energies and then the simulations could be extrapolated to the conditions described in this paper. Assuming the input physics are correct, one would expect the transport simulations to reproduce both qualitatively and quantitatively correct results.

V. CONCLUSION

This is the first time the NSRL facility has been used to irradiate highly-scaled commercial CMOS and SOI technologies. The 1 GeV/amu ^{56}Fe beam allowed true 90° grazing angle irradiation of SRAM and FPGA parts without special die or package preparation. These experiments at the NSRL facility represent the current state-of-the-art for high-energy, accelerated ground testing and allow for upset characterization with a realistic GCR heavy ion beam.

While it would be ideal to be able to execute these kind of experiments on a regular basis, experimental logistics and cost are significant barriers. Fortunately for most parts, this kind of testing is unnecessary for reasonably accurate rate calculations. Standard laboratory tilt angles should reveal the limiting case trends shown in Figs. 5(a), 5(b), 6, and 7. However, these data also underscore the fact that data pattern and roll angle can and do play a significant role in upset cross section and thus are relevant concerns for single-event hardness assurance and must be investigated.

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