Single Event Upset (SEU) Analysis of Complex Circuits Implemented in Actel RTAX-S Field Programmable Gate Array (FPGA) Devices

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Motivation

• The SEU cross section Linear Energy Transfer threshold ($\text{LET}_{\text{th}}$) is a significant factor that drives device bit error rates
• The ability to uncover $\text{LET}_{\text{th}}$ has proven to be a challenging task for FPGA devices
• Traditional SEU FPGA Testing has been limited:
  – Shift Registers: Simple, linear Data Paths
  – Complex circuits: Restricted State Space Traversal during irradiation
  – Inability to observe all digital upsets due to tester limitations
• Presentation will discuss –
  – Actel Anti-fuse FPGA (RTAXs) susceptibility
    • Flip Flop (DFF) Single Event Upsets (SEUs) $\rightarrow P_{\text{DFFSEU}}$
    • Single Event Transient (SET) Capture ($P_{\text{SET} \rightarrow \text{SEU}}$)
  – Traditional testing methodologies and results
  – Evolution of testing techniques and results

Actel RTAXs Susceptibility and Embedded Mitigation

Design Specific SEE upset rate

Configuration SEE upset rate

Functional logic SEE upset rate

Single Event functional Interrupt

CCELLs: Combinatorial logic cells

Local Triple Modular Redundant (LTMR) DFFs lower $P_{\text{DFFSEU}}$ but cannot mitigate $P(fs)_{\text{SET} \rightarrow \text{SEU}}$

RCELLs: DFF + Combinatorial

A SET must be Generated, Propagated, and Captured to Create $P(fs)_{SET\to SEU}$

$P\left(\frac{fs}{LETS}\right)$

- Probability of capturing a SET at a given LET per RCELL
- Probability a SET can turn “ON” an “OFF” gate
- Probability a SET can reach a DFF or Output

SETs that will propagate:

- SET with adequate width and amplitude

SETs that will not propagate or that will attenuate:

- SET with Small Amplitude
- SET with Narrow Pulse Width

Gate cut-off frequencies filter SETs as they propagate through CCELLS.
Transient width as Seen From the Destination DFF and Frequency can Affect $P(fs)_{SET \rightarrow SEU}$

Low LET produces smaller SETs $\rightarrow \tau_{width}$ is smaller $\rightarrow$ $P(fs)_{SET \rightarrow SEU}$ (probability of capture) at RCELLs is lower

Can make it difficult to find $\text{LET}_{th}$ while testing with low frequencies
SEE testing has been performed for Windowed Shift Registers (WSR) with varying N levels of combinatorial logic between DFFs.

Frequencies have been varied from 1MHz to 160MHz.

Data patterns were also varied (Static 0, Static 1, Checkerboard).

Testing Parameters Affect \( LET_{th} \)

- Low LETs have small transients → can significantly reduce the error cross section if frequency is too low.
- Discovering the lowest \( LET_{th} \) requires sophisticated test schemes that enable high speed operation.

\( P(\text{fs})_{\text{SET} \rightarrow \text{SEU}} \) and SET propagation in RCELLs and CCELLS:

- **RCELL:**
  \[
  P_{\text{DF SEU}} + P(\text{fs})_{\text{SET} \rightarrow \text{SEU}}
  \]
  \( P_{\text{prop}} \) is high

- **CCELLs:**
  \[
  P(\text{fs})_{\text{SET} \rightarrow \text{SEU}}
  \]
  \( P_{\text{prop}} \) Depends on the SET’s ability to get through several CCELLS and higher capacitive NETs without getting filtered away

With Small SETs, \( P(f_s)_{\text{SET} \rightarrow \text{SEU}} \) is Non-Linear with respect to Serially Adding CCELL logic

\[
P(f_s)_{\text{SET} \rightarrow \text{SEU}} \propto \sum_{i=1}^{\text{Number of CCells}} P_{\text{gen}(i)} P_{\text{prop}(i)} \tau_{\text{width}} f_s
\]

- **Higher LETs** → Wider SETs Propagate with sufficient amplitude → More CCELLS contribute to upsets
- **Low LETs** → some SETs get attenuated by CCELLs, hence SRs with a small number of CCELLS can have a slightly larger cross section at low LET
- **Non-Linear**: Depending on the CCELL configuration and the CCELL output load, LET attenuation can result in different shapes
LETs Affect SET Propagation and Consequently Affect SEU Cross Section

Real Circuits Have Fan-In and Fan-Out... How can this affect LET_{th}?

- Fan-In can increase \( P(f_{S})_{SET\rightarrow SEU} \)
- More paths that can pass narrow SETs to DFFs... Can affect LET_{th}

\[
P(f_{S})_{SET\rightarrow SEU} \propto \sum_{i} \text{Number of Cells} \cdot P_{\text{gen}}(i) \cdot P_{\text{prop}}(i) \cdot \tau_{\text{width}(i)}
\]

Considerations when Developing a Complex Design Test Methodology

• Design should contain Repeatability ... increase statistics

• Stress building blocks...
  – Test Design should be stressed at highest frequency
  – Full state space traversal should be accomplished within one test run

• Fault Isolation...Create test designs that will facilitate error detection and differentiation

• Test design should have the characteristics of a complex design with:
  – Fan-Out and Fan-In > 1
Counters Meet Requirements

- Has characteristics of a complex design with:
  - fan-out and fan-in > 1
  - contains a mixture of sequential and combinatorial logic.
- Variety of data pattern frequencies \( f_d \)
- State spaceTraversal = \( \frac{2^N}{f_s} \)
  - 24 bit counter takes \( 1.6777216 \times 10^{7} \) clock cycles
  - Less than 1 second state space traversal for 17MHz and above

\[
fd = \frac{2^N}{f_s}
\]

- MSB depends on all other bits: Largest fan-in
- LSB has fan-in of one

2 Bit Counter State Space Example:

Counter Implementation – Non-stop Increment and Snapshot

- All counters must be observable
- Large number of counters requires too many outputs

- Parallel Counters:
  - All counters are independent
  - Great fault isolation
  - Full state space traversal
  - Requires special means to output each counter: Snapshot Array

**Fault Detection in a Counter**

- Counters are counting every cycle
- At the end of the snapshot cycle, all of the counters will be captured into snapshot array
- Snapshot will occur sometime after error... but will still be observed because counter upset will persist
- Single Bit upset Number (SBN) is the bit position that has flipped

**Example:** $SBN = 5; \ 2^{SBN} = 32$

Counter Value = expected value + $(2^{SBN}) \times (Bit_{\text{upset}} - Bit_{\text{expected}})$

<table>
<thead>
<tr>
<th>Counter Value</th>
<th>Bit_0</th>
<th>Bit_1</th>
<th>Bit_2</th>
<th>Bit_3</th>
<th>Bit_4</th>
<th>Bit_5</th>
<th>Bit_6</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>000</td>
<td>1010</td>
<td>0100</td>
<td>0000</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0</td>
<td>000</td>
<td>1011</td>
<td>0101</td>
<td>0001</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0</td>
<td>000</td>
<td>1110</td>
<td>0110</td>
<td>0010</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0</td>
<td>000</td>
<td>1111</td>
<td>0111</td>
<td>0011</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

All values will be off by $(2^{SBN}) \times (Bit_{\text{upset}} - Bit_{\text{expected}})$ after the upset occurs.

Counters at 120MHz Have a Lower LET$_{th}$ than SRs at 160MHz

Fault Isolation and Analysis: Counter SEU Bit Errors @120MHz

- Counter Fan-In Increases probability of observing lowest LETth values
- At higher LETs Lower order bits have the highest cross section as expected due to the higher frequency data patterns of the counter.
Summary: REAG Evolution of FPGA Designs Under Test

**Traditional Shift Register Testing with addition of Combinatorial logic**

*WSRs: High Speed Signal Integrity*

*Counter Arrays: More Realistic testing… not meant to replace WSRs – just an enhancement*

*All Designs are used for all FPGA dynamic tests*

Conclusion

- Cross Sections are affected by:
  - Frequency of operation
  - Data Pattern
  - Propagation strength due to LET of ionizing particle and resultant SET size
  - Fan-in and Fan-out
  - Tester Integrity

- The significance of $\text{LET}_{\text{th}}$ within FPGA Bit Error-rate calculations and the difficultly of finding $\text{LET}_{\text{th}}$ dictates the necessity of complex testing

- Tester must be fast enough to drive the DUT and capture DUT output:
  - Test circuit must be stressed during testing

\[ \frac{\tau_{\text{width}}}{\tau_{\text{clk}}} \text{ can significantly decrease } P_{\text{SET} \rightarrow \text{SEU}} \text{ if } \tau_{\text{clk}} \text{ is too large (low frequency) and } \tau_{\text{width}} \text{ is small (@ low } \]
Conclusion

• REAG has developed a novel test structure that can characterize circuits with fan-in and fan-out
  – Uses an independent parallel array of counters
  – Can operate up to speeds of 120MHz
  – Fault isolation and detection is superior to serial cascaded counters

• Realistic circuits such as counters have proven to be a beneficial test point:
  – counter fan-in paths have uncovered lower LET_{th} values
  – Because of the intricate fault isolation of parallel counters, an in-depth bit analysis can be performed:

• Proposed Test Methodology can be used in all