Single Event Upset (SEU) Analysis of Complex Circuits Implemented in Actel RTAX-S Field Programmable Gate Array (FPGA) Devices

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Sponsor: NASA Electronic Parts and Packaging (NEPP)

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Motivation

- The SEU cross section Linear Energy Transfer threshold (LET_{th}) is a significant factor that drives device bit error rates
- The ability to uncover LET_{th} has proven to be a challenging task for FPGA devices
- Traditional SEU FPGA Testing has been limited:
  - Shift Registers: Simple, linear Data Paths
  - Complex circuits: Restricted State Space Traversal during irradiation
  - Inability to observe all digital upsets due to tester limitations
- Presentation will discuss –
  - Actel Anti-fuse FPGA (RTAXs) susceptibility
    - Flip Flop (DFF) Single Event Upsets (SEUs) $\rightarrow P_{DFFSEU}$
    - Single Event Transient (SET) Capture ($P_{SET \rightarrow SEU}$)
  - Traditional testing methodologies and results
  - Evolution of testing techniques and results

Actel RTAXs Susceptibility and Embedded Mitigation

M. Berg ***Selection of Integrated Circuits for Space Systems*** **IEEE NSREC 2009 Short Course, Quebec City, CN**

$$P(fs)_{error} \propto P_{Configuration} + P_{functionalLogic} + P_{SEFI}$$

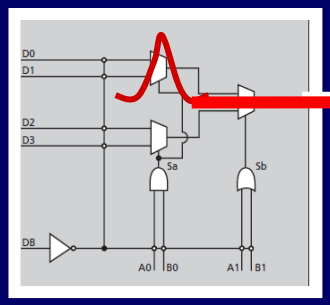
Design Specific SEE upset rate

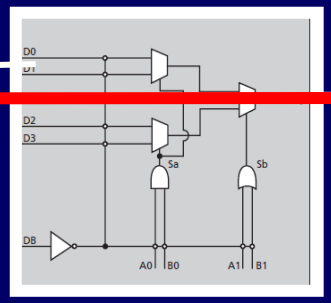
Configuration SEE upset rate

Functional logic SEE upset rate

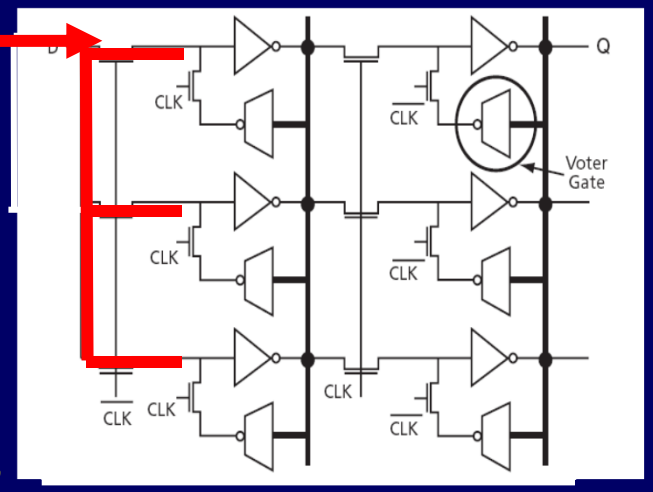
Single Event functional Interrupt

$$P_{DFFSEU} + P(fs)_{SET \rightarrow SEU}$$





CCELLs: Combinatorial logic cells



RCELLS: DFF + Combinatorial

Local Triple Modular Redundant (LTMR) DFFs lower P_{DFFSEU} but can not mitigate $P(fs)_{SET \rightarrow SEU}$

A SET must be Generated, Propagated, and Captured to Create $P(fs)_{SET \rightarrow SEU}$

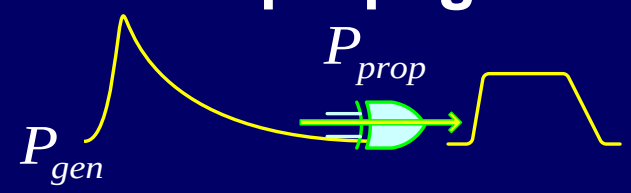
$P(fs)_{SET \rightarrow SEU} \big|_{LET}$ *Probability of capturing a SET at a given LET per RCELL*

P_{gen} *Probability a SET can turn "ON" an "OFF" gate*

P_{prop} *Probability a SET can reach a DFF or Output*

SETs that will propagate:

SET with adequate width and amplitude



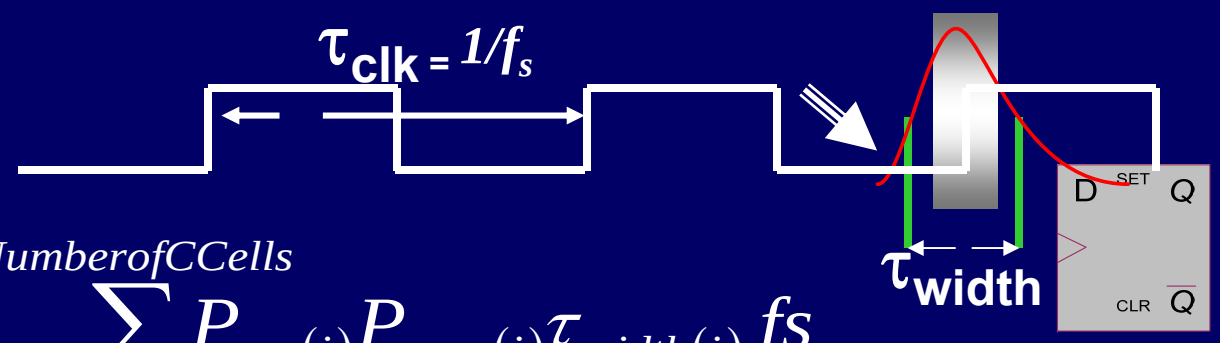
Gate cut-off frequencies filter SETs as they propagate through CCELLS.

SETs that will not propagate or that will attenuate:

SET with Small Amplitude

SET with Narrow Pulse Width

Transient width as Seen From the Destination DFF and Frequency can Affect $P(fs)_{SET \rightarrow SEU}$



$$P(fs)_{SET \rightarrow SEU} \propto \sum_{i=1}^{NumberofCCells} P_{gen(i)} P_{prop(i)} \tau_{width(i)} fs$$

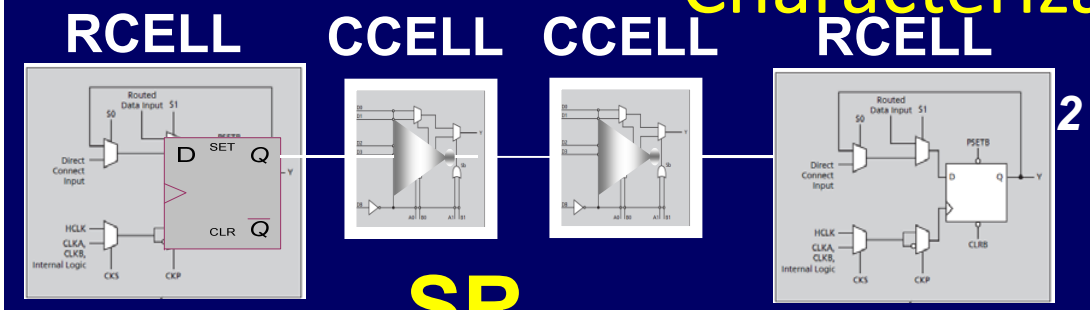
At a given RCELL at a given LET

$$\propto \sum_{i=1}^{NumberofCCells} P_{gen(i)} P_{prop(i)} \left(\frac{\tau_{width(i)}}{\tau_{clk}} \right)$$

Source: M. Berg ***Design for Radiation Effects*** **MAPLD 2008 Annapolis, MD**

- **Low LET produces smaller SETs → τ_{width} is smaller → $P(fs)_{SET \rightarrow SEU}$ (probability of capture) at RCELLs is lower**
- **Can make it difficult to find LET_{th} while testing with low frequencies**

Shift Register (SR) Test Structures for Actel SEU Characterization



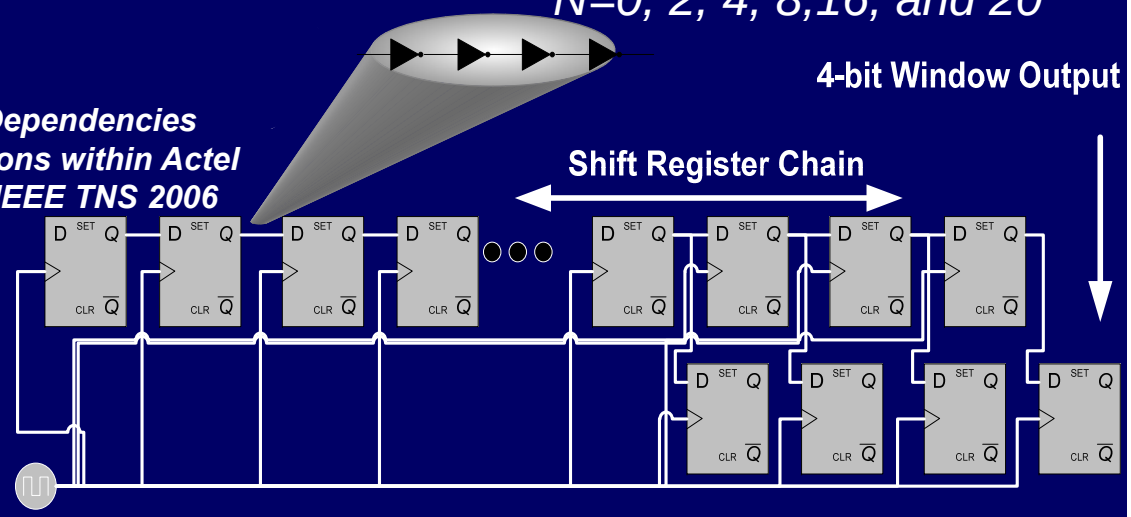
SR

N levels of inverters between DFF stages:

N=0, 2, 4, 8,16, and 20

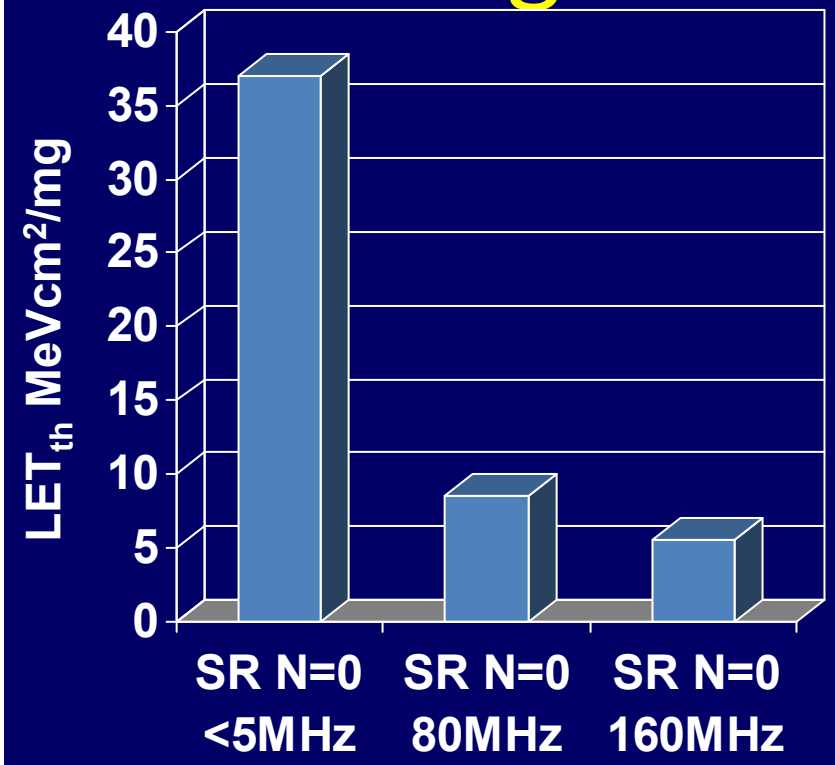
M.Berg et. al. "An Analysis of Single Event Upset Dependencies on High Frequency and Architectural Implementations within Actel RTAX-S Family Field Programmable Gate Arrays", IEEE TNS 2006

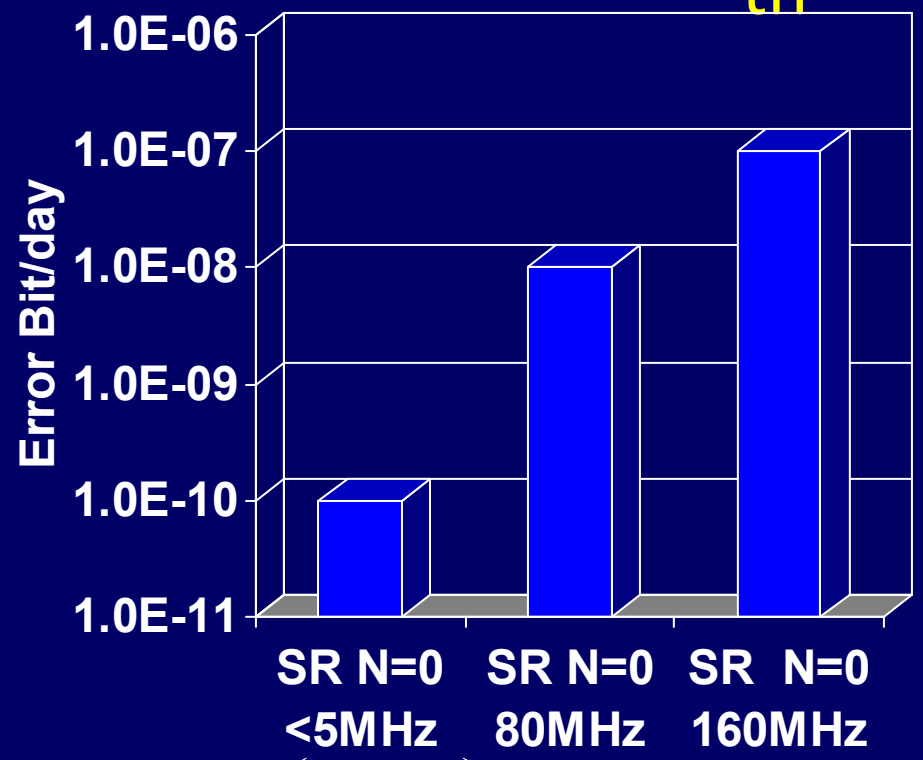
WSR



- SEE testing has been performed for Windowed Shift Registers (WSR) with varying N levels of combinatorial logic between DFFs
- Frequencies have been varied from 1MHz to 160MHz
- Data patterns were also varied (Static 0, Static 1, Checkerboard)

Testing Parameters Affect LET_{th}

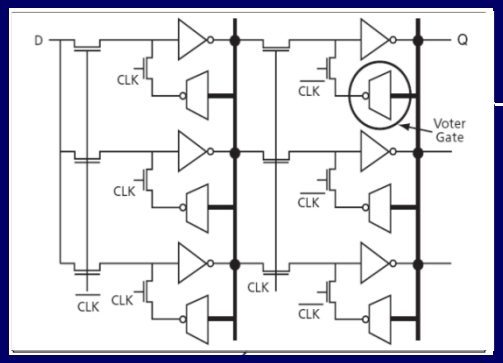




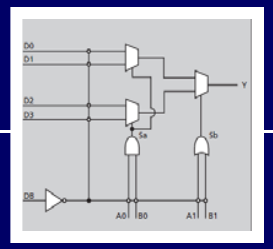
- Low LETs have small transients→ $\left(\frac{\tau_{width(i)}}{\tau_{clk}}\right)$ can significantly reduce the error cross section if frequency is too low
- Discovering the lowest LET_{th} requires sophisticated test schemes that enable high speed operation

$P(fs)_{SET \rightarrow SEU}$ and SET propagation in RCELLs and CCELLS:

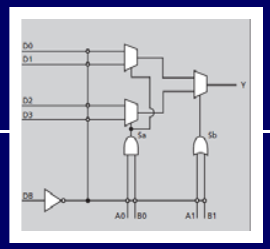
RCELL



TX



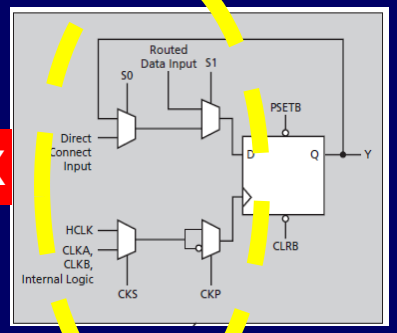
CCELL



CCELL

RX

RCELL

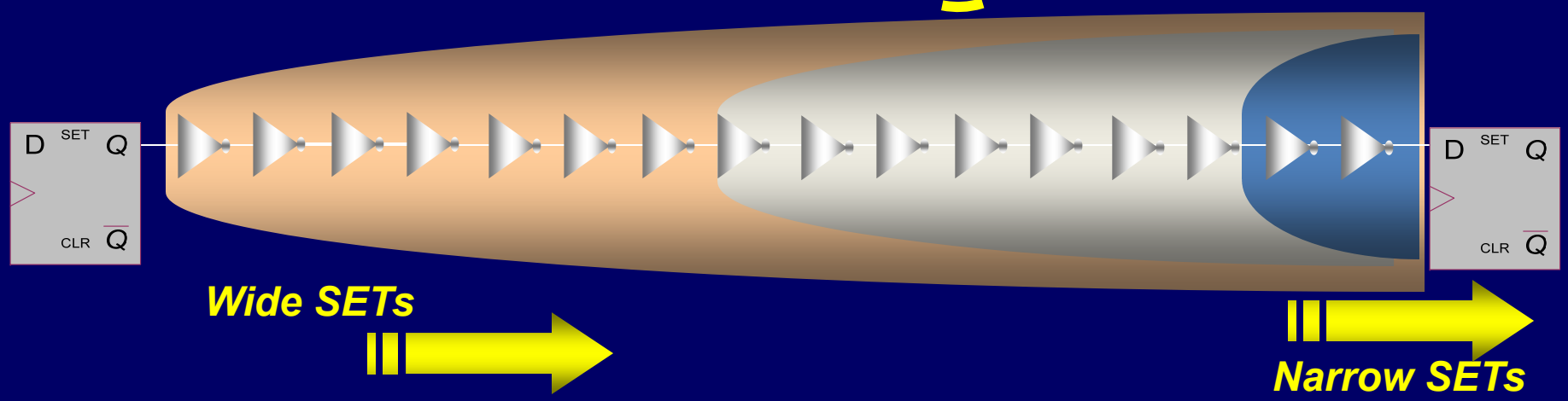


RCELL: $P_{DF\ SEU} + P(fs)_{SET \rightarrow SEU}$ ***P_{prop} is high***

CCELLs: $P(fs)_{SET \rightarrow SEU}$ ***P_{prop} Depends on the SET's ability to get through several CCELLS and higher capacitive NETs without getting filtered away***

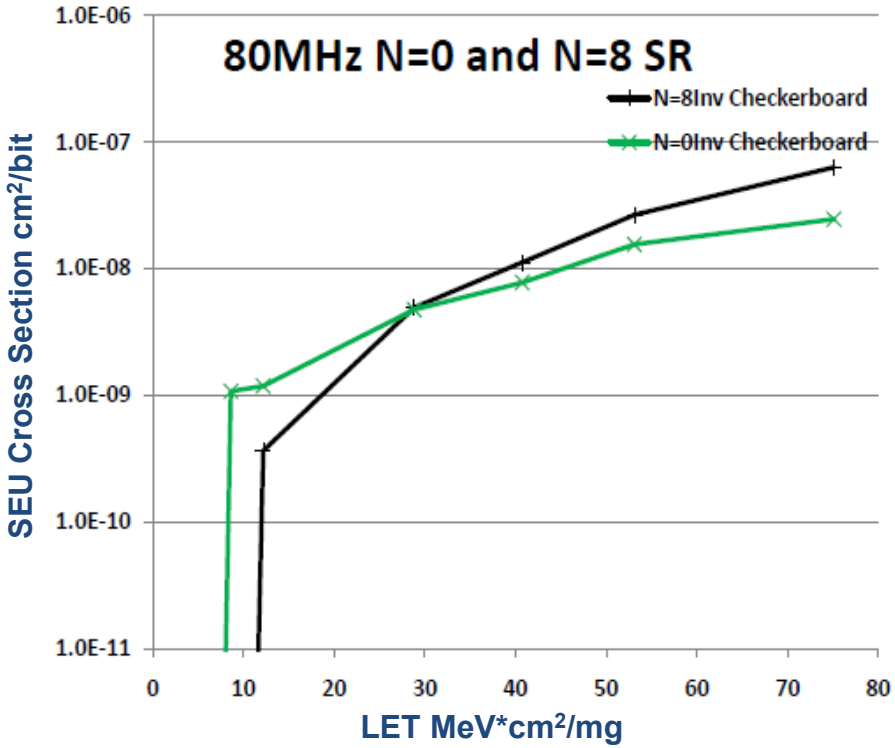
With Small SETs, $P(fs)_{SET \rightarrow SEU}$ is Non-Linear with respect to Serially Adding CCELL logic

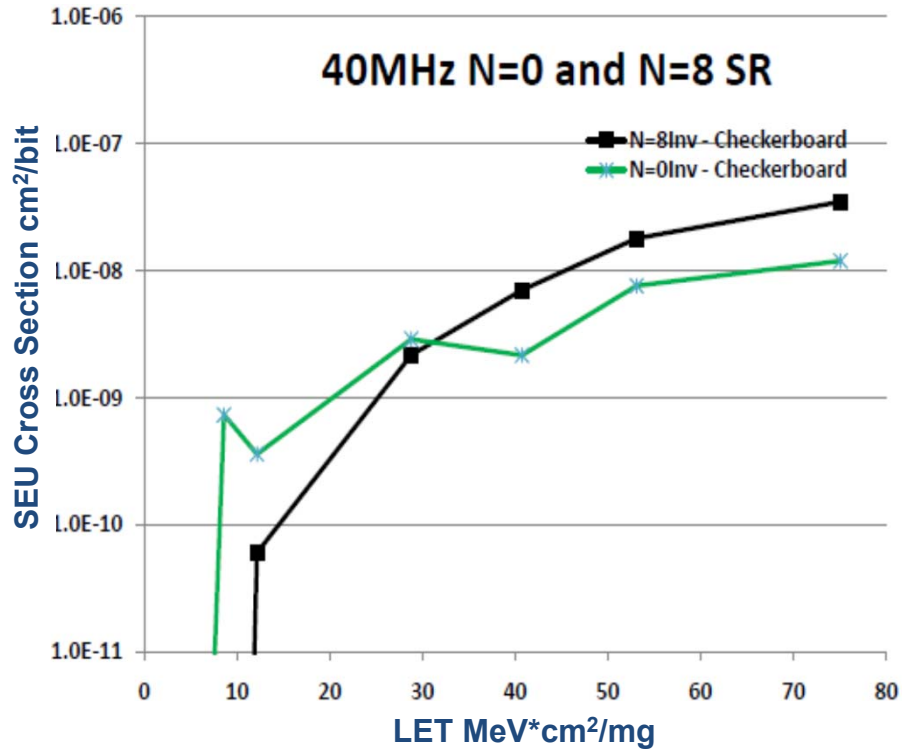
$$P(fs)_{SET \rightarrow SEU} \propto \sum_{i=1}^{NumberofCCells} P_{gen(i)} P_{prop(i)} \tau_{width} fs$$



- **Higher LETs → Wider SETs Propagate with sufficient amplitude→ More CCELLS contribute to upsets**
- **Low LETs→ some SETs get attenuated by CCELLs, hence SRs with a small number of CCELLS can have a slightly larger cross section at low LET**
- **Non-Linear: Depending on the CCELL configuration and the CCELL output load, LET attenuation can result in different shapes**

LETs Affect SET Propagation and Consequently Affect SEU Cross Section

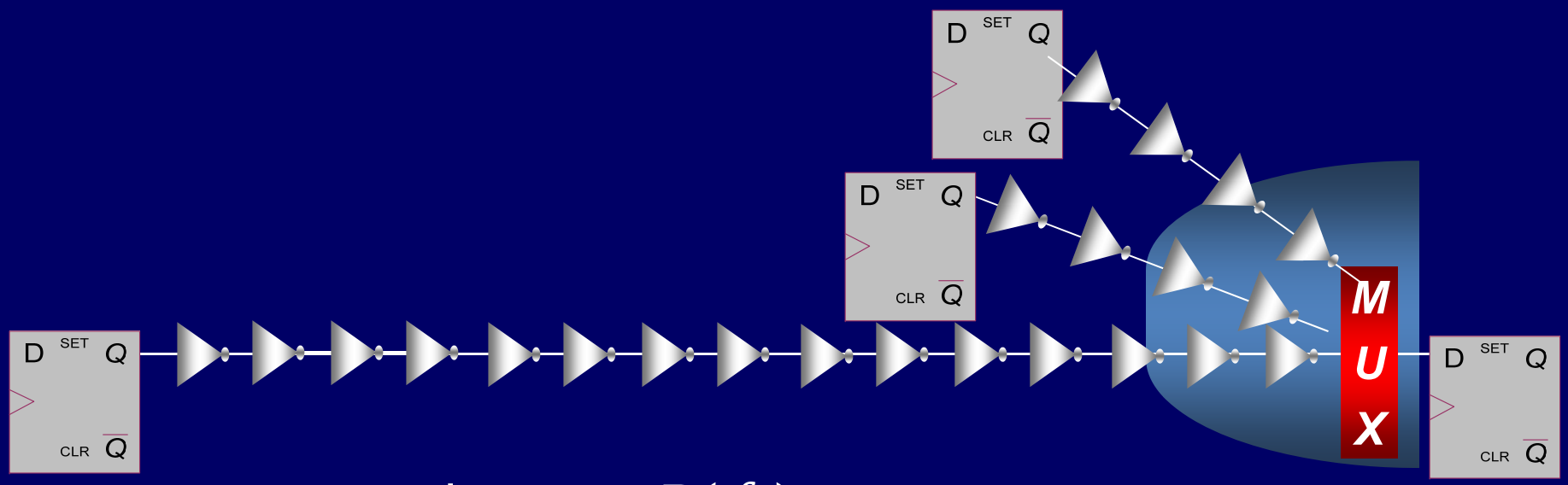




$$P(fs)_{SET \rightarrow SEU} \propto \sum_{i=1}^{NumberofCCells} P_{gen(i)} P_{prop(i)} \tau_{width} fs$$

Lower LET values→ SR N=0 has higher SEU cross section than SR N=8. Demonstrates SET filtration effects

Real Circuits Have Fan-In and Fan-Out… How can this affect LET_{th}?



- Fan-In can increase $P(fs)_{SET \rightarrow SEU}$
- More paths that can pass narrow SETs to DFFs… Can affect LET_{th}

$$P(fs)_{SET \rightarrow SEU} \propto \sum_{i=1}^{NumberofCCells} \frac{P_{gen(i)} P_{prop(i)} \tau_{width(i)}}{\tau_{clk}}$$

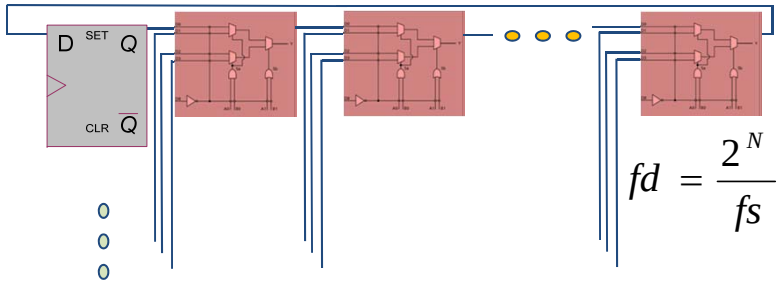
Considerations when Developing a Complex Design Test Methodology

- Design should contain Repeatability … increase statistics
- Stress building blocks…
  - **Test Design should be stressed at highest frequency**
  - Full state space traversal should be accomplished within one test run
- Fault Isolation…Create test designs that will facilitate error detection and differentiation
- Test design should have the characteristics of a complex design with:
  - Fan-Out and Fan-In > 1

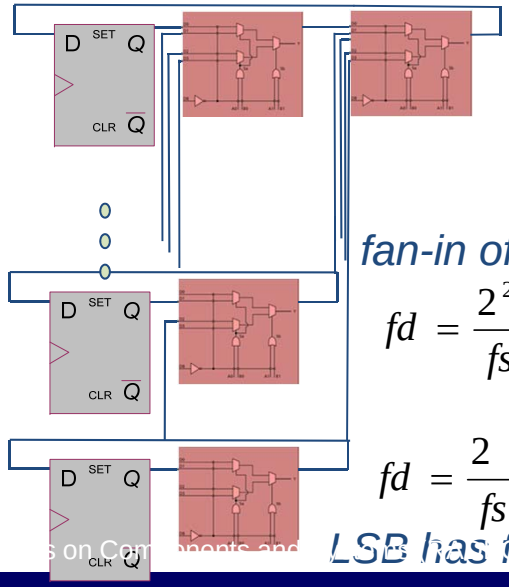
Counters Meet Requirements

- Has characteristics of a complex design with:
  - fan-out and fan-in > 1
  - contains a mixture of sequential and combinatorial logic.
- Variety of data pattern frequencies (f_d)
- State space Traversal = $2^N/f_s$
  - 24 bit counter takes 1.6777216×10^7 clock cycles
  - Less than 1 second state space traversal for 17MHz and above

MSB depends on all other bits: Largest fan-in



$$fd = \frac{2^N}{fs}$$



fan-in of two

$$fd = \frac{2^2}{fs}$$

$$fd = \frac{2}{fs}$$

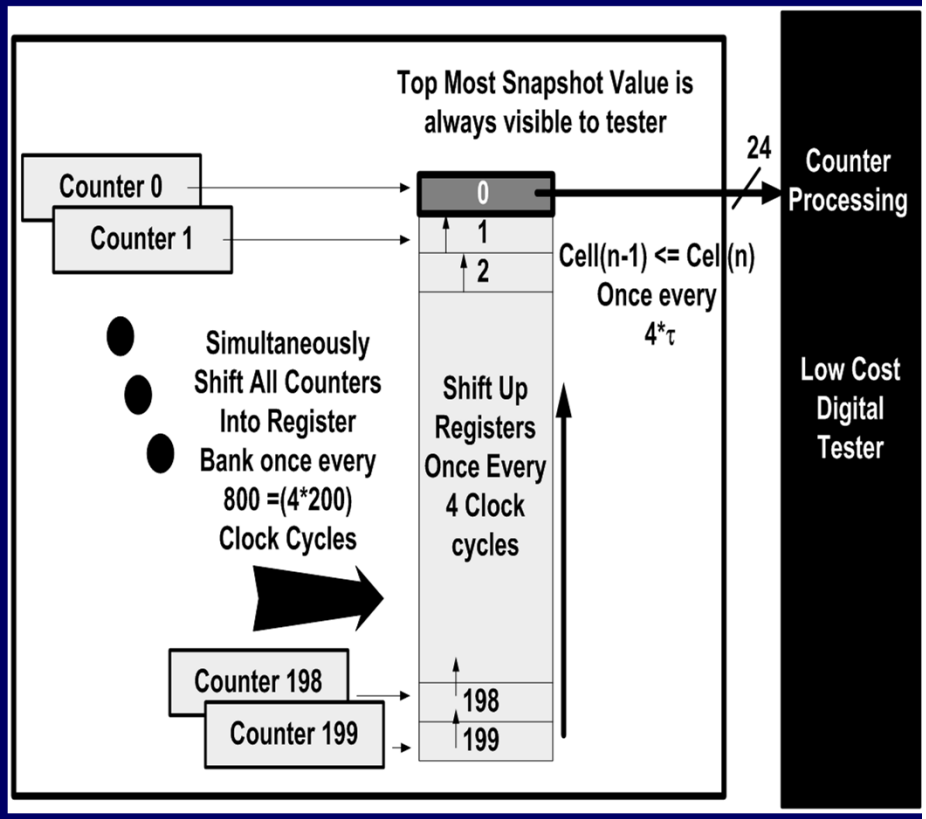
LSB has fan-in of one

2 Bit Counter State Space Example:

0	0	→	0	1	→	1	0	→	1	1

Counter Implementation – Non-stop Increment and Snapshot

- All counters must be observable
- Large number of counters requires too many outputs



- **Parallel Counters:**
  - All counters are independent
  - Great fault isolation
  - Full state space traversal
  - Requires special means to output each counter: Snapshot Array

Fault Detection in a Counter

- Counters are counting every cycle
- At the end of the snapshot cycle, all of the counters will be captured into snapshot array
- Snapshot will occur sometime after error… but will still be observed because counter upset will persist
- Single Bit upset Number (SBN) is the bit position that has flipped

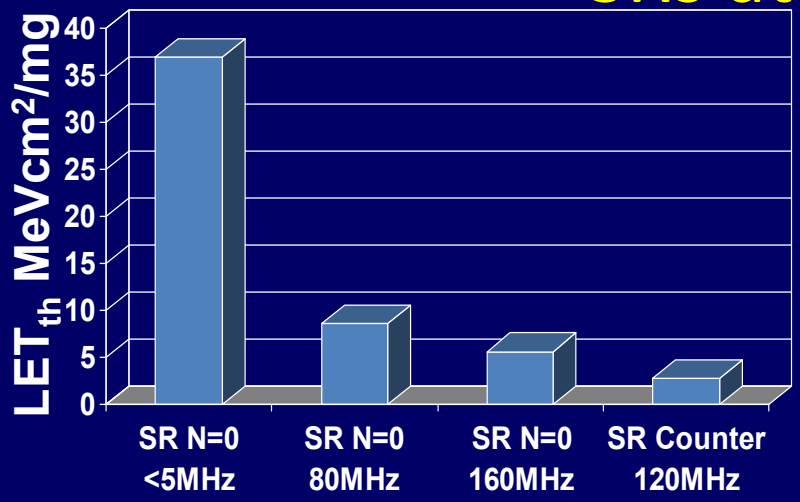
Example: SBN = 5; $2^{SBN} = 32$

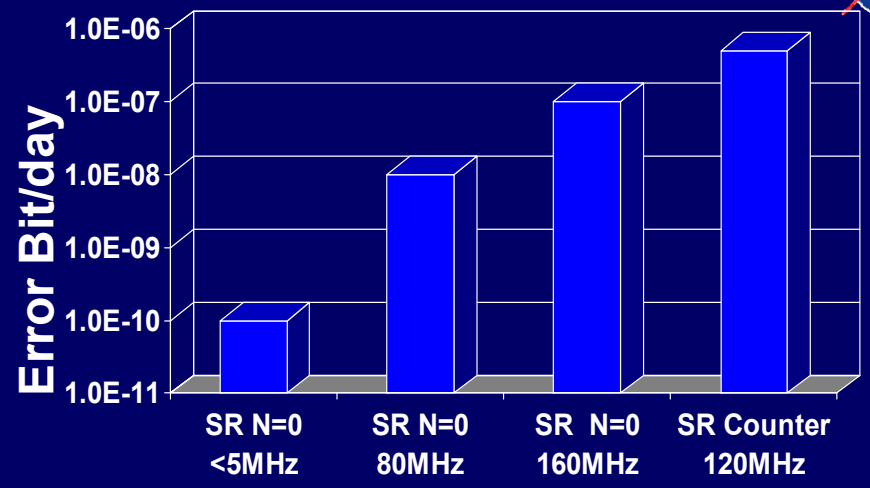
Counter Value = expected value + $(2^{SBN})*(Bit_{upset}-Bit_{expected})$

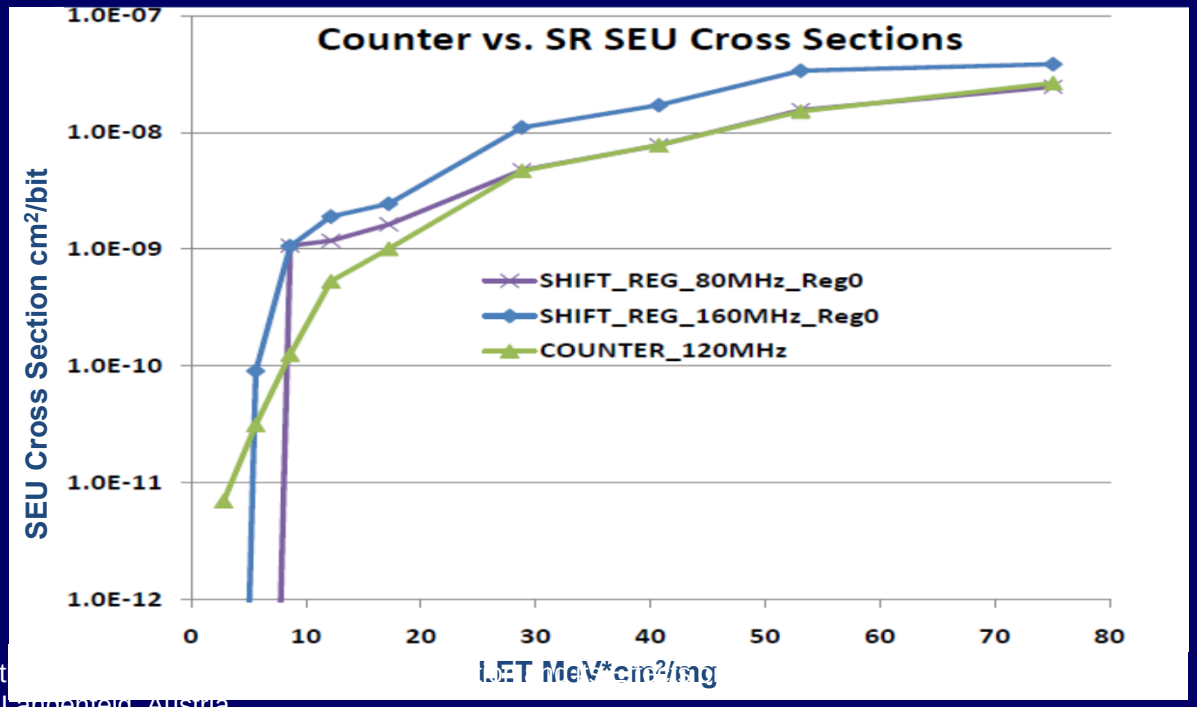
All values will be off by $(2^{SBN})*(Bit_{upset}-Bit_{expected})$ after the upset occurs

23		6	5	4	3	2	1	0		
0		0	0	1	0	1	0	0	20	
0	…	0	1	1	0	1	0	1	21	53
0		0	1	1	0	1	1	0	22	54

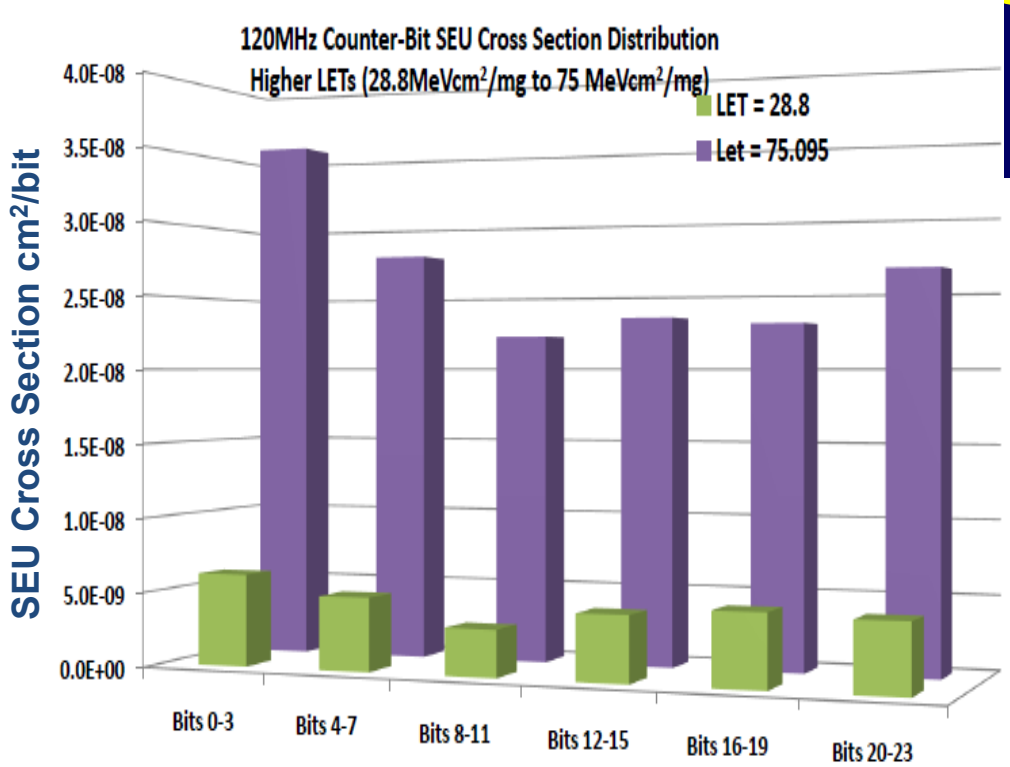
Counters at 120MHz Have a Lower LET_{th} than SRs at 160MHz

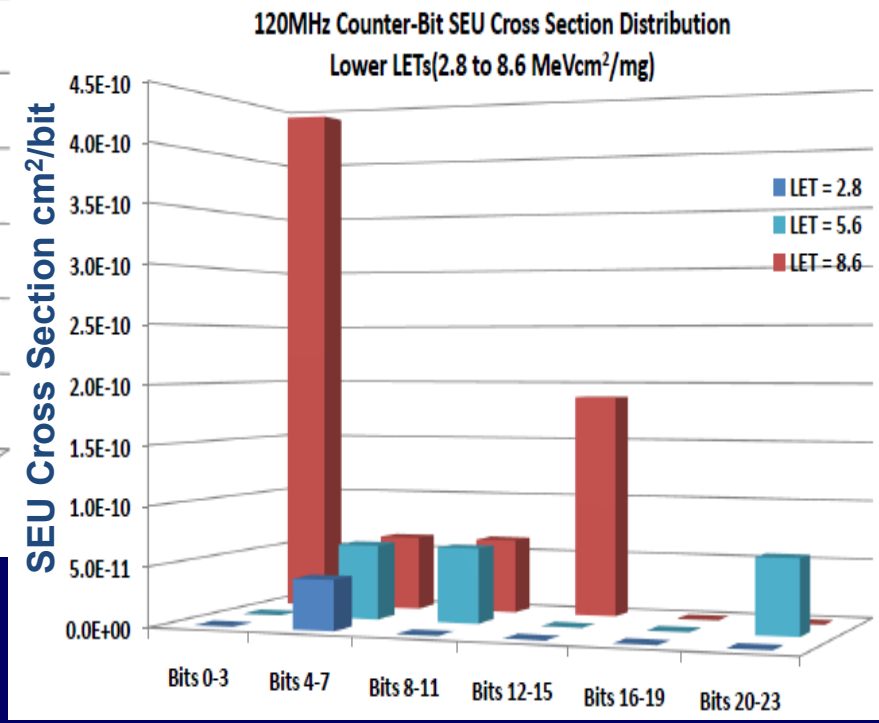






Fault Isolation and Analysis: Counter SEU Bit Errors @120MHz

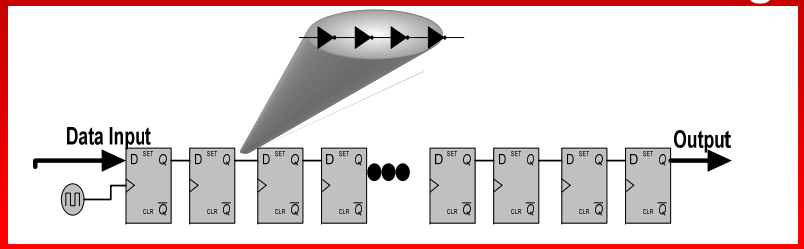




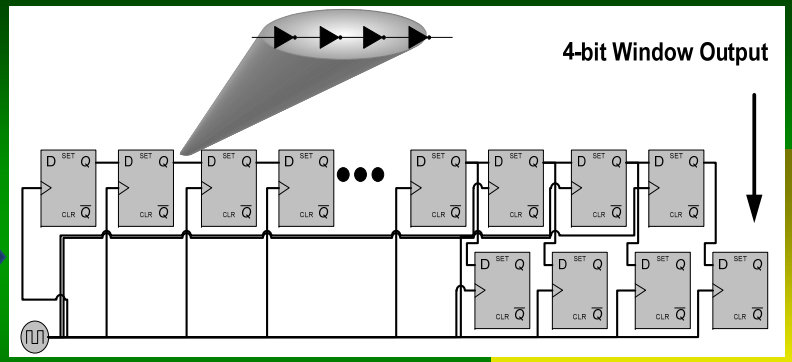
- Counter Fan-In Increases probability of observing lowest LETth values
- At higher LETs Lower order bits have the highest cross section as expected due to the higher frequency data patterns of the counter

Summary: REAG Evolution of FPGA Designs Under Test

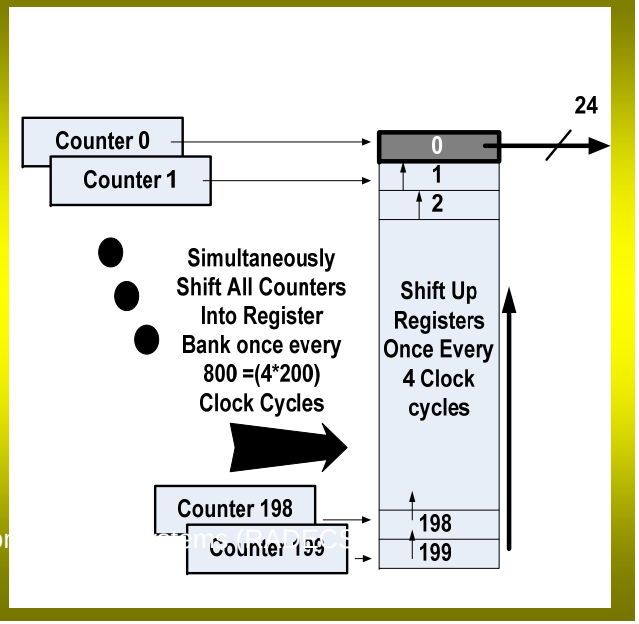
Traditional Shift Register Testing with addition of Combinatorial logic



WSRs: High Speed Signal Integrity



Counter Arrays: More Realistic testing… not meant to replace WSRs – just an enhancement



All Designs are used for all FPGA dynamic tests

Conclusion

- Cross Sections are affected by:
  - Frequency of operation
  - Data Pattern
  - Propagation strength due to LET of ionizing particle and resultant SET size
  - Fan-in and Fan-out
  - Tester Integrity
- The significance of LET_{th} within FPGA Bit Error-rate calculations and the difficultly of finding LET_{th} dictates the necessity of complex testing
- Tester must be fast enough to drive the DUT and capture DUT output:
  - Test circuit must be stressed during testing
  - τ_{width}/τ_{clk} can significantly decrease $P_{SET \rightarrow SEU}$ if τ_{clk} is too large (low frequency) and τ_{width} is small (@ low

Conclusion

- REAG has developed a novel test structure that can characterize circuits with fan-in and fan-out
  - Uses an independent parallel array of counters
  - Can operate up to speeds of 120MHz
  - Fault isolation and detection is superior to serial cascaded counters
- Realistic circuits such as counters have proven to be a beneficial test point:
  - counter fan-in paths have uncovered lower LET_{th} values
  - Because of the intricate fault isolation of parallel counters, an in-depth bit analysis can be performed:
- Proposed Test Methodology can be used in all