Effect of compressive stresses on leakage currents in microchip tantalum capacitors

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Abstract

Microchip tantalum capacitors are manufactured using new technologies that allow for production of small size capacitors (down to EIA case size 0402) with volumetric efficiency much greater than for regular chip capacitors. Due to a small size of the parts and leadless design they might be more sensitive to mechanical stresses that develop after soldering onto printed wiring boards (PWB) compared to standard chip capacitors. In this work, the effect of compressive stresses on leakage currents in capacitors has been investigated in the range of stresses up to 200 MPa. Significant, up to three orders of magnitude, variations of currents were observed after the stress exceeds a certain critical level that varied from 30 MPa to 140 MPa for six types of microchip capacitors used in this study. A stress-induced generation of electron traps in tantalum pentoxide dielectric is suggested to explain reversible variations of leakage currents in tantalum capacitors. Thermo-mechanical characteristics of microchip capacitors have been studied to estimate the level of stresses caused by assembly onto PWB and assess the risk of degradation of leakage currents.

Introduction

One of the major trends in electronic industry is further microminiaturization of devices, assemblies, and parts that requires production of high performance, efficient, and cheap components within a smaller volume. To answer the request for downsizing, manufacturers of tantalum capacitors developed recently new technologies to produce small size capacitors with increased volumetric efficiency that might replace with time conventional design tantalum capacitors that have been manufactured for more than 30 years. These technologies were originally developed for commercial mobile wireless devices such as handheld computers, SmartPhones, cameras, etc., but provided the parts have adequate quality and reliability, their application would be beneficial for space systems allowing for reduction of weight and size of assemblies and units.

Currently, tantalum capacitors with code size of 0603 and 0402 are commercially available from Vishay and AVX. Considering that tantalum capacitors have better time, temperature, and voltage stability of capacitance compared to ceramic (X7R) capacitors, these new technologies
are expanding successfully to areas of application where ceramic capacitors were traditionally used.

Although conventional chip tantalum capacitors are considered high volumetric efficiency devices, only ~30% of their volume is occupied by tantalum [1] and the rest is “wasted” mostly for the lead frame and molding compound (MC). New technologies increase volumetric efficiency further, up to ~45% for TM8 (Vishay) series and up to 54% for TAC (AVX) series devices [2].

Our previous study [3] showed that compressive stresses might degrade substantially characteristics of tantalum capacitors and cause failures. Leakage currents in regular chip capacitors under compressive stress increased more than two orders of magnitude and surge current breakdown voltages were up to 40% less than for unstressed capacitors. Different part types had different sensitivity to mechanical stresses, and average levels of critical stresses varied from 10 MPa to 40 MPa. The most intriguing feature of the stress-induced degradation was the reversibility of current variations and hysteresis during measurements at increasing and decreasing forces.

Microchip capacitors do not have leads that might provide some stress relief, and their cross-sectional area and thickness of the encapsulating molding compound are smaller compared to regular chip tantalum capacitors. This might make them more susceptible to the effect of mechanical stresses. In this work, variations of leakage currents in different types of microchip tantalum capacitors with compressive stresses were studied to assess the level of critical stresses and get more insight into the mechanism of the effect. Thermo-mechanical (coefficients of thermal expansion, CTE) and mechanical (Young’s modulus) characteristics of the parts were measured to estimate soldering-induced mechanical stresses in microchips and evaluate the risk of degradation caused by assembly onto PWBs.

### Experiment

Seven types of microchip tantalum capacitors from two manufacturers were used in this study. Table 1 shows description of the parts including their specified electrical characteristics and size.

<table>
<thead>
<tr>
<th>Gr.</th>
<th>Mfr</th>
<th>C, uF</th>
<th>VR, V</th>
<th>case</th>
<th>DCL, μA</th>
<th>L, mm</th>
<th>W, mm</th>
<th>H, mm</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>A</td>
<td>33</td>
<td>10</td>
<td>A (1206)</td>
<td>3.3</td>
<td>3.2</td>
<td>1.6</td>
<td>1.6</td>
</tr>
<tr>
<td>2</td>
<td>A</td>
<td>33</td>
<td>10</td>
<td>R (0805)</td>
<td>3.3</td>
<td>2.1</td>
<td>1.4</td>
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<tr>
<td>3</td>
<td>A</td>
<td>1</td>
<td>35</td>
<td>R (0805)</td>
<td>0.5</td>
<td>2.1</td>
<td>1.4</td>
<td>1.4</td>
</tr>
<tr>
<td>4</td>
<td>A</td>
<td>10</td>
<td>10</td>
<td>R (0805)</td>
<td>1</td>
<td>2.1</td>
<td>1.4</td>
<td>1.4</td>
</tr>
<tr>
<td>5</td>
<td>B</td>
<td>10</td>
<td>16</td>
<td>A (1206)</td>
<td>0.8</td>
<td>3.4</td>
<td>1.7</td>
<td>1.7</td>
</tr>
<tr>
<td>6</td>
<td>B</td>
<td>47</td>
<td>10</td>
<td>T</td>
<td>2.35</td>
<td>3.5</td>
<td>2.8</td>
<td>1.5</td>
</tr>
<tr>
<td>7</td>
<td>B</td>
<td>4.7</td>
<td>6.3</td>
<td>M</td>
<td>0.16</td>
<td>1.6</td>
<td>0.85</td>
<td>0.85</td>
</tr>
</tbody>
</table>

To assess the effect of compressive stresses, leakage currents of capacitors were monitored under the stresses changing with time. A stress created by a compressed spring was applied to the

terminals of the parts and was monitored by a force gage. A PC-based data acquisition system that is shown in Figure 1 allowed for programming of stress and voltage variations with time and for recording the values of applied force, voltage, and leakage current.

![Figure 1. Experimental set-up for programming stress and voltage profiles and monitoring leakage currents in microchip capacitors with time.](image)

To assess the effective coefficients of thermal expansion of microchip tantalum capacitors, their deformation was measured with temperature using a thermal mechanical analyzer, TMA2940, manufactured by TA Instruments. These measurements were carried out at a rate of 3 °C/min. during cooling from 220 °C, followed by heating the sample in the analyzer at the same rate. Using the cooling curve allowed for diminishing of the effects related to the stress relief and elimination of possible errors caused by the presence of moisture. Measurements of deformations were carried out along the terminals with a probe placed directly on one of the terminals of the part.

To assess the effective Young’s modulus, $E$, of the capacitors and tantalum anode (slug) deformation of the parts and the level of applied load were recorded using an Instron Model 4442 tester. Measurements were carried out at compressive forces up to 250 N during increasing and decreasing of the load at a speed of 0.005 in/min.

**Results**

*Effect of mechanical stresses on leakage currents.*

Typical experimental results for different part types showing variations of leakage currents with compressive stresses at rated voltages are shown in Figures 2 to 4. Electro-mechanical behavior of microchip capacitors is similar to what was observed for regular tantalum capacitors and indicate that stresses might substantially, in some cases (see Figure 4a) up to three orders of magnitude, increase leakage currents. After the stress removal the currents might recover completely (see Figures 2a, 3b, and 4b) or partially, decreasing noticeably, but not to the initial level (see Figures 2b, 3a).
In some cases, currents increased instantaneously from $\sim 10^{-9}$ A to $\sim 10^{-5}$ A, as in Figure 2a, sharply drop to $\sim 10^{-7}$ A and then gradually decrease back to the nanoampere level. The sharp spike is likely due to a scintillation breakdown caused by mechanical damage to the Ta$_2$O$_5$ dielectric. However, in most cases currents increased gradually, remained relatively stable when the stress was stabilized, and then decreased as the stress lowered to the “safe” level of 5 N that was used to maintain electrical contacts to the part. A delay in stabilization of currents is clearly seen in Figures 3b and 4b where the current levels off in approximately 1.5 min after stabilization of stress.

Figure 2. Effect of compressive mechanical stresses on Gr.2 and Gr.3 microchip capacitors.

Figure 3. Variations of leakage currents with compressive stresses in Gr.4 microchip capacitors.

Figure 4. Variation of leakage currents with compressive stresses Gr.7 microchip capacitors.

To evaluate I-V characteristics under stress, currents were monitored after application of different voltages for 3 to 5 minutes till stabilization as shown in Figure 5a. Typical I-V
characteristics of microchip capacitors in initial and stressed (under 100 N) conditions are shown in Figure 5b. In Poole-Frenkel coordinates, \( \ln(I/V) \) vs. \( V^{0.5} \), the data can be approximated with straight lines indicating bulk-limited Poole-Frenkel conduction that is due to electrons released to a conduction band from traps in the forbidden energy gap of the oxide. The similarity of I-V characteristics in compressed and unstressed capacitors suggests that the same mechanism likely controls conduction of the dielectric in both cases.

Based on \( I - F \) characteristics measured at rated voltages, the values of critical forces, \( F_{cr} \), that correspond to a substantial (at least 2 times) increase in leakage currents were determined for each capacitor. The relevant critical stresses, \( \sigma_{cr} \), were calculated as a ratio of \( F_{cr} \) to the cross-sectional area of the part. Distributions of critical stresses are shown in Weibull coordinates in Figure 6. In most cases the distributions could be approximated with two-parameter Weibull functions with slopes, \( \beta \), varying in a relatively narrow range, from 3 to 4. Similar slopes for different part types indicate that likely the same mechanism is responsible for the stress-induced degradation of leakage currents in all microchip capacitors. The characteristic critical stress, \( \eta \), for different groups of capacitors varied in a wide range from 33 MPa to 156 MPa.

One sample in Gr.2 parts was “out of family” showing degradation at a stress as low as 10 MPa that was more than 3 times less than for other samples in this group. Similar parts might result in failures caused by soldering and handling-related stresses (e.g. board flexing). To avoid failures and reveal defective lots, the susceptibility of microchips to mechanical stresses should be evaluated during qualification testing of the parts. This can be done by measuring leakage currents in a group of parts under a stress of 10 MPa and comparing results with the initial measurements. For normal quality parts currents under the stress should not increase more than 100%.
Figure 6. Distributions of critical stresses in different types of microchip tantalum capacitors.

Table 2 displays parameters of distributions of the critical stresses for six types of capacitors. Average values of $\sigma_{cr}$ for all groups, except for Gr.7, were in a range, from 30 MPa to 60 MPa that is slightly greater than what was observed for regular chip tantalum capacitors [3]. Interestingly, the smallest size capacitors, Gr.7, had the largest values of $\sigma_{cr}$ that vary from 81 MPa to 185 MPa.

Table 2. Critical stresses (MPa) in microchip tantalum capacitors.

<table>
<thead>
<tr>
<th>Lot</th>
<th>QTY</th>
<th>$\beta$</th>
<th>$\eta$</th>
<th>Mean</th>
<th>STD</th>
<th>max</th>
<th>min</th>
</tr>
</thead>
<tbody>
<tr>
<td>Gr.1</td>
<td>9</td>
<td>4.1</td>
<td>55.2</td>
<td>50.1</td>
<td>13.7</td>
<td>75.4</td>
<td>32.0</td>
</tr>
<tr>
<td>Gr.2</td>
<td>18</td>
<td>2.2</td>
<td>66.5</td>
<td>58.9</td>
<td>28.0</td>
<td>87.0</td>
<td>9.9</td>
</tr>
<tr>
<td>Gr.3</td>
<td>7</td>
<td>3.5</td>
<td>43.1</td>
<td>38.7</td>
<td>12.4</td>
<td>68.6</td>
<td>25.8</td>
</tr>
<tr>
<td>Gr.4</td>
<td>13</td>
<td>2.9</td>
<td>32.8</td>
<td>29.3</td>
<td>10.9</td>
<td>64.0</td>
<td>16.0</td>
</tr>
<tr>
<td>Gr.6</td>
<td>7</td>
<td>3.9</td>
<td>45.4</td>
<td>41.1</td>
<td>11.7</td>
<td>53.4</td>
<td>22.9</td>
</tr>
<tr>
<td>Gr.7</td>
<td>9</td>
<td>3.7</td>
<td>156.3</td>
<td>141.0</td>
<td>42.7</td>
<td>185.0</td>
<td>81.1</td>
</tr>
</tbody>
</table>

Thermo-mechanical characteristics of microchip tantalum capacitors.

Typical results of measurements of deformations for four types of capacitors are shown in Figure 7. Expansion of tantalum microchip capacitors with temperature is similar to molding compounds and exhibit two distinctive areas of deformation that might be approximated with straight lines and the interception point indicating the glass transition temperature (Tg) of the molding compound. The slopes of the lines give the effective values of CTE that are obviously less than CTE of molding compounds and depend on the relative size, Young’s modulus, and CTE values of the MC and tantalum slug.

Results of measurements of the TMA characteristics, including effective CTE values in the glassy (low temperatures, $T < T_g$) and rubbery (high temperatures, $T > T_g$) states of molding compounds are summarized in Table 3. The parts manufactured by the same vendor had similar
characteristics indicating that the same molding compound was used for different part types. Encapsulating polymer composition used by Mfr. A had a relatively low glass transition temperature, from 100 °C to 110 °C, and relatively large effective CTE values, exceeding 11 ppm/°C to 14 ppm/°C at low temperatures and 29 ppm/°C to 38 ppm/°C at high temperatures. Mfr. B employed high-Tg (~150 °C) molding compound that has lower CTE values in the glassy (~6 ppm/°C) and in rubbery (~12 ppm/°C) states.

![Figure 7. Thermo-mechanical characteristics of four types of microchip capacitors.](image)

Results of thermo-mechanical analysis of tantalum slugs showed that in the range of temperatures from room to 150 °C CTE = 5.7 ppm/°C and it increases to 6.5 ppm/°C at higher temperatures, from 150 °C to 300 °C. An average CTE in the range from room temperature to 300 °C is 6.2 ppm/°C, which is close to literature data for tantalum (6.3 ppm/°C). Considering that the stiffness of the tantalum slug is much greater than of molding compound, a difference between the effective CTE for microchips and tantalum slug indicates substantial stresses in the slug and the possibility that molding compound is shifting relatively to the slug under temperature excursions. Deformations of MC and slug with temperature and their possible displacements might result in mechanical stresses large enough to damage the tantalum pentoxide dielectric. Obviously, the greater the difference in CTEs between MC and the slug, the more probable damaging of the dielectric and failures of capacitors during temperature cycling are.

The values of CTE at low-temperatures for Mfr.B parts (~6.3 ppm/°C) are close to CTE of the tantalum slug. This decreases thermo-mechanical stresses in the slug caused by CTE mismatch with the MC, reduces the probability of damaging of the dielectric during temperature excursions, and improves reliability of the parts. Direct experiments performed in [4] showed that CTE mismatch between various materials used in the construction of a tantalum capacitor can cause leakage current failures after soldering. When soldering simulation was carried out with unencapsulated devices no change in leakage currents was observed; however, failures occurred when this experiment was repeated after encapsulation.
Unfortunately, an attempt to measure the effective Young’s modulus, \( E \), of the capacitors was not successful because the stiffness of the parts was relatively large and the measured deformations were close to the deformation of the frame with the gage. This allowed for rough estimations of a minimal level of the Young’s modulus only. Results of these estimations are presented in Table 3 and indicate \( E \) in the range from 5 GPa to 15 GPa. This range is consistent with the literature data for Young’s modulus of epoxy molding compounds (from 1 GPa to 20 GPa) and for porous tantalum materials (from 15 GPa to 20 GPa) with the pore volume fraction between 27% and 55% [5]. Note, that the Young’s modulus of solid tantalum at room temperature is much greater, \(~ 190 \) GPa.

### Discussion

*Leakage currents in tantalum capacitors.*

Excessive leakage currents in tantalum capacitors are often attributed to the presence of defects in the dielectric created by rupture of the tantalum pentoxide layer under high mechanical stresses [6]. Fagerholt [7] suggested that stresses applied to the part can drive sharp MnO\(_2\) crystals that exist in the manganese cathode layer to penetrate and impair the dielectric resulting in scintillations or increasing leakage currents in the capacitors.

Scintillations, or local breakdown terminated by conversion of the conductive MnO\(_2\) into a high-resistive Mn\(_2\)O\(_3\) phase due to local heat dissipation, result typically in high current spikes that were observed during our experiments. However, this mechanism cannot explain stabilization of leakage currents at a constant level of stress and their recovery after the stress is released.

Also, additional experiments (see Figure 8) showed that the effect of stress is not specific to the parts with manganese cathodes, but is also observed for capacitors with cathodes made of conductive polymers. This indicates that the stress-induced degradation of leakage currents was not related to the type of the cathode used but is a characteristic feature of the sintered tantalum/tantalum pentoxide system. A possible explanation for this phenomenon is stress-induced generation of electron traps that increases conductivity of the tantalum pentoxide.
dielectric in local areas where tantalum particles are in close proximity and create high compressive stresses.

Multiple studies have shown that the electron transport in Ta$_2$O$_5$ dielectrics is due either to a bulk-limited Poole-Frenkel conduction or to surface-barrier-limited Schottky mechanisms [8-11]. It is assumed that different conduction mechanisms can prevail in different ranges of voltage and temperature, and can vary depending on the treatment of the oxide (e.g. annealing conditions) [12-13]. Simmons proposed a modified Schottky mechanism according to which the current depends on the surface barrier level and mobility of electrons in the bulk of dielectric [14]. The surface-barrier-limiting mechanism is likely prevailing at relatively low electric fields, while a bulk-limiting mechanism is prevailing at high voltages [12, 15-16]. A detailed analysis of different conduction mechanisms in Ta$_2$O$_5$ dielectrics was performed by Novkovski and Atanassova [17]. Anodic tantalum oxide films have a disordered structure and a substantial amount of electron traps, up to $10^{19}$ cm$^{-3}$, so electron transport through the oxide at sufficiently large electric fields is commonly described as Poole-Frenkel conduction.

Our experimental data can be explained assuming that conduction is bulk-limited and increases with concentration of electron traps. Mechanical stresses result in formation of microscopic defects such as broken Ta-O bonds or generation of oxygen vacancies, increase the concentration of electron traps in the Ta$_2$O$_5$ dielectric and leakage currents in the capacitors. A similar mechanism related to the Si-O bond breaking due to physical stresses in silicon dioxide was used to explain factors affecting reliability of gate oxides in microcircuits [18-19].

The reversibility of the process of current degradation in capacitors can be explained assuming that the trap concentration is determined by a dynamic equilibrium of two concuring and competitive processes: generation of stress-induced defects and their annealing (e.g., recombination of the broken bonds). When the stress is removed, the concentration of the traps returns to its initial value and so does the leakage current. Both processes, generation under the stress and recombination after stress removal develop with time resulting in delays and hysteresis during stress cycling that was observed in our experiments.
Due to a sponge-like structure of the tantalum anode, the level of stress that causes trap generation in Ta$_2$O$_5$ dielectrics is likely much greater than the measured critical stress in the part. Repeat applications of compressive stresses after recovery of currents in some cases increased currents to a lesser degree. Assuming that the increased dielectric leakage current (DCL) is due to local areas with sufficiently high level of stress, a loss of the sensitivity to the stress might be due to some non-reversible deformations in the part or creeping that does not allow restoring the same level of local stresses as developed initially. However, for some capacitors the sensitivity increased during the following cycles. This behavior is also consistent with the time delay of stress-induced trap generation assuming that the level of the local stresses is the same and annealing of the traps was not completed during the relaxation period.

A trend of increasing of $\sigma_{cr}$ for parts with smaller size might be explained assuming that the stress-induced degradation of leakage currents is associated with the presence of some macro-structural defects in the parts, e.g. bumps or burrs on the surface of the tantalum slug. These macro-defects have high sensitivity to mechanical stresses, are relatively small and their size does not depend on the size of the part. In this case, capacitors with different size but similar defects would have close critical forces; however, the critical stress calculated as the ratio of the critical force and cross-sectional area of the part would be less for larger-size capacitors.

**Estimations of stresses caused by soldering onto PWBs**

During soldering of a capacitor onto a printed wiring board (PWB) both, the part and the board, are heated up to temperatures above the melting point of solder (typically to $\sim$ 230 °C for eutectic Sn/Pb solder) which solidifies when the system is cooled down to room temperature. Due to differences of the coefficients of thermal expansion between the part and PWB, mechanical stresses are building up as the temperature decreases below the point of solidification of solder. However, when the temperature remains above the glass transition temperature of the PWB, $T_{gPBW}$, the level of stresses is relatively low and for rough estimations we can assume that the stresses are formed only after temperature decreases below $T_{gPBW}$.

To estimate these stresses let us consider a schematic of a microchip tantalum capacitor soldered onto a PWB shown in Figure 9. For a simplified one-dimensional model, assuming that materials follow the Hookian’s law, and that the temperature variations of Young’s modulus, $E$, and CTE, $\alpha$, in the glassy state can be neglected, the compressive stress that develop in a soldered capacitor after cooling to room temperature, $T_r$, can be expressed as:

$$\sigma = \frac{(\alpha_{PWB} - \alpha_{cap}) \times (T_g - T_r)}{(E_{cap})^{-1} + \left(E_{PWB} \times \frac{A_{PWB}}{A_{cap}}\right)^{-1}},$$

(1)

where $A_{cap}$ and $A_{PWB}$ are the cross-sectional areas of the capacitor and PWB, and $E_{cap}$ and $E_{PWB}$ are the values of their effective Yang’s modulus.
Based on literature data [20] and results of our measurements, parameters of epoxy-based (FR4) and polyimide-based (PI) boards and microchip tantalum capacitors used for stress calculations are summarized in Table 4. The areas of the capacitor and board were calculated as a product of their thicknesses and widths, $A_{cap} = h_{cap} \times W_{cap}$ and $A_{PWB} = h_{PWB} \times W_{cap}$. Results of calculations per Eq.(1) for different part types and boards with the thickness 1/8 inch (3.175 mm) are presented in Table 5.

Table 4. Mechanical characteristics used for stress calculations.

<table>
<thead>
<tr>
<th>Characteristic</th>
<th>FR4</th>
<th>PI</th>
<th>microchip</th>
</tr>
</thead>
<tbody>
<tr>
<td>$T_g$, °C</td>
<td>145</td>
<td>230</td>
<td></td>
</tr>
<tr>
<td>$CTE$, ppm/°C</td>
<td>15</td>
<td>12.4</td>
<td>Per Table 3</td>
</tr>
<tr>
<td>$E$, GPa</td>
<td>17.5</td>
<td>23.5</td>
<td>10</td>
</tr>
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</table>

The stresses in the case of assembly of Mfr.B capacitors onto a polyimide board, which are typically used for space applications, are slightly greater compared to assembly onto FR4 board. Although the CTE mismatch is lower for PI board, a higher $T_g$ value for PI results in greater buildup stresses. However, in all cases soldering-related stresses are below the critical levels.

Negative stresses for Mfr.A capacitors (Gr.2 to Gr.4) assembled onto PI board indicate tensile stresses that are due to relatively large CTE for these parts that exceed CTE of polyimide. Tensile stresses create a danger of fractures in the attachment and open circuit failures.

The smallest size capacitors from Gr.7 have the greatest margin between the minimal observed critical stress (81.1 MPa) and the level of stresses that might be caused by soldering onto a PI board (~11 MPa). The minimal critical stress observed in Gr.2 parts, ~10 MPa, was still substantially below the level of stress expected after soldering onto FR4 board (~1 MPa). Note that even a twofold increase of the thickness of the board (to ¼ inch) only slightly, from 6% to 13%, raises the level of stresses in the capacitors. However, an increase in the Young’s modulus of capacitor from 10 GPa to 20 GPa would raise stresses on 60% to 80% thus substantially decreasing the margin between the critical and soldering-induced stresses.
Table 5. Calculated mechanical stresses in microchip capacitors.

<table>
<thead>
<tr>
<th>Gr.</th>
<th>W, mm</th>
<th>H, mm</th>
<th>CTE, ppm/°C</th>
<th>A_{cap}, m²</th>
<th>A_{PWB}, m²</th>
<th>σ_{FR4}, Mpa</th>
<th>σ_{PI}, Mpa</th>
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<tbody>
<tr>
<td>1</td>
<td>1.6</td>
<td>1.6</td>
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<td>0.85</td>
<td>6.6</td>
<td>7.23E-07</td>
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<td>9.0</td>
<td>10.6</td>
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More data on mechanical characteristics of microchip capacitors and additional analysis of the soldering-induced stresses are necessary to evaluate the possibility of degradation of the parts caused by soldering onto PWBs more accurately. Preliminary results discussed above show that for normal quality parts a sufficient margin exists between the critical level of stresses and stresses developed after soldering. However, for capacitors with macro-defects on the surface of the slug, the level of critical stresses might be low enough to degrade characteristics of the capacitors after soldering. A special care should be taken to assure the necessary margin in all lots of microchip capacitors used for high-reliability applications. To avoid failures, a qualification testing that includes measurements of leakage currents under a stress of 10 MPa is recommended.

**Conclusion**

1. Compressive stresses can result in increase of leakage currents in microchip tantalum capacitors up to three orders of magnitude. The level of critical stresses in different part types varies from 30 MPa to 140 MPa.

2. Similar to regular chip tantalum capacitors, stress-induced degradation in microchip capacitors is reversible: leakage currents increase gradually with the stress, remained relatively stable when the stress is stabilized, and then decrease as the stress lowered. The results are explained assuming bulk-limited Poole-Frenkel mechanism of conduction and stress-induced generation of electron traps that increases conductivity of the tantalum pentoxide dielectric. The processes of trap generation and their annealing develop with time resulting in hysteresis of the current-stress characteristics.

3. Thermo-mechanical characteristics (Tg and CTE) for parts from different vendors vary substantially from ~105 °C to ~ 150 °C (Tg) and from 6.1 ±0.5 ppm/°C to 13.2 ±1.3 ppm/°C (CTE). Considering that CTE for tantalum slugs is ~6.2 ppm/°C, different part types might experience different level of thermo-mechanical stresses during temperature excursions and have different reliability under temperature cycling conditions.
4. Analysis of mechanical stresses in microchips caused by the CTE mismatch between boards and capacitors showed that for both, polyimide and FR4 boards, the level of estimated stresses is relatively low, and for normal quality parts a sufficient margin exists between the critical level of stress and stresses developed after soldering.

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