Radiation Effects of Commercial Resistive Random Access Memories

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Acronyms

- 1T1R – 1 transistor 1 resistor
- BEOL – Back-end-of-line
- CBRAM – Conductive-bridge random access memory
- CMOS – Complimentary metal-oxide-semiconductor
- EEPROM – Electrically erasable programmable read only memory
- LCDT – Low cost digital tester
- LBNL – Lawrence Berkeley National Laboratory
- LET – Linear energy transfer
- RAM – Random access memory
- ROM – Read-only memory
- ReRAM – Reduction-oxidation random access memory
- RRAM – Resistive Random Access Memory
- SEE – Single-event effect
- SEFI – Single-event functional interrupt
- SEU – Single-event upset
- SOIC – Small Outline Integrated Circuit
- TAMU – Texas A&M University
Motivation

• Limited availability of radiation tolerant flash memories
• Radiation performance of state-of-the-art flash is generally good but include some weaknesses
• Flash already reaching scaling limits
• Resistive random access memory (RRAM) has shown very good tolerance to radiation*
• Published radiation test results only from test chips
• A first look at the SEE performance of two commercial production-level RRAMs


Panasonic Embedded ReRAM

- Panasonic MN101L
  - 16 bit microcontroller with embedded ReRAM
  - Industry’s first mass production-level ReRAM
- 1T1R array architecture, with CMOS transistor as access transistor to each ReRAM stack
- TaOₓ as switching layer
- Minimum device width ~ 0.5 µm
- Fabricated back-end-of-line in a 180 nm CMOS process

<table>
<thead>
<tr>
<th>Function</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Memory Size</td>
<td>64 KB</td>
</tr>
<tr>
<td>Program Endurance</td>
<td>Program area (62 KB): ≥ 10³</td>
</tr>
<tr>
<td></td>
<td>Data area (2 KB): ≥ 10⁵</td>
</tr>
<tr>
<td>Programming Voltage</td>
<td>1.8 to 3.6 V</td>
</tr>
<tr>
<td>Reading Voltage</td>
<td>1.1 to 3.6 V</td>
</tr>
<tr>
<td>Data Retention</td>
<td>10 years</td>
</tr>
</tbody>
</table>


ReRAM – Reduction-Oxidation Random Access Memory
1T1R – 1 transistor 1 resistor

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Heavy Ion Testing

- Kovar lid collimator (254 µm) exposed ReRAM array and peripheral control circuits
- Used Panasonic’s evaluation card as test vehicle
- ROM operating conditions: $V_{cc} = 3.3$ V, Frequency = 8 MHz or DC
- Test modes: static, dynamic read, read/compare/write, and write
- Data patterns: 00, FF, 55, and AA
- 15 MeV/amu heavy ions in air at Texas A&M University
- 16 MeV/amu heavy ions in vacuum at Lawrence Berkeley National Laboratory

ROM – Read-Only Memory
Heavy Ion Test Results

- No SEU from static test
  - 1 functional error following Xe irradiation, during read-back, recovered by a reset
- Dynamic read and write produced mostly SEFIs
  - 1 locked mode event
- Similar SEFI cross sections for read and write test mode
- Angular irradiation
  - Beam shadowing from the collimator likely contributed to reduced cross section

SEU – Single-Event Upset
SEFI – Single-Event Functional Interrupt
SEE Characteristics

- **Functional interrupts**
  - Microcontroller stops reading/writing
  - Flash vulnerable to large scale page and block errors

- **Bit upsets**
  - Include single-bit and multiple-bit upsets
  - Error address locations distributed throughout the microcontroller memory bank
  - 8 SEUs in the ROM

Pulsed-Laser Testing

- Pulsed-laser testing was carried out at the Naval Research Laboratory
- Laser characteristics
  - Wavelength = 590 nm
  - 1/e penetration range = 2 μm in silicon
  - Beam diameter = 1.7 μm for 20× lens, 0.9 μm for 100× lens
- We probed the ReRAM array and surrounding peripheral circuits with a 20× lens to identify the sensitive regions
- Sensitive areas were further investigated with a 100× lens, and the energy was fine-tuned to determine the upset energy threshold
- Equivalent LET values are based on empirical data from previous studies on other device types

LET – Linear Energy Transfer
Sensitive Locations

- **Energy ≈ 167 pJ**
  
  - (515 MeV·cm²/mg)

- **Energy ≈ 400 pJ**
  
  - (1200 MeV·cm²/mg)

- **Energy ≈ 37 pJ**
  
  - (115 MeV·cm²/mg)

- **Most sensitive region**
  
  - Energy ≥ 5.5 pJ
  
  - (17 MeV·cm²/mg)

- **No upset from the ReRAM array**

**Bit upsets**

- Did not originate from the ReRAM array
- Location sensitive to SEUs also susceptible to SEFIs

**Functional interrupt**

- Stops reading/writing
- Continuously reading out errors from the ROM
- Stuck reading at end of Bank0 (FFFF)
- Continuously reading errors from other address locations beside the ROM

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Upset Sensitivity in the Most Sensitive Location

- Determine upset energy threshold at the most sensitive location using 100× lens

- **Location 1:**
  - Read mode: 5.5 pJ (17 MeV·cm²/mg)
  - Write mode: 8.6 pJ (26.5 MeV·cm²/mg)

- **Location 2:**
  - Read mode: 71 pJ (220 MeV·cm²/mg)

- **Location 3:**
  - Read mode: 105 pJ (320 MeV·cm²/mg)
SEE Characteristics

- Compare SEE characteristics with heavy ion results
- Memory address of errors from laser test are similar to those from heavy ion test
- SEFI modes from laser and heavy ion test are also similar
  - Although limited information was gained from SEFIs that caused immediate cease of operation
- Sensitive region consists of sense amplifier circuit
  - SEU in the sensing circuit of flash devices lead to SEFI*


SF Register – Special function register
IO Register – Input/Output register
Adesto CBRAM

- 128 kb EEPROM from Adesto
- Ag/GeS2/W conductive bridge memory (CBRAM)
- 1T1R structure
- Back-end-of-line 130 nm CMOS

EEPROM – Electrically Erasable Programmable Read-Only Memory
Adesto CBRAM

- Heavy ion test carried out at LBNL in vacuum
- 8-pin SOIC packages were chemically etched to expose die
- 16 MeV/nuc cocktail
- Test conditions:
  - NASA’s LCDT tester
  - Vcc = 3.3 V
  - Frequency = 1 kHz or DC
  - Mode: static random read, static sequential read, continuous random read, write all/random read, write all/sequential read
  - Patterns: 00, FF, AA, and counter

DUT

LBNL – Lawrence Berkeley National Laboratory
SOIC – Small Outline Integrated Circuit
LCDT – Low Cost Digital Tester

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SEE Characteristics

- Static “On” and dynamic test modes produced mostly SEFIs
- Most (if not all) bit upsets due to acknowledgement fails, indicative of control circuit errors and not array errors
- SEFI modes
  - Stuck address, accumulating acknowledgement failures
    - Occurred during read and write/read test modes
    - Reset usually required
  - Read errors in continuous addresses
    - Column, page, or entire memory read out 00FF
    - Errors may clear by itself, or reset required
- No Apparent pattern sensitivity for FF, 00, AA, and Counter
SEE Characteristics

- Column errors (0000 to 000F) during read; memory still functional
SEE Characteristics

- Column errors (0000 to 00CF) during read; memory still functional
SEE Characteristics

- Entire memory reading 00FF during read
- Column errors (0000 to 00CF) during read
- Stuck at single address; reset required
SEE Characteristics

Irradiated with 16 MeV/nuc heavy ions
Frequency = 100 kHz, $V_{cc} = 3.6$ V

Cross Section (cm$^2$/device)

Effective LET (MeV·cm$^2$/mg)

- Black square: Read
- Red circle: Write/Random Read
- Blue triangle: Write/Sequential Read
Conclusion

• RRAM array immune to heavy ions with LET as high as 75 MeV·cm²/mg
  – SEU in CMOS access transistor not enough to cause bit flip
• SEFI is the dominant error mode
  – Panasonic MN101L embedded ReRAM’s SEFIs originate from sense amplifier circuits
  – Adesto CBRAM showed column/page errors, mass read errors from entire memory, and stuck address errors
• Lack of charge pump reduces sensitivity to erase or program failure
  – Eliminates block erase failures (issue for flash)