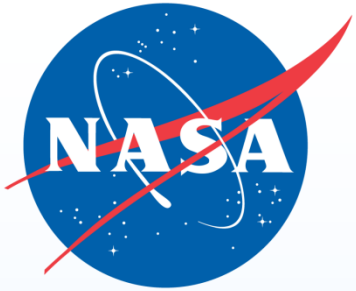
NEPP Electronic Technology Workshop
17-19 June 2014

National Aeronautics
and Space Administration



Advanced CMOS Radiation Effects Testing & Analysis

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Acronyms

- CMOS: complementary metal oxide semiconductor
- CNL: Crocker Nuclear Laboratory
- DBU: double-bit upset
- DUT: device under test
- EDAC: error detection and correction
- (e)DRAM: (embedded) dynamic random access memory
- FET: field-effect transistor
- FY: fiscal year
- IBM YKT: IBM Yorktown Heights, NY
- ICRU: International Commission on Radiation Units & Measurements
- IEEE: Institute of Electrical and Electronics Engineers
- IUCF: Indiana University Cyclotron Facility
- LBNL: Lawrence Berkeley National Laboratory
- LEP: low-energy proton
- LET: linear energy transfer
- MCU: multi-cell upset (errors not necessarily in the same data word)
  - Different from multi-bit upset (MBU)
- NIST: National Institute of Standards and Technology
  - ASTAR and PSTAR are NIST tools, not acronyms
- NPTC: Northeast Proton Therapy Center
- NSREC: Nuclear and Space Radiation Effects Conference
- RHBD: radiation hardened by design
- SBU: single-bit upset
- SEE: single-event effect(s)
- SEU: single-event upset
- SET: single-event transient
- SOI: silicon on insulator
- SRAM: static random access memory
- TAMU: Texas A&M University
- TID: total ionizing dose
- TNS: Transactions on Nuclear Science
- TRIUMF: not an acronym – formerly the Tri-University Meson Facility, Vancouver, Canada
- TSMC: Taiwan Semiconductor Manufacturer
- UC Davis/UCD: University of California, Davis

Goals

- **Assess advanced CMOS processes for space applications**
  - To date we have investigated or are making plans to evaluate radiation effects at the 180, 90, 65, 45, 32, 28, and 22 nm technology nodes.
- **Develop and maintain relationships with advanced CMOS fabrication companies and fabless suppliers**
  - To date we have partnered with Cisco & Robust Chip, Cyprus Semiconductor, IBM, Intel, Jazz Semiconductor, and Texas Instruments.
- **Investigate SEE/TID susceptibility of leading-edge technology nodes**
  - Since last year, we have focused on IBM 32 nm SOI CMOS and have plans to move to the IBM 14 nm SOI FinFET process.
- **Understand SEE/TID mechanisms to enable/validate radiation hardening**
- **Work with government agency partners and their programs**

Thank you to all manufacturers who have partnered with us over the years to provide critical insights to the radiation effects and aerospace communities.

Overview

- **IBM 32 nm SOI CMOS evaluation (SEE/TID)**
  - 128 Mb SRAM test vehicle
  - 128 Mb eDRAM test vehicle
  - SET pulse width measurement test vehicle
- **IBM 14 nm SOI FinFET evaluation (SEE/TID)**
  - Planning to transition to 14 nm technology evaluation by the end of FY2014.
- **Other plans for 2014-2015**
  - Forming collaboration with Cisco & Robust Chip to investigate SEE in TSMC 28 nm CMOS.

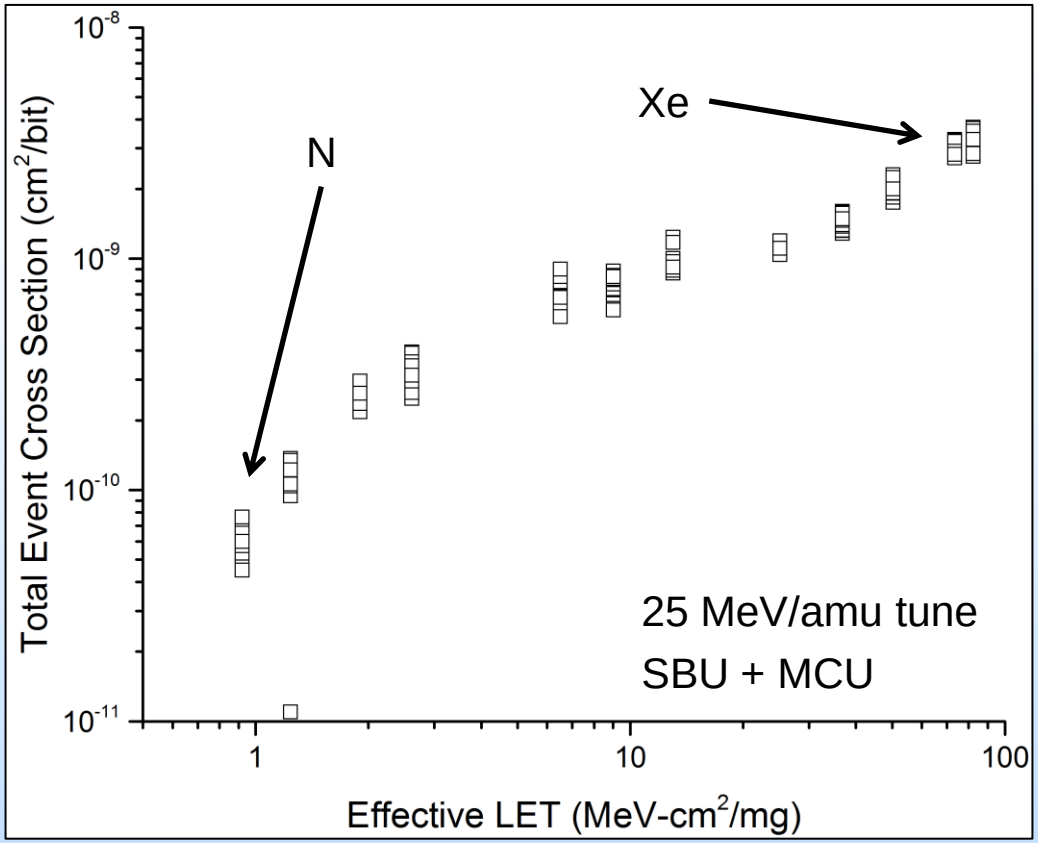
IBM SOI CMOS Devices

128 Mb SRAM Line Monitor in CMOS13S (32 nm SOI)

- Radiation Effects Evaluation
  - SEE
    - LBNL: 01/2013
    - TAMU: 05/2013
    - UCD: 11/2013
- ***Stay tuned for presentation at 2014 NSREC (Pellish et al.)***

- **Similar in design to 45 nm SOI SRAM tested during FY09 – FY10.**
- **Flip-chip land grid array required mechanical grinding and polishing with UltraTec vertical mill.**
  - Test sample was thinned from ~800 um to < 120 um.

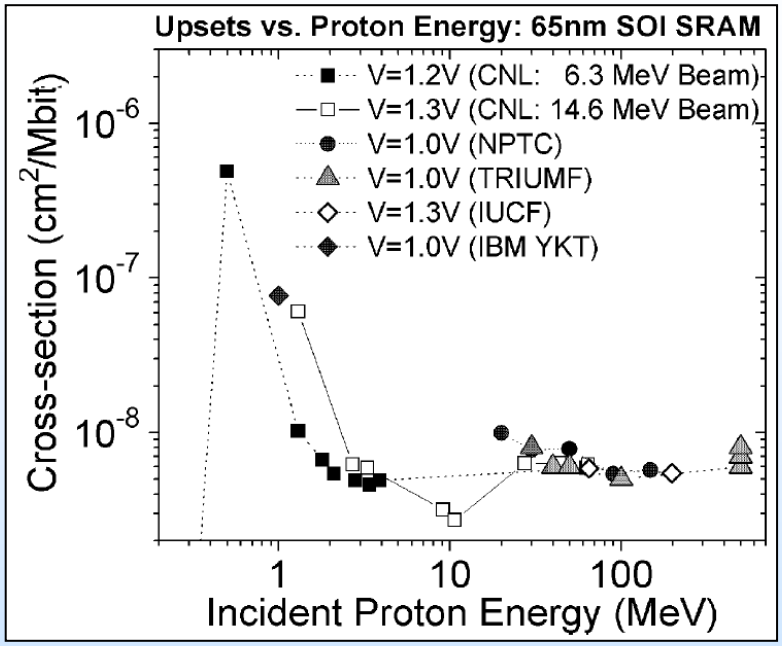
IBM 32 nm SOI SRAM – Heavy Ion SEE



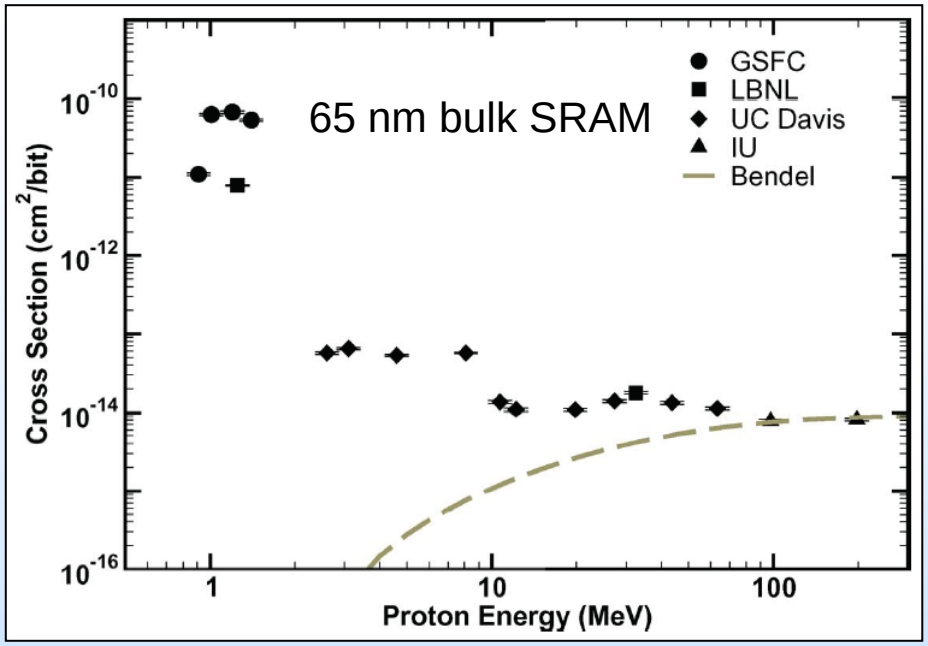
Error bars are smaller than data points.

- **Conducted primary SEE evaluation at TAMU in the summer of 2013.**
- **Response typical of other unhardened advanced CMOS technologies.**

Early Low-Energy Proton (LEP) Data



D. F. Heidel et al., IEEE TNS, vol. 6, 2008.



B. D. Sierawski et al., IEEE TNS, vol. 6, 2009.

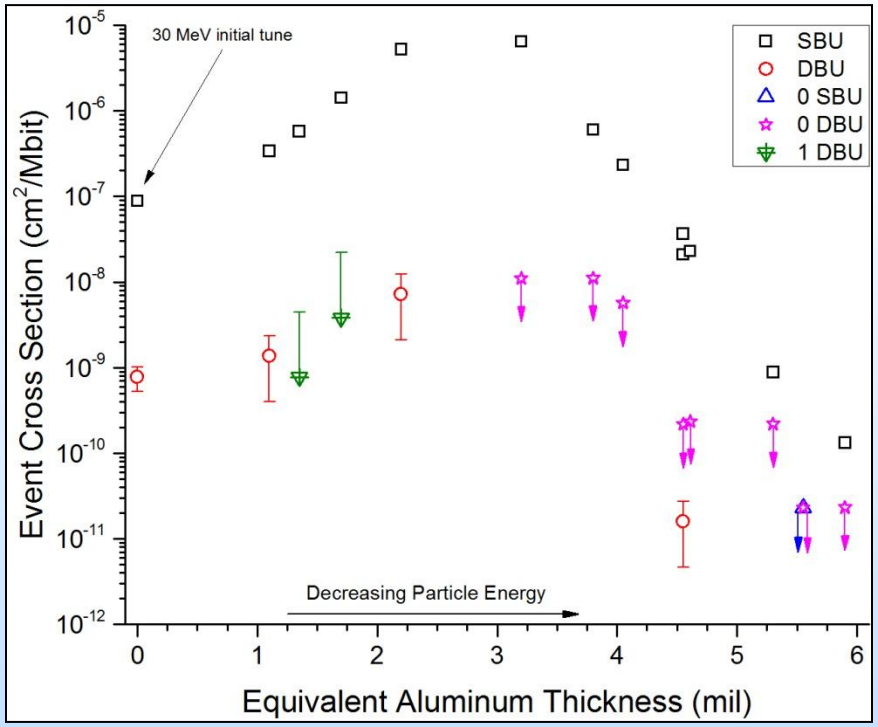
- **First documented in 2007 (K. P. Rodbell et al., *IEEE TNS*, vol. 6, 2007).**
- **Important for hardness assurance.**

IBM 32 nm SOI SRAM – LEP SEE

- **Used 6.5 MeV protons and 30 MeV alpha particles.**
  - Aimed to perform direct proton/alpha particle comparison.
  - Previous data (65, 45, and 32 nm SOI) were inconclusive, but hinted at potential hardness assurance issues.
- **All irradiation conducted in-air at normal incidence and room temperature.**
- **Used a range of blanket, logical, and physical data patterns.**
  - 0, 1, logical checkerboard, and physical checkerboard.
  - Only reporting blanket 0 and 1 pattern data here
- **Used standard array voltage of 1.05 V.**

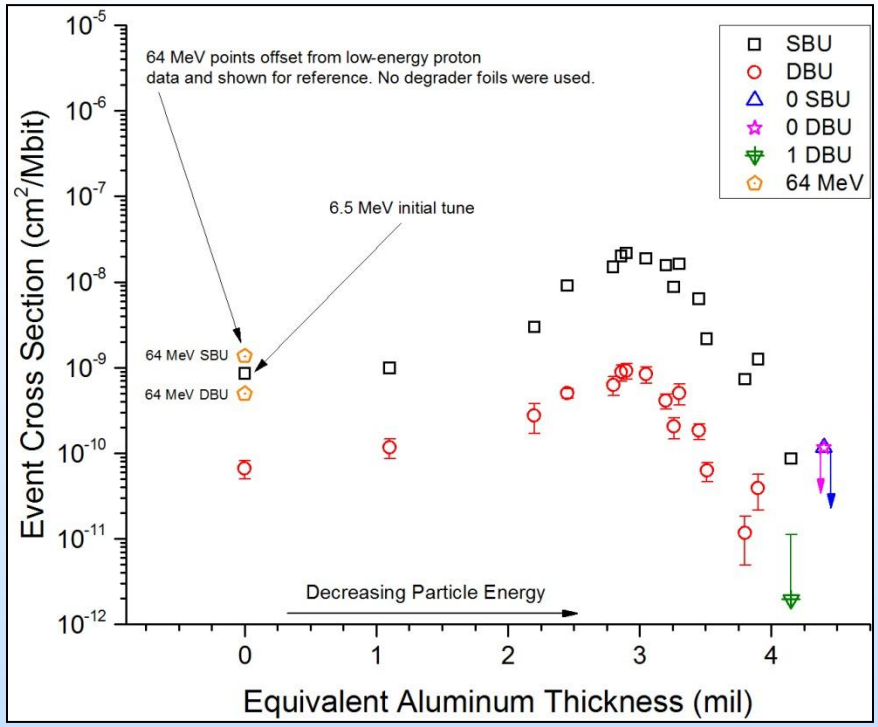
IBM 32 nm SOI SRAM – LEP SEE

Alpha



J. A. Pellish, et al., 2014 SEE Symposium, La Jolla, CA, May 2014.

Proton



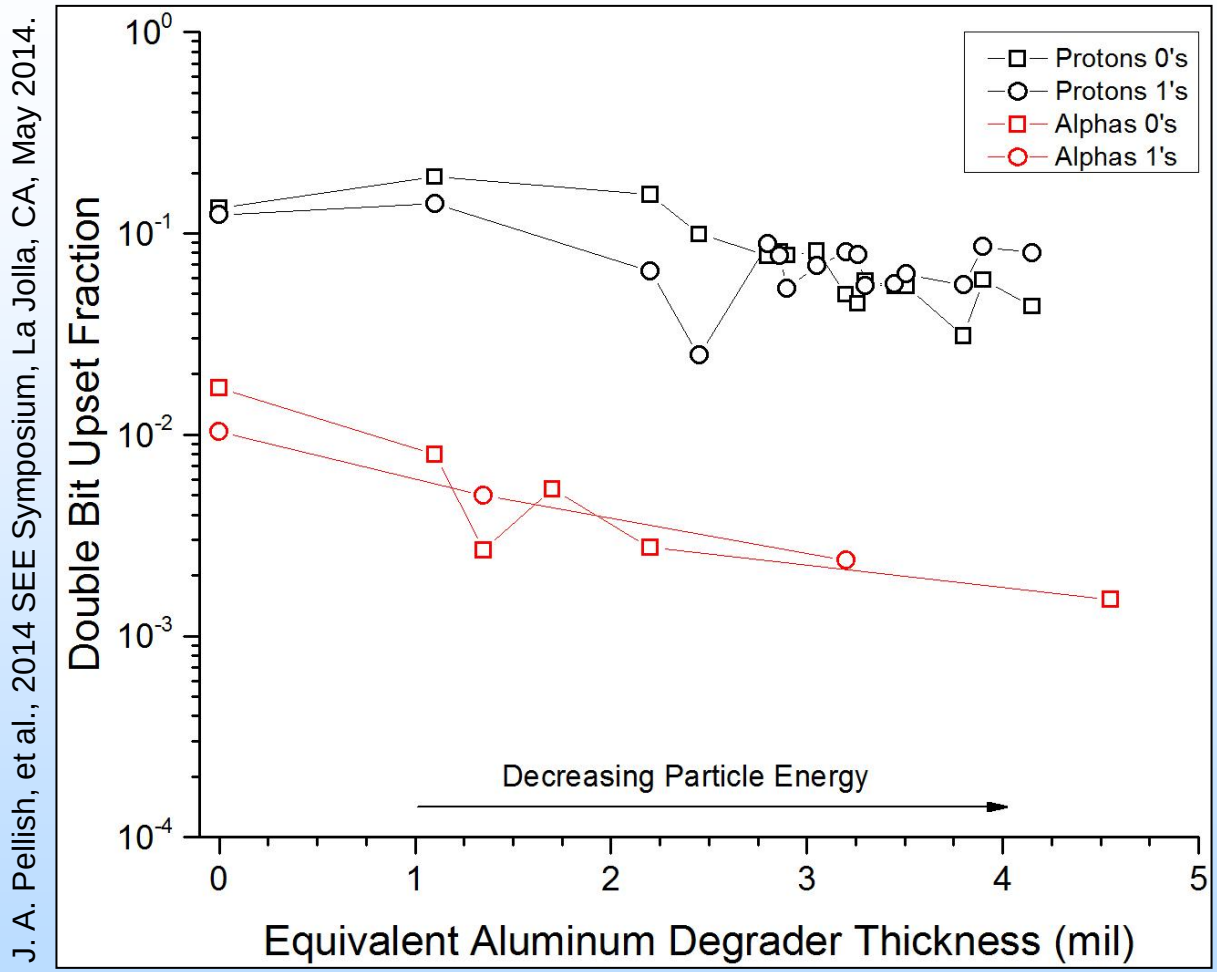
J. A. Pellish, et al., 2014 SEE Symposium, La Jolla, CA, May 2014.

- **On the low-energy side of the Bragg peak, the cross sections are similar, but the type of events are not.**
- **One of the key features is the separation between SBUs and DBUs.**

LEP Data Discussion Points

- Green triangles represent 1 DBU. Error bars are at the 90% confidence level.
- Blue triangles and magenta stars are limiting cross sections. Data symbols are at the upper 90% confidence level.
- Cross sections are given as a function of degrader thickness because data reduction is still ongoing.
  - Will subsequently determine whether the peak in the SBU cross section coincides in energy with alphas/protons of maximum LET.
- At this point, we have not taken into account induced flux loss of the incident alphas/protons when computing the cross sections.
  - We expect flux loss to elevate the low-energy cross sections.

IBM 32 nm SOI SRAM – LEP SEE



Shows both 0x0000 and 0xFFFF data patterns; includes multiplicity of DBU events.

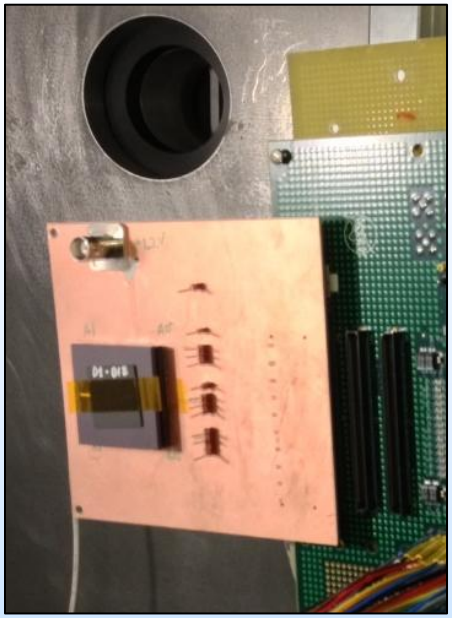
Alpha & Proton DBU Fraction

IBM 32 nm SOI SRAM – LEP SEE

- **Proton/Alpha Conclusions**
  - Data have added a new wrinkle to radiation hardness assurance issues with ultra deep submicron processes.
    - Suggests that there may be an additional mechanism present with low-energy proton upsets – not just direct ionization by a *constant trajectory* primary.
    - This mechanism must be explored with detailed physical modeling and, potentially, additional data collection.
    - Likely means that light heavy ions cannot be used as a 1:1 test surrogate for low-energy protons in all cases. This may work for studying single-bit upsets, but if multiple-bit effects are important (*e.g.*, RHBD, EDAC, *etc*.), then low-energy protons may be necessary for full understanding.
  - **Additional investigations**
    - Sandia National Labs is pursuing a LEP evaluation technique using degraded proton beams. For more information, contact Nathaniel Dodds and refer to his papers at the 2014 SEE Symposium and 2014 IEEE NSREC.

IBM SOI CMOS Devices

SET pulse width measurement macro in CMOS13S (32 nm SOI)

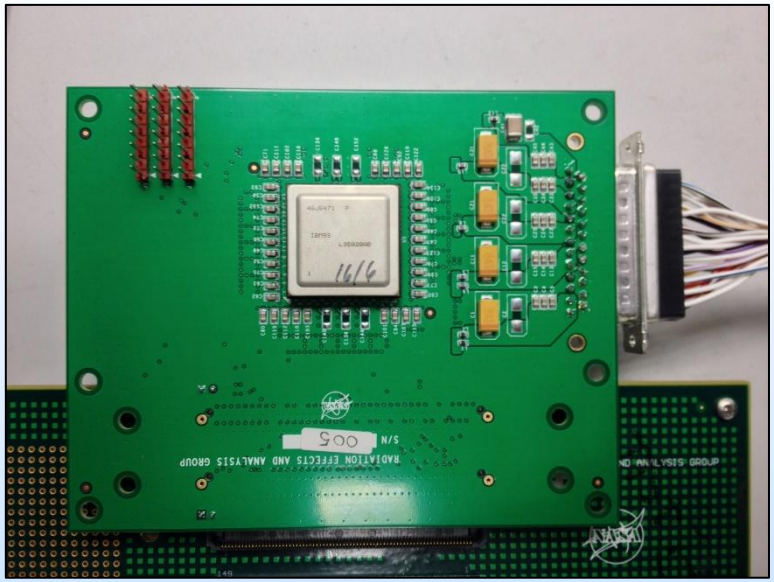


- Radiation Effects Evaluation
  - SEE
    - LBNL: 09/2013
    - LBNL: 05/2014
- ***Stay tuned for presentation at 2014 NSREC (Rodbell et al.)***

- **Measures SET pulse width based on stage delay.**
  - Designed using concepts laid out in B. Narasimham et al., “On-Chip Characterization of Single-Event Transient Pulsewidths,” *IEEE Trans. Device Mater. Rel.*, vol. 6, no. 4, pp. 542-549, Dec. 2006.
- **Meant to act as a companion to a companion design, which measures the effect of SETs at the system level by allowing measurement of SETs that are captured as SEUs.**

IBM SOI CMOS Devices

128 Mb eDRAM Line Monitor in CMOS13S (32 nm SOI)



- Radiation Effects Evaluation
  - TID
    - GSFC: 07/2014 (planned)
  - SEE
    - Not currently in scope

- **New type of test chip – we have not previously evaluated embedded DRAM, but it is a critical feature of the IBM 32 nm SOI process.**
- **Sample to undergo TID testing.**
- **If we choose to pursue heavy ion testing, the flip-chip land grid array will required mechanical thinning.**

Summary

- **Continuing to investigate radiation effects in the latest CMOS technology nodes.**
- **Focusing on aerospace applications and the natural space radiation environment.**
- **Evaluating both single-event and total dose effects.**
  - **IBM 32 nm SRAM (heavy ion and LEP SEE)**
  - **IBM 32 nm eDRAM (TID)**
  - **IBM 32 nm latches (heavy ion SEE)**
- **Starting migration to IBM 14 nm SOI FinFETs this fall.**

Acknowledgements

- IBM Corp.
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- NASA Electronic Parts and Packaging Program
- Defense Threat Reduction Agency
- National Reconnaissance Office