

1. SCOPE

1.1 Purpose. This specification defines the requirements for high reliability, ceramic dielectric, multilayer, base-metal electrodes, fixed value, chip capacitors for high reliability space applications. It defines the processing verification and inspections required by assemblies used in flight.

1.2 Part or Identifying Number (PIN). The complete PIN for the capacitors supplied to this specification shall be specified per Table I. Allowable combinations of voltage, capacitance, dielectric type, and package size as described in Table II herein.

1.3

Table I: Part or Identifying Number

GSFC Identifier	Ultrasonic Examination	Size Code	Dielectric Type	Capacitance	Tolerance	Voltage (Vdc)	Termination	Packaging/Marking
S311P838	A = 100%	A = 0402 B = 0603 C = 0805 D = 1206 E = 1210 F = 1812	X = X7R	XXX Capacitance in picofarads where third digit is number of zeros: eg 103 equals 10,000pF	J = ±5% K = ±10% M = ±20%	1 = 25V 2 = 50V 3 = 100V 6 = 16V	R = Sn/Pb plated	1 = T/R unmarked capacitors 2 = T/R marked capacitors 3 = Waffle Pack, unmarked capacitors 4 = Waffle Pack, marked capacitors

Table II. Allowable Capacitance/Voltage Combinations

Component Size	Capacitance Range (pF)	Rated Voltage (V _R)	Minimum Dielectric Thickness ^{1/} in (mils)	Tolerance (+/-) (%)
0603	2,200 to 18,000	100	0.60	5, 10, 20
0603	2,200 to 150,000	50	0.33	5, 10, 20
0603	2,200 to 180,000	16, 25	0.28	5, 10, 20
0805	2,200 to 100,000	100	0.60	5, 10, 20
0805	2,200 to 470,000	50	0.33	5, 10, 20
0805	2,200 to 1,000,000	16, 25	0.28	5, 10, 20
1206	18,000 to 390,000	100	0.60	5, 10, 20
1206	18,000 to 1,000,000	50	0.33	5, 10, 20
1206	18,000 to 2,200,000	16, 25	0.28	5, 10, 20
1210	47,000 to 820,000	100	0.60	5, 10, 20
1210	47,000 to 1,000,000	50	0.33	5, 10, 20
1210	47,000 to 1,000,000	16, 25	0.28	5, 10, 20
1812	150,000 to 2,200,000	100	0.60	5, 10, 20
1812	150,000 to 4,700,000	50	0.33	5, 10, 20
1812	150,000 to 8,200,000	16, 25	0.28	5, 10, 20

^{1/} Thickness measured after firing

- 1.3.1 Ultrasonic Examination. Devices supplied to this specification shall be subjected to ultrasonic examination in accordance with the manufacturer's standard procedures, except as modified herein. Ultrasonic examination may be performed prior to capacitor termination (in accordance with [MIL-PRF-123](#) requirements) or after capacitor termination, at the manufacturer's option.
- 1.3.2 Dielectric Type. The voltage temperature characteristic shall be referenced to the +25°C value, applicable over the entire temperature range of -55°C to +125°C, and ±15% of capacitance.
- 1.3.3 Termination. Devices supplied to this specification shall have a termination coating of base metal with a flexible layer, nickel barrier, tin-lead solder plated. Tin lead solder plating shall contain a minimum of 3% lead by mass.
- 1.3.4 Package/Marking. Capacitors supplied to this specification greater than chip size 0603 shall be marked with the manufacturer's identifier code. The complete GSFC PIN shall be marked on packaging and certifications. Capacitors shall be packaged on tape and reel (identifier code 1 for unmarked, code 2 for marked) or in waffle packs (identifier code 3 for unmarked and code 4 for marked).
- 1.3.5 Unit Conversion. The unit used in this documentation is in British system. When converting to metric system the number should be multiplied by 25.4.

2. APPLICABLE DOCUMENTS

- 2.1 Government Specifications, Standards, and Handbooks. The following Government specifications, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those listed in the issue of the Department of Defense Index of Specifications and Standards (DoDISS) and supplement thereto, in effect on the date of the contract or purchase order.

STANDARDS

Military

[MIL-STD-202](#)

Test Method Standard Electronic and Electrical Component Parts

SPECIFICATIONS

Military

[MIL-PRF-123](#)

Capacitors, Fixed, Ceramic Dielectric, (Temperature Stable and General Purpose), High Reliability, General Specification

National Aeronautics and Space Administration (NASA)

[EEE-INST-002](#)

Instructions for EEE Parts Selection, Screening, Qualification, and Derating

[S-311-M-70](#)

Specification for the Performance of Destructive Physical Analyses (DPA)

- 2.2 Non-Government Publications. The following documents form a part of this document to the extent specified herein. Unless otherwise specified, the issues of the documents which are DoD adopted are those listed in the issue of the DoD ISS in effect on the date of the contract or purchase order. Unless otherwise specified, the issues of documents not listed in the DoD ISS are the issues of the documents in effect on the date of the contract or purchase order.

American National Standards Institute (ANSI)

ANSI/NCSL Z540.3-2007

General Requirements for Calibration Laboratories and Measuring and Test Equipment

ANSI/ISO/IEC 17025:2005

General Requirements for the Competence of Testing and Calibration Laboratories

Automotive Electronics Council (AEC)

AEC-Q200-005

Board Flex Test

American Society for Testing and Materials (ASTM)

ASTM E112-10

Standard Test Methods for Determining Average Grain Size

Electronic Components Industry Association (ECIA)

EIA/ECA-469

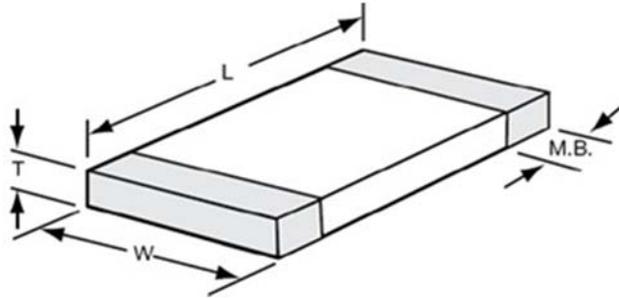
Standard Test Method for Destructive Physical Analysis (DPA) of Ceramic Monolithic Capacitors

- 2.3 Order of precedence. In the event of a conflict between the text of this document and the references cited herein (except for related associated specifications, specification sheets, or MS sheets), the text of this document takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained from the procuring activity.

3. REQUIREMENTS

- 3.1 Individual Item Requirements. Individual item requirements for capacitors supplied to this specification shall be in accordance with the requirements as specified herein, under all combinations of environmental conditions specified herein.

- 3.1.1 Electrodes. All capacitors supplied to this specification shall be manufactured with nickel electrodes.
- 3.1.2 Pure Tin. The use of pure tin, as an underplate or final finish, is prohibited both internally and externally. Tin content of capacitor components and solder shall not exceed 97%, by mass. Tin shall be alloyed with a minimum of 3% lead, by mass.
- 3.1.3 Interface Requirements. Capacitors supplied to this specification shall meet the physical dimension requirements as specified in Figure 1 herein.



Size	Length L in mm (inches)	Width W in mm (inches)	Thickness Max T in mm (inches)	Metallization Band M.B. in mm (inches)
0402	1.016 ± 0.102 (0.040 ± 0.004)	0.508 ± 0.102 (0.020 ± 0.004)	0.610 (0.024)	0.102 (0.004) Min. Band 0.381 (0.015) Min. Space
0603	1.600 ± 0.152 (0.063 ± 0.006)	0.813 ± 0.152 (0.032 ± 0.006)	1.016 (0.040)	0.127 (0.005) Min. Band 0.635 (0.025) Min. Space
0805	2.032 ± 0.254 (0.080 ± 0.010)	1.270 ± 0.254 (0.050 ± 0.010)	1.524 (0.060)	0.508 ± 0.254 (0.020 ± 0.010)
1206	3.200 ± 0.203 (0.126 ± 0.008)	1.600 ± 0.203 (0.063 ± 0.008)	1.803 (0.071)	0.508 ± 0.254 (0.020 ± 0.010)
1210	3.200 ± 0.203 (0.126 ± 0.008)	2.499 ± 0.254 (0.098 ± 0.010)	2.794 (0.110)	0.508 ± 0.254 (0.020 ± 0.010)
1812	4.572 ± 0.381 (0.180 ± 0.015)	3.175 ± 0.381 (0.125 ± 0.015)	2.794 (0.110)	0.610 ± 0.356 (0.024 ± 0.014)

Figure 1: Mechanical Configuration

- 3.2 Process Reliability Verification Test (PRVT) Requirements. Each capacitor lot supplied to this specification shall be tested to and meet the PVRT requirements of paragraph 4.4 herein. Any lot that does not meet these requirements shall not be delivered against this specification.
- 3.2.1 Construction/Microstructure Requirements. Capacitors tested as specified in paragraph 4.4.1 herein shall meet the following requirements.

3.2.1.1 Average Dielectric Thickness: Capacitors rated below 50Vdc shall be no less than the minimum dielectric thickness requirement of (0.28 mils) Voids, or the cumulative effect of voids shall not reduce the total dielectric thickness by more than 30%.

3.2.1.2 Side Margin Requirements. For capacitors rated at < 25 V, side margins shall be (0.6 mils), minimum. Capacitors rated at ≥ 25 V shall be 1.0 mil, minimum.

3.2.1.3 End Margin Requirements. For capacitors rated at < 25 V, end margins shall be 25μm (1 mil), minimum. Capacitors rated at ≥ 25 V shall be 1.6 mil, minimum.

3.2.1.4 Cover Plate Thickness Requirements. For capacitors rated at < 25 V, cover plate thickness shall be (1.0 mil), minimum. Capacitors rated at ≥ 25 V shall be 1.6 mil, minimum.

3.2.1.5 Dielectric Layers. The maximum number of dielectric layers per capacitor body shall be ≤ 300 layers.

3.2.1.6 Average Grain Size: Capacitors shall be measured for average grain size as specified in paragraph 4.4.2.

3.2.2 BME Capacitor Acceptance Criterion. Capacitor samples, processed as specified in paragraphs 4.4.1 and 4.4.2 herein and meeting the requirements of paragraph 3.2.1 herein, shall meet Equation 1 as shown below:

$$F_t = 1 - R_t = 1 - \left[1 - \left(\frac{\bar{r}}{d} \right)^\alpha \right]^N < 0.00001 \text{ Equation 1}$$

Where \bar{r} is the measured average grain size, d is the average dielectric thickness, N is the total number of dielectric layers, $\alpha = 5$ for capacitors rated voltage > 100V and $\alpha=6$ for capacitors rated voltage ≤ 100V.

3.3 Insulation Resistance (IR @ 125°C). Capacitors tested as specified in paragraph 4.6.3 herein shall have a minimum IR measurement of 10,000 Megohms or 100 Megohm-Microfarads, whichever is greater.

3.4 Dielectric Withstanding Voltage (DWV). Capacitors tested as specified in paragraph 4.6.4 herein shall exhibit no physical damage or breakdown.

3.5 Insulation Resistance (IR @ 25°C). Capacitors tested as specified in paragraph 4.6.5 herein shall have a minimum IR measurement of 100,000 Megohms or 1,000 Megohm-Microfarads, whichever is greater.

3.6 Capacitance. Capacitors tested as specified in paragraph 4.6.6 herein shall be within the tolerance specified by the PIN per Table I.

3.7 Dissipation Factor (DF). Capacitors tested as specified in paragraph 4.6.7 herein shall have the dissipation factor ≤ 3.5% at the 16 and 25 volt ratings and ≤ 2.5% at the 50 and 100 volt ratings.

- 3.8 Percent Defective Allowable (PDA). When calculated per paragraph 4.6.8 herein, the cumulative PDA for failures from Voltage Conditioning and Insulation Resistance at 125°C shall be $\leq 5\%$.
- 3.9 Visual Examination. Capacitors visually inspected as specified in paragraph 4.6.9 herein shall meet the requirements as specified in MIL-PRF-123, Appendix B.
- 3.10 Thermal Shock. Capacitors tested as specified in paragraph 4.6.1 herein shall exhibit no physical damage after completion of the specified thermal shock cycles. For Group A inspection, the number of cycles shall be twenty (20). For Group B inspection, the number of cycles shall be one hundred (100).
- 3.11 Voltage Conditioning. Capacitors shall be tested as specified in paragraph 4.6.2 herein.
- Insulation resistance (at +125°C): Capacitors tested as specified in paragraph 4.6.3 herein shall be not less than the initial requirement.
 - Dielectric withstanding voltage (at +25°C): Capacitors tested as specified in paragraph 4.6.4 herein shall meet the requirement as specified in paragraph 3.4.
 - Insulation resistance (at +25°C): Capacitors tested as specified in paragraph 4.6.5 herein shall be not less than the initial requirement.
 - Capacitance (at +25°C): Capacitors tested as specified in paragraph 4.6.6 herein shall be within the tolerance specified as specified in Table I.
 - Dissipation factor (at +25°C): Capacitors tested as specified in paragraph 4.6.7 herein shall not exceed the values as specified in paragraph 3.7.
- 3.12 Life Test. Life test shall be performed as specified in paragraph 4.7.1. If the dielectric thickness is ≥ 0.8 mils, sample size shall be forty-five (45) capacitors. If the dielectric thickness is < 0.8 mils, sample size shall be one hundred, twenty-five (125) capacitors. For Group B, test duration shall be 1,000 hours. For Product Development Certification per paragraph 4.2.1, test duration shall be 4,000 hours. Capacitors shall meet the following requirements at the test points specified.

250-hour test point:

- Insulation Resistance (at +125°C): Paragraph 4.6.3; Measurement shall be $\geq 5,000$ Megohms or 50 Megohm-Microfarads, whichever is greater.
- Visual Examination: Paragraph 4.6.9; No mechanical damage shall be evident. Marking shall remain legible (if applicable).
- Insulation Resistance (at +25°C): Paragraph 4.6.5; Measurement shall be $\geq 50,000$ Megohms or 500 Megohm-Microfarads, whichever is greater.
- Capacitance: Paragraph 4.6.6; Measurement shall be $\leq \pm 15\%$ from the initial measured value (Group A post-voltage conditioning).
- Dissipation Factor: Paragraph 4.6.7; Measurement shall not exceed $\leq 3.5\%$ at the 16 and 25 volt ratings and $\leq 2.5\%$ at the 50 and 100 volt ratings.

1,000-hour, 2,000-hour, and 4,000-hour test points:

1. Insulation Resistance (at +125°C): Paragraph 4.6.3; Measurement shall be $\geq 3,000$ Megohms or 30 Megohm-Microfarads, whichever is greater.
2. Visual Examination: Paragraph 4.6.9; No mechanical damage shall be evident. Marking shall remain legible (if applicable).
3. Insulation Resistance (at +25°C): Paragraph 4.6.5; Measurement shall be $\geq 30,000$ Megohms or 300 Megohm-Microfarads, whichever is greater.
4. Capacitance: Paragraph 4.6.6; Measurement shall be $\leq \pm 20\%$ from the initial measured value (Group A post-voltage conditioning).
5. Dissipation Factor: Paragraph 4.6.7; Measurement shall not exceed $\leq 3.5\%$ at the 16 and 25 volt ratings and $\leq 2.5\%$ at the 50 and 100 volt ratings.

- 3.13 Temperature-Humidity Bias. Capacitors shall be tested as specified in paragraph 4.7.2 herein. For Group B, test duration shall be 96 hours minimum. For Product Development Certification per paragraph 4.2.1, test duration shall be 1000 hours minimum. Post-test Insulation Resistance shall be $\geq 30\%$ of the Initial Insulation Resistance at 25°C as specified in paragraph 3.5.
- 3.14 Solderability. Capacitors tested as specified in paragraph 4.7.3 herein shall have zero (0) failures. The immersed metallized surface shall be at least 85% covered with a smooth solder coating. The remaining 15% of the surface may contain small pinholes or exposed termination material; however, these shall not be concentrated in one area. In case of dispute, the percent coverage with pinholes or exposed termination material shall be determined by actual measurement in these areas, as compared to the total area.
- 3.15 Resistance to Soldering Heat. Capacitors tested as specified in paragraph 4.7.4 herein shall meet the following requirements. There shall be no evidence of mechanical damage or delamination or exposed electrodes. Dissolution of metallization over unsolderable base material shall be a maximum of 25% on each edge of mounting area (reference MIL-PRF-123, Figure 2).
- a. Insulation Resistance at +25°C: Capacitors tested as specified in paragraph 4.6.5 herein shall not be less than the initial measured value at +25°C.
 - b. Capacitance: Capacitors tested as specified in paragraph 4.6.6 herein shall change not more than -1.0 % to +6.0 % from the initial measured value.
 - c. Dissipation Factor: Capacitors tested as specified in paragraph 4.6.7 herein shall not exceed the initial values.
- 3.16 Shear Stress. Capacitors mounted and tested as specified in paragraph 4.7.5 herein. Post-test visual inspection shall show no evidence of cracking or the capacitor being sheared from its pad.
- 3.17 Breakdown Voltage Test. Capacitors tested as specified in paragraph 4.7.6 herein shall have zero (0) failures at less than 6X rated voltage. A failure is defined as a steady state current of 5 mA. For Product Development Certification per paragraph 4.2.1, sample size shall be thirty (30) capacitors with zero failures.

3.18 Board Flex Test. Capacitors tested as specified in paragraph 4.7.7 herein shall meet the following requirements.

a. Post-test capacitance change shall be $\leq \pm 10\%$.

b. Dissipation Factor shall be $\leq 3.5\%$ at the 16 and 25 volt ratings and $\leq 2.5\%$ at the 50 and 100 volt ratings.

c. Capacitors shall not exhibit any visual damage to device body, terminals, and body/terminal junction.

3.19 In-Process Inspection Requirements. Each capacitor lot supplied to this specification shall be tested to and meet the In-Process requirements of paragraph 4.5 herein. Any lot that does not meet these requirements shall not be delivered.

4. QUALITY ASSURANCE PROVISIONS

4.1 Responsibility for Inspection. Unless otherwise specified in the contract purchase order, the manufacturer of ceramic capacitors supplied against this specification shall be responsible for the performance of all inspection requirements as specified herein. The procuring activity shall retain the right to perform any of the inspections specified herein, where such inspections are deemed necessary to assure that supplies and services conform to prescribed requirements.

4.1.1 Test Equipment and Inspection Facilities. The manufacturer shall keep test and measuring equipment and inspection facilities with sufficient accuracy, quality, and quantity to permit performance of the required inspections specified herein. The establishment and maintenance of a calibration system to control the accuracy of the measuring and test equipment shall be in accordance with ANSI/NCSL Z540.3 and ANSI/ISO/IEC 17025, or similar system approved by the procuring activity.

4.2 Design and Source Approval. Prior to Product Development Certification, the manufacturer's facility may be subjected to survey, at the option of GSFC. Compliance with ANSI/NCSL Z540.3, ANSI/ISO/IEC 17025 or equivalent is required. In addition, the history and detailed engineering of the specific (part) design shall be reviewed, as well as the documented manufacturing and quality control procedures. Only those source(s) approved in the design and source phase shall be eligible for lot acceptance test or award of contract under this specification. Source approval and design approval do not constitute part lot acceptance test or an equivalent thereof.

4.2.1 Product Development Certification (PDC). Capacitors furnished to this specification shall be the product which meets all of following tests:

Table III: Product Development Certification Inspections

Inspection	Requirement Paragraph	Method Paragraph
Process Reliability Verification Test	3.2	4.4
In-Process Inspection	3.19	4.5
Group A Inspection		4.6
Group B Inspection with PDC Requirements		4.7

All testing data shall be reviewed and approved by NASA/GSFC, in order to be listed in the latest revision of the GSFC Qualified Products List Directory (QPLD).

4.2.2 QPLD Status. Manufacturers supplying capacitors to this specification shall be listed on the version of NASA GSFC QPLD in effect on the date of purchase order or contract.

- 4.2.3 Product Development Certification. Product Development Certification shall be imposed following any change in design, manufacture, materials, or quality control procedures as reviewed and approved during Product Development Process. Product Re-certification shall be required if it is demonstrated that any stipulation initially presented in the manufacturer's certification no longer applies. Inspection discrepancies that are not suitably explained by failure analysis, or by other means, shall also be considered a basis for disqualification by GSFC.
- 4.3 Classification of Inspections. Inspections required by this specification shall be classified as follows.
- a. Processing Reliability Verification Test
 - b. In Process Inspection
 - c. Group A Inspection
 - d. Group B Inspection
- 4.3.1 Inspection of Product for Delivery. Inspection of product for delivery to this specification shall consist of Process Reliability Verification Test, In-Process Inspection, Group A Inspection, and Group B Inspection.
- 4.3.2 Inspection Lot. An inspection lot shall be defined in accordance with [MIL-PRF-123](#), paragraph 4.5.2.1.
- 4.4 Process Reliability Verification Test. Each capacitor lot shall meet these requirements prior to all other inspection steps as specified herein.
- 4.4.1 BME Capacitors Construction/Microstructure Analysis. A minimum of two (2) samples per capacitor type shall be cross-section processed from the termination end to reveal the side margins per EIA/ECA-469, Figure D1. A minimum of three (3) samples per capacitor type shall be cross-section processed from the side of the capacitor body to reveal the end margins per EIA/ECA-469, Figure D1. The following construction features shall be measured at three locations using Scanning Electron Microscopy (SEM) on each sample: Dielectric Thickness, Side Margin, End Margin, Cover Plate Thickness, Optical microscope can be used for the measurement of Total Number of Dielectric Layers per capacitor body. When measuring the dielectric layer thickness using SEM two parallel lines should be used and placed as a parallel as possible to the internal electrode layer. The dielectric thickness shall be measured at the smallest distance between two adjacent electrode layers. All measurements shall be photo documented and have a scale bar to reference feature sizes on the photo. Calculate the average dielectric thickness, side margin, end margin, and cover plate thickness.

- 4.4.2 BME Capacitor Acceptance Criterion. At least one of the cross-section samples as prepared as specified in paragraph 4.4.1 herein shall be further processed using wet or dry chemical etch to reveal the dielectric structure. SEM photos shall be taken at a magnification of $\geq 1.5K$ to show the dielectric microstructure where individual ceramic grains are distinguishable. The average grain size shall be measured using Linear Intercept Method per ASTM E112-10, section 13.
- 4.5 In-Process Inspection. In-process inspection shall be as specified in [MIL-PRF-123](#), paragraph 4.6.1 for nondestructive internal examination and as specified herein for destructive physical analysis in paragraph 4.5.1.
- 4.5.1 Destructive Physical Analysis (DPA). Destructive Physical Analysis (pre-termination) shall be performed on each inspection lot of capacitors supplied to this specification. DPA shall be performed in accordance with the requirements of [MIL-PRF-123](#), paragraph 3.6; sample size shall be as specified in [MIL-PRF-123](#), Table XIV. Analysis shall verify compliance with manufacturer's internal design requirements, as well as the requirements of EIA/ECA-469. The DPA shall follow the guidelines specified in NASA document GSFC [S-311-M-70](#).
- 4.6 Group A Inspection. Group A inspection shall be performed on 100% of capacitors supplied to this specification. Group A inspection shall consist of the tests as specified in Table IV performed in the order shown.

Table IV: Group A Inspection

Inspection/Test	Requirement Paragraph	Test Method Paragraph
Thermal Shock	3.10	4.6.1
Voltage Conditioning	3.11	4.6.2
Insulation Resistance at +125°C	3.3	4.6.3
Dielectric Withstanding Voltage	3.4	4.6.4
Insulation Resistance at +25°C	3.5	4.6.5
Capacitance	3.6	4.6.6
Dissipation Factor	3.7	4.6.7
Percent Defective Allowable (PDA)	3.8	4.6.8
Visual Inspection	3.9	4.6.9

- 4.6.1 Thermal Shock. Thermal shock shall be performed in accordance with [MIL-STD-202, Method 107](#), Test Condition A, except the step 3 temperature shall be +125°C and the number of cycles shall be twenty (20), minimum.
- 4.6.2 Voltage Conditioning. Voltage conditioning shall consist of applying twice the rated voltage to the capacitors at the maximum rated temperature of +125°C +4/-0°C, for a minimum of 168 hours and a maximum of 264 hours. Voltage conditioning may be terminated at any time during the 168 to 264 hour time interval, provided that the number of failures detected during the last 48 hours of test is < 0.1%, or one piece. Resistors may be used in lieu of fuses specified by [MIL-PRF-123](#), Figure 4.

- 4.6.3 Insulation Resistance at +125°C. Capacitors shall be tested at +125°C and rated voltage in accordance with [MIL-STD-202, Method 302](#).
- 4.6.4 Dielectric Withstanding Voltage. Capacitors shall be hold for 60 seconds and tested at two and one half times the rated voltage in accordance with [MIL-STD-202, Method 301](#).
- 4.6.5 Insulation Resistance at +25°C. Capacitors shall be charged for 120 seconds and tested at 25°C and rated voltage in accordance with [MIL-STD-202, Method 302](#).
- 4.6.6 Capacitance. Capacitors shall be tested at +25°C, a test frequency of 1 kHz, and 1.0 VAC_{rms} in accordance with [MIL-STD-202, Method 305](#).
- 4.6.7 Dissipation Factor. The dissipation factor shall be measured with a capacitance bridge or other suitable method at a test frequency of 1 kHz and 1.0 VAC_{rms}. The inherent accuracy of the measurement shall be $\leq \pm 2\%$ of the reading plus 0.1% dissipation factor (absolute) unless otherwise specified. Suitable measurement techniques shall be used to minimize errors due to the connections between the measuring apparatus and the capacitor.
- 4.6.8 Percent Defective Allowable (PDA). PDA shall be calculated by combining the DWV failures identified in voltage conditioning (paragraph 4.6.2) and the failures identified in Insulation Resistance at +125°C testing (paragraph 4.6.3), and divided by the number of capacitors submitted to voltage conditioning.
- 4.6.9 Visual Inspection. Visual inspection shall be performed on 100% of the capacitors delivered to this specification, in accordance with [MIL-PRF-123](#), Appendix B, except the magnification shall be 20X, minimum.
- 4.7 Group B Inspection. Group B inspection shall be performed on each inspection lot of capacitors delivered against this specification. Capacitors used for Group B inspections shall have successfully passed all Group A inspections. Group B inspection shall consist of the tests as specified in Table V herein and performed in the order shown.

Table V: Group B Inspection

Inspection	Requirement Paragraph	Test Method Paragraph	Quantity (Accept Number)
Subgroup 1			45 or 125 (0) 1/
Thermal Shock	3.10	4.6.1	
Life Test	3.12	4.7.1	
Insulation Resistance (at 125°C)	3.3	4.6.3	
Dielectric Withstanding Voltage	3.4	4.6.4	
Insulation Resistance (at +25°C)	3.5	4.6.5	
Capacitance	3.6	4.6.6	
Dissipation Factor	3.7	4.6.7	

Table V: Group B Inspection

Inspection	Requirement Paragraph	Test Method Paragraph	Quantity (Accept Number)
Subgroup 2			12(0)
Temperature Humidity Bias	3.13	4.7.2	
Subgroup 3			12(0)
Solderability	3.14	4.7.3	
Subgroup 4			6(0)
Insulation Resistance (at +25°C)	3.5	4.6.5	
Capacitance	3.6	4.6.6	
Dissipation Factor	3.7	4.6.7	
Resistance to Soldering Heat	3.15	4.7.4	
Insulation Resistance (at +25°C)	3.5	4.6.5	
Capacitance	3.6	4.6.6	
Dissipation Factor	3.7	4.6.7	
Subgroup 5			6(0)
Shear Stress	3.16	4.7.5	
Subgroup 6			22(0)
Breakdown Voltage Test	3.17	4.7.6	
Subgroup 7			6(0)
Board Flex Test	3.18	4.7.7	

1/ If dielectric thickness is ≥ 0.8 mils) quantity is 45. If dielectric thickness is < 0.8 mils, quantity is 125

- 4.7.1 Life Test. Capacitors shall be tested in accordance with [MIL-STD-202, Method 108](#) with the following details and exceptions. Test temperature shall be +125°C, +4/-0°C. Capacitors shall be subjected to the twice the rated voltage.
- 4.7.2 Temperature-Humidity Bias. Capacitors shall be mounted and there shall be one series resistor for each DUT. The value of the series resistor shall be such that there is not greater than 5% voltage drop across the resistor. Initial Insulation Resistance at 25°C shall be measured as specified in paragraph 4.6.3 herein. Capacitors shall be subjected to an environment of +85°C with 85% relative humidity. A dc potential of rated voltage $\pm 5\%$ shall be applied continuously. Upon completion of test, remove capacitors from the chamber and allow 3 hours ± 0.5 hours to dry and stabilize at +25°C before performing the Post-test Insulation Resistance at 25°C measurement as specified in paragraph 4.6.3 herein.

4.7.3 Solderability. Capacitors shall be tested in accordance with one of the following methods:

4.7.3.1 Method 1: Capacitors shall be tested in accordance with [MIL-STD-202 Method 208](#) with following details and exceptions. Each chip capacitor shall be immersed in molten solder. The number of terminations to be tested shall be two (2).

4.7.3.2 Method 2: Capacitors shall be tested in accordance with J-STD-002, Test S.

4.7.4 Resistance to Solder Heat. Capacitors shall be tested in accordance with [MIL-STD-202, Method 210](#), Test Condition J with the following details and exceptions. Only one (1) heat cycle shall be required. After completion of the cleaning process and following a minimum 10-minute to maximum 24-hour cooling period, the Insulation Resistance, Capacitance, and Dissipation Factor shall be measured as specified in paragraphs 4.6.5, 4.6.6, and 4.6.7, respectively.

4.7.5 Shear Stress. Capacitors shall be mounted. Use of epoxy adhesives shall be limited to the terminations only. Pre and post measurement are not applicable. With the component mounted on a PCB, apply the specified force to the side of the device being tested. This force shall be applied for 60 seconds \pm 1 second. The force shall be applied gradually as not to apply a shock to the component being tested. Shear Stress Setup is shown in Figure 2. Shear Stress Force as specified in Table VI herein. Visual examination after test shall be performed as specified in paragraph 4.6.9 herein and under magnification of the mechanical integrity of the device body, terminals, and body/terminal junction.

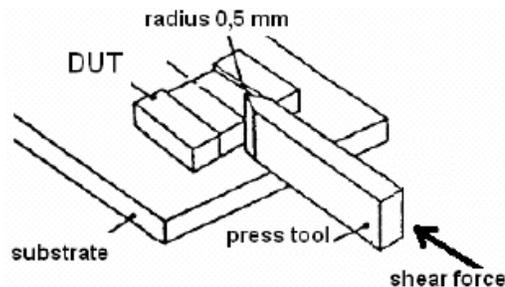


Figure 2 Shear Stress Setup.

Table VI: Shear Stress Force

Part Size	Force
> 1210	1.8 Kg
> 0603 and \leq 1210	1.0 Kg
> 0201 and < 0603	0.5 Kg
\leq 0201	4.1 Kg

4.7.6 Breakdown Voltage Test. Capacitors shall be tested in accordance with MIL-STD-202, Method 301 with the following details. A dc voltage shall be gradually applied until catastrophic failure occurs or when the current reaches 10mA. Voltage at time of failure shall be recorded.

NOTE: 1. During voltage ramping large value capacitors might have large displacement currents that can result in power supply instability and cause false reading of VBR. For this reason, a voltage ramp of 25 V/sec shall be used for parts 1 μ F and above and 100 V/sec for parts below 1 μ F.

NOTE: 2. Due to high leakage currents and thermal nature of breakdown in low-voltage BME capacitors, thermal conditions affect results of measurements. For this reason, BME capacitors shall be immersed in a dielectric fluid such as a stable fluorocarbon-based insulating liquid.

4.7.7 Board Flex Test. Capacitors shall be tested per AEC-Q200-005 with a bend radius of 0.08 inches minimum.

- a. Initial capacitance shall be measured as specified in paragraph 4.6.6 herein.
- b. Post-test capacitance shall be measured as specified in paragraph 4.6.6 herein.
- c. Post-test Dissipation Factor shall be measured as specified in paragraph 4.6.7 herein.
- d. Post-test visual examination shall be performed as specified in paragraph 4.6.9 herein.

4.7.8 Group B Samples. Capacitors used for Group B inspections shall not be delivered as flight material. Test samples, or their remains, shall be packaged separately and delivered with the Group B data package.

4.8 Deliverable data package. Each shipment of capacitors supplied to this specification shall contain the following information as a minimum.

- a. Certificate of Conformance
- b. DPA report
- c. Attribute summary data for Group A and Group B inspections
- d. Variables data for Group B, life test

5. **PREPARATION FOR DELIVERY**

5.1 Packaging Requirements. Capacitors shall be clean, dry, and packaged as per the part number designation, in an electrostatic discharge (ESD) safe package, in a secure manner that will afford adequate protection against corrosion, deterioration, and physical damage during common carrier shipment to the procuring activity. These packages shall conform to the applicable carrier rules and regulations.

5.1.1 Bulk Packaging. Bulk packaging of any capacitors supplied to this specification is not permitted.

6. NOTES

- 6.1 Ordering Data. Acquisition documents shall specify the following minimum information.
- a. Number, title, and date of this specification
 - b. Goddard PIN
 - c. Quantity
- 6.2 Notice. When GSFC drawings, specification, or other data are used for any purpose other than in connection with a definitely related GSFC procurement operation, the United States Government thereby incurs no responsibility nor any obligation whatsoever; the fact that GSFC might have formulated, furnished, or in any way supplied the said drawings, specification, or other data is not to be regarded by implication or otherwise in any manner licensing the holder or any person or corporation, or conveying any right or permission to manufacture, use, or sell any patented invention that may in any way be related thereto.
- Custodian: QPLD Administrator
Parts, Packaging, and Assembly Technologies Office, Code 562
Goddard Space Flight Center
8800 Greenbelt Road
Mailstop 562.0
Greenbelt, Maryland 20771
- 6.3 Approved Source(s) of Supply. Identification of the suggested source(s) of supply hereon is not to be construed as a guarantee of present or continued availability as a source of supply for the item.
- 6.4 Use and Application Information. Capacitors supplied to this specification have been subjected to Product Verification Certification (Process Reliability Verification Test, In-Process Inspection, Group A Inspection, and Group B Inspection with PDC requirements) and lot specific Group A Inspection and Group B Inspection in accordance with the requirements of this specification. Manufacturers of capacitors authorized to supply to this specification are currently listed on the GSFC QPLD for S-311-P-838.
- 6.5 Mounting. The mounting of chip BME capacitors should follow the manufacturer's recommendations. The hand soldering of chip capacitors onto circuit boards is strongly discouraged. It is highly recommended to use only hot air soldering tools for rework.